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Part 6: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points

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Introduction

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For international standards, comments will be reviewed by the relevant UK national committee before sending the consensus UK vote and comments to the international committee, which will then decide appropriate action. If the international standard is approved, it is usual for the text to be published as a British Standard.

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Template for comments and secretariat observations

Date: xx/xx/20xx	Document: ISO/DIS xxxx
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1	2	(3)	4	5	(6)	7
MB	Clause No./ Subclause No./Annex (e.g. 3.1)	Paragraph/Figure/ Table/Note	Type of comment	Commend (justification for change) by the MB	Proposed change by the MB	Secretariat observations on each comment submitted
	3.1	Definition 1	ed	Definition is ambiguous and needs clarifying.	Amend to read '...so that the mains connector to which no connection...'	
	6.4	Paragraph 2	te	The use of the UV photometer as an alternative cannot be supported as serious problems have been encountered in its use in the UK.	Delete reference to UV photometer.	



47D/969/CD

COMMITTEE DRAFT (CD)

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47D/951/NP, 47D/956A/RVN

IEC SC 47D : SEMICONDUCTOR DEVICES PACKAGING	
SECRETARIAT: Japan	SECRETARY: Mr Hiroyoshi Yoshida
OF INTEREST TO THE FOLLOWING COMMITTEES: TC 91	PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CD to the secretary.
FUNCTIONS CONCERNED: ☐ EMC ☐ ENVIRONMENT ☐ QUALITY ASSURANCE ☐ SAFETY	

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TITLE:

Thermal standardization on semiconductor packages - Part 6: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points

NOTE FROM TC/SC OFFICERS:

CD file is attached.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES

Part 6: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points

FOREWORD

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IEC 63378-6 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47D/XX/FDIS	47D/XX/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement to Part 1.

126 at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are
127 described in greater detail at www.iec.ch/publications.

128 The committee has decided that the contents of this document will remain unchanged until the
129 stability date indicated on the IEC website under webstore.iec.ch in the data related to the
130 specific document. At this date, the document will be

- 131 • reconfirmed,
- 132 • withdrawn,
- 133 • replaced by a revised edition, or
- 134 • amended.

135

INTRODUCTION

The IEC 63378-6 series is composed of the following parts:

- IEC 63378-6-1 defines the model creation method using a datasheet of semiconductor devices.
- IEC 63378-6-2 defines the model creation method using measurement data of semiconductor devices.

The IEC 63378-6 series includes subjects such as the definition of a new thermal compact model for thermal transient analysis of semiconductor package, model creation methods, accuracy assessment of these models, etc.

THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES

Part 6: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points

1 Scope

This part of IEC 63378 specifies a thermal resistance and capacitance model for semiconductor packages. This model is named the Digital Transformation using thermal Resistance and Capacitance (DXRC) model. It predicts transient temperature at junction and measurement points.

This document applies to semiconductor packages such as TO-252, TO-263, and HSOP. It supports single chip packages dissipated heat from single package surface.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60191-2:2012 DB, *Mechanical standardization of semiconductor devices - Part 2: Dimensions*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1
junction temperature
temperature at an arbitrary position of the chip

3.2
thermal resistance
quotient of the difference between the virtual temperature of the device and the temperature of a stated external reference point, by the steady-state power dissipation in the device

[SOURCE: IEC 60050-521, 521-05-13]

3.3
thermal capacitance
ability of a material to store thermal energy, calculated by product of specific heat and density

3.4**thermal resistance from junction to case top** θ_{JC}

thermal resistance between a junction and a semiconductor package surface

3.5**Thermal RC topology**

thermal network consisting of several thermal resistances, capacitances, and nodes

3.6 T_J

thermal node representing the junction in a thermal RC topology

3.7 T_{CORE}

internal thermal node as a branch point, not representing any actual location

3.8 T_N internal thermal nodes between T_J and T_{CORE} , not representing any actual locations, a natural number starting from the one closest to T_J for N**3.9** T_{TOP}

thermal node representing an arbitrary position on the top surface of the package, with a surface based on the top surface of the package, that exchanges heat with the surrounding environment

3.10 T_C

internal thermal node representing at an arbitrary position on the bottom metal surface of the package

3.11 T_{BI}

thermal node with a surface based on the metal surface directly under the chip, that exchanges heat with the surrounding environment

3.12 T_{BO}

thermal node with a surface based on the bottom resin surface of the package, that exchanges heat with the surrounding environment

3.13 T_L

internal thermal node representing an arbitrary position on the lead terminals

3.14 T_{LB}

thermal node with surfaces based on the bottom surface of the lead terminals, that exchange heat with the surrounding environment

3.15 T_S

internal thermal node representing an arbitrary position on a metal heat spreader of the package