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Part 3: Evaluation method of spike dependent plasticity in memristor devices

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Introduction

This draft standard is based on national and international discussions. Your comments on this draft are invited and will assist in the preparation of the consequent standard.

For international standards, comments will be reviewed by the relevant UK national committee before sending the consensus UK vote and comments to the international committee, which will then decide appropriate action. If the international standard is approved, it is usual for the text to be published as a British Standard.

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Template for comments and secretariat observations

Date: xx/xx/20xx	Document: ISO/DIS xxxx
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1	2	(3)	4	5	(6)	7
MB	Clause No./ Subclause No./Annex (e.g. 3.1)	Paragraph/Figure/ Table/Note	Type of comment	Commend (justification for change) by the MB	Proposed change by the MB	Secretariat observations on each comment submitted
	3.1	Definition 1	ed	Definition is ambiguous and needs clarifying.	Amend to read '...so that the mains connector to which no connection...'	
	6.4	Paragraph 2	te	The use of the UV photometer as an alternative cannot be supported as serious problems have been encountered in its use in the UK.	Delete reference to UV photometer.	



47/2876/CD

COMMITTEE DRAFT (CD)

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SUPERSEDES DOCUMENTS: 47/2812/NP, 47/2838/RVN	

IEC TC 47 : SEMICONDUCTOR DEVICES	
SECRETARIAT: Korea, Republic of	SECRETARY: Mr Cheolung Cha
OF INTEREST TO THE FOLLOWING COMMITTEES:	HORIZONTAL FUNCTION(S):
ASPECTS CONCERNED:	

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TITLE:

Semiconductor devices - Neuromorphic devices - Part 3: Evaluation method of spike dependent plasticity in memristor devices

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**Semiconductor devices - Neuromorphic devices-
Part 3: Evaluation method of spike dependent plasticity in memristor
devices**

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International Standard IEC 63550-3 has been prepared by technical committee 47: Semiconductor devices.

The text of this International Standard is based on the following documents:

NP	Report on voting
47/2812/NP	47/2838/RVN

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, and the ISO/IEC Directives, JTC 1 Supplement available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

Semiconductor devices - Neuromorphic devices-

Part 3: Evaluation method of spike dependent plasticity in memristor devices

1 Scope

This part of IEC 62951 specifies the test methods for evaluating the spike dependent plasticity of neuromorphic memristor devices. The test methods in this international standard include spike time dependent plasticity (STDP), indirect STDP, spike rate dependent plasticity (SRDP), and their retention properties. This document shall be applicable to neuromorphic memristor devices without any limitations prone to device technology and size.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 62951-9:2022 Semiconductor devices - Flexible and stretchable semiconductor devices Part 9: Performance testing methods of one transistor and one resistor (1T1R) resistive memory cells

3 Terms and definitions

For the purpose of this document, the following terms and definitions apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1 pre voltage

V_{pre}
bias applied to the pre terminal (top electrode) of the memristor devices

3.2 post voltage

V_{post}
bias applied to the post terminal (bottom electrode) of the memristor devices

3.3 memristor

a non-linear two terminal electrical component that limits or regulate the flow of electrical current in a circuit and remembers the amount of charge that has previously flowed through it.

3.4 forming voltage

V_{Form}
high voltage applied across the active layer in the memristor to induce defects within the active layer to form a filament or conduction path initially

3.5 resistance of low resistance state

R_{LRS}
resistance of memristor in potentiation state

3.6**resistance of high resistance state** R_{HRS}

resistance of memristor in depression state

3.7**trip point resistance** R_{TRP} intermediate reference resistance between R_{HRS} and R_{LRS}

$$R_{HRS} > R_{TRP} > R_{LRS} \quad (1)$$

memristor program voltage V_P

voltage applied to the top electrode (TE) of memristor in order to change its resistance state

3.8**step voltage** V_{Step}

ramp of voltage intervals applied to memristor

3.9**read voltage** V_{Read}

specific voltage for measuring the resistance of memristor

3.10**read current** I_{Read} specific current value at V_{Read} of memristor**3.11****resistance of memristor** R_R resistance value at V_{Read} , defined by the following formula

$$R_R = \frac{V_{Read}}{I_{Read}} \quad (2)$$

3.12**conductance of memristor** G_R conductance value at V_{Read} , defined by the following formula

$$G_R = \frac{I_{Read}}{V_{Read}} \quad (3)$$

3.13**Potential voltage** V_{Po}

voltage required to increase the conductance state of the memristor after forming process

3.14**Depression voltage** V_{De}

voltage required to switch to decrease the conductance state of the memristor