



DPC: 25 / 30510059 DC

BSI Group Headquarters

389 Chiswick High Road London W4 4AL

Tel: +44 (0)20 8996 9000

Fax: +44 (0)20 8996 7400

www.bsigroup.com

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Part 2-2: 3D thermal simulation models of semiconductor packages for steady-state analysis - PBGA and FBGA packages

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Direct tel: **020 8996 7009**
E-mail: csc@bsigroup.com

Introduction

This draft standard is based on national and international discussions. Your comments on this draft are invited and will assist in the preparation of the consequent standard.

For international standards, comments will be reviewed by the relevant UK national committee before sending the consensus UK vote and comments to the international committee, which will then decide appropriate action. If the international standard is approved, it is usual for the text to be published as a British Standard.

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Please indicate whether you consider the UK should submit a negative (with supporting technical reasons) or positive vote on this draft. Please indicate if you are aware of any reason why this draft standard should not be published as a British Standard.

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Template for comments and secretariat observations

Date: xx/xx/20xx	Document: ISO/DIS xxxx
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1	2	(3)	4	5	(6)	7
MB	Clause No./ Subclause No./Annex (e.g. 3.1)	Paragraph/Figure/ Table/Note	Type of comment	Commend (justification for change) by the MB	Proposed change by the MB	Secretariat observations on each comment submitted
	3.1	Definition 1	ed	Definition is ambiguous and needs clarifying.	Amend to read '...so that the mains connector to which no connection...'	
	6.4	Paragraph 2	te	The use of the UV photometer as an alternative cannot be supported as serious problems have been encountered in its use in the UK.	Delete reference to UV photometer.	



47D/986/CD

COMMITTEE DRAFT (CD)

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SUPERSEDES DOCUMENTS:
47D/964/NP, 47D/972A/RVN

IEC SC 47D : SEMICONDUCTOR DEVICES PACKAGING	
SECRETARIAT: Japan	SECRETARY: Mr Hiroyoshi Yoshida
OF INTEREST TO THE FOLLOWING COMMITTEES: TC 91	HORIZONTAL FUNCTION(S):
ASPECTS CONCERNED: Digital content,Energy Efficiency	

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TITLE:

Thermal standardization on semiconductor packages - Part 2-2: 3D thermal simulation models of semiconductor packages for steady-state analysis - PBGA and FBGA packages

NOTE FROM TC/SC OFFICERS:

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –**Part 2-2: 3D thermal simulation models of semiconductor packages for steady-state analysis - PBGA and FBGA packages****FOREWORD**

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IEC 63378-2-2 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC technical committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47D/XX/FDIS	47D/XX/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –

Part 2-2: 3D thermal simulation models of semiconductor packages for steady-state analysis - PBGA and FBGA packages

1 Scope

This part of IEC 63378 specifies three-dimensional (3D) thermal models of PBGA (Plastic Ball Grid Array) and FBGA (Fine pitch Ball Grid Array) packages, utilized in the steady-state thermal analysis of electronic devices to estimate junction temperatures accurately.

This model is intended to be made by semiconductor suppliers and to be used by assembly makers of electronic devices.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 63378-2-1 :ED1, *Thermal standardization on semiconductor packages - Part 2-1: 3D thermal simulation models of semiconductor packages for steady-state analysis - Discrete packages*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1 interposer substrate

a space transformer circuit element with terminations that connect the die or packaged device to the system board via terminals, ball-grid arrays, direct metal connections or sockets

Note 1 to entry: Substrate is sometimes used in place of interposer. Interposer is adopted in this document.

4 Attributes of 3D thermal models

4.1 General

PBGA structure is shown in Figure 1. This package is composed of a die, bonding wires, a die attach, a molding, an interposer and solder balls.

FBGA indicates finer (0,8 mm or less solder pitch) BGA compared to PBGA.

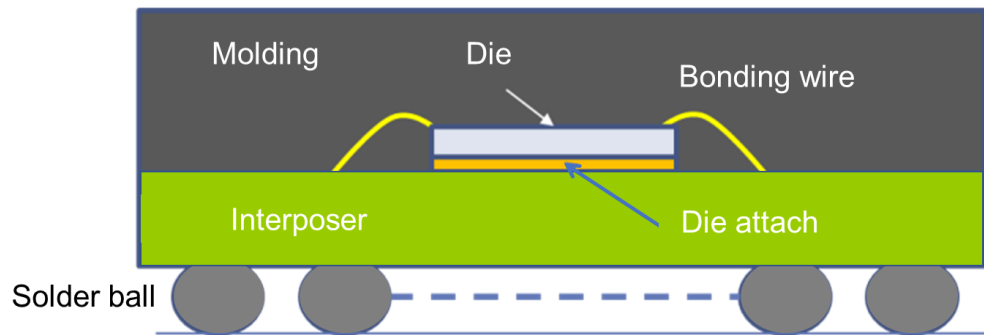


Figure 1 – PBGA structure

This clause 4 shows the attributes such as dimensions and thermal conductivities of the packages. These attributes are used to make a thermal simulation model of the package.

This simulation model should apply to a uniform die heating case. If a die is divided into multiple regions and the heat that each region generates is input, a local die heating case may be applied.

4.2 Geometry

4.2.1 Geometries except solder ball region

This semiconductor package model shall have the attributes as indicated in Table 1. All the attributes of Table 1 are shown in Figure 2.

Table 1 – Attributes except solder ball region

Attribute	Symbol	Value	Unit	Remark
Package width	D		mm	
Package length	E		mm	
Package thickness	A		mm	
Standoff	$A1$		mm	
Interposer thickness	$A2$		mm	
Die attach thickness	$A3$		mm	
Die thickness	$A4$		mm	
Die width	X		mm	
Die length	Y		mm	
Die horizontal offset	ZX		mm	
Die vertical offset	ZY		mm	