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Introduction

This draft standard is based on national and international discussions. Your comments on this draft are invited and will assist in the preparation of the consequent standard.

For international standards, comments will be reviewed by the relevant UK national committee before sending the consensus UK vote and comments to the international committee, which will then decide appropriate action. If the international standard is approved, it is usual for the text to be published as a British Standard.

For national standards, comments will be reviewed by the relevant UK national committee and the resulting standards published as a British Standard.

UK Vote

Please indicate whether you consider the UK should submit a negative (with supporting technical reasons) or positive vote on this draft. Please indicate if you are aware of any reason why this draft standard should not be published as a British Standard.

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Template for comments and secretariat observations

Date: xx/xx/20xx	Document: ISO/DIS xxxx
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1	2	(3)	4	5	(6)	7
MB	Clause No./ Subclause No./Annex (e.g. 3.1)	Paragraph/ Figure/Table/Note	Type of comment	Comment (justification for change) by the MB	Proposed change by the MB	Secretariat observations on each comment submitted
	3.1	Definition 1	ed	Definition is ambiguous and needs clarifying.	Amend to read '...so that the mains connector to which no connection...'	
	6.4	Paragraph 2	te	The use of the UV photometer as an alternative cannot be supported as serious problems have been encountered in its use in the UK.	Delete reference to UV photometer.	

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Safety

☐ SUBMITTED FOR CENELEC PARALLEL VOTING

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TITLE:

Functional safety of electrical/electronic/programmable electronic safety-related systems Part 2-1: Requirements for complex semiconductors

PROPOSED STABILITY DATE: 2030

NOTE FROM TC/SC OFFICERS:

IEC 61508 is the basic safety publication for the functional safety of electric, electronic and programmable electronic systems (E/E/PES). Since publication of Edition 2 in 2010 it has become apparent that the requirements related to semiconductors are now out of date with many changes planned for revision 3 of IEC 61508-2 which is now due out around 2027.

For first CD IEC 61508-2-1 was a TS but as part of the comment review a request has been submitted to the plenary meeting in Calgary to update IEC 61508-2-1 to a full standard. In addition the semiconductor content from IEC 61508 parts 1 to 7 has been removed.

Due to committee meetings planned at the end of May in Pisa, Italy, it is appreciated to voluntarily submit comments on this Part of the IEC 61508 series by 2025-05-12 already. Of course, there will be all comments accepted for consideration by the committee arriving within the official circulation period, but it will help the committee for starting their work on the project phase

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FUNCTIONAL SAFETY OF ELECTRICAL/ELECTRONIC/PROGRAMMABLE ELECTRONIC SAFETY-RELATED SYSTEMS

Part 2-1: Requirements for complex semiconductors

FOREWORD

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The text of this TS is based on the following documents:

DTS	Report on voting
65A/xxx/DTS	65A/xxx/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

241 The committee has decided that the contents of this document will remain unchanged until the
242 stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to
243 the specific document. At this date, the document will be.

- 244 • reconfirmed,
- 245 • withdrawn,
- 246 • replaced by a revised edition, or
- 247 • amended.

248

249 The National Committees are requested to note that for this document the stability date is
250 2024.

251 THIS TEXT IS INCLUDED FOR THE INFORMATION OF THE NATIONAL COMMITTEES AND WILL BE DELETED
252 AT THE PUBLICATION STAGE.

253

INTRODUCTION

Introduction

This technical specification is intended as an update to the ASIC requirements contained in IEC 61508-2:2010 and IEC 61508-7:2010 Annex E.

The term semiconductor is now used to replace the term ASIC (application specific integrated circuits) as even standard semiconductor devices are used to develop safety applications. While the intention of this annex was to address complex semiconductors the term complex was removed except for the title as the content is relevant to all but the most simple semiconductor devices.

In particular this technical specification gives addition and updated guidance related to

- Updated guidance on the claiming on-chip HFT
- Guidance on how to select a semiconductor for use to develop a safety system
- Guidance on performing safety analysis including that required to calculate an SFF
- Guidance on reliability predictions for integrated circuits
- Guidance on the requirements for on-chip software
- The prevention of the introduction of systematic failures during the design of analog and mixed signal devices
- Guidance on the application of route 2s (proven in use) to semiconductors
- Defines class 0,1 and 2 semiconductors
- Adds additional guidance on the design of mixed signal and analog semiconductors

FUNCTIONAL SAFETY OF ELECTRICAL/ELECTRONIC/PROGRAMMABLE ELECTRONIC SAFETY-RELATED SYSTEMS

Part 2-1: Requirements for complex semiconductors (IEC 61508-2-1:202X)

1 Scope

This International stand

- a) is intended to replace the guidance in IEC 61508-2 for semiconductor devices
- b) adds additional guidance for analog and mixed signal integrated circuits

This annex does not apply to simple semiconductor devices such as MOSFETS, transistors or diodes where all the failure modes are easily recognized and known.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this TS. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

- [1] ISO/IEC 61508-1 ed. 2.0: Functional Safety of electrical/electronic/programmable electronic safety-related systems, Part 1: General requirements IEC Geneva
- [2] IEC/TS 61508-2 ed. 2.0: Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 2: Requirements for electrical/electronic/programmable electronic safety-related systems IEC Geneva
- [3] IEC/TS 61508-3 ed. 2.0: Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 3: Software Requirements version as discussed
- [4] ISO/IEC 61508-4 ed. 2.0: Functional Safety of electrical/electronic/programmable electronic safety-related systems, Part 4: Definitions and abbreviations IEC Geneva
- [5] IEC/TS 61508-5 ed. 2.0: Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 5 Examples and methods for the determination of safety integrity levels, IEC Geneva
- [6] IEC 61508-6 ed. 2.0: Functional Safety of electrical/electronic/ programmable electronic safety-related systems, Part 6: Guidelines on the application of IEC 61508-2 and IEC 61508-3 IEC Geneva
- [7] ISO/IEC 61508-7 ed. 2.0: Functional Safety of electrical/electronic/ programmable electronic safety-related systems, Part 7: Overview of techniques and measures, IEC Geneva

3 Definitions and abbreviations

A term that occurs only once in this standard, is defined by a footnote. The definitions and abbreviations given in IEC 61508-4 apply. They are not repeated here. The following ones are used additionally.

3.1 Terms

3.1.2**Class 0 semiconductor**

Integrated circuit that either:

- has no safety features or has safety features including diagnostics that can be verified by system-integrator / hardware designer without knowledge of details of the design

or

- were not developed per IEC 61508. Example: Mass-produced electronic integrated circuits such as a standard microprocessor.

Note – Safety features include diagnostics and things like the use of two ground pins where one is normally sufficient.

3.1.3**Class 1 semiconductor**

Integrated circuit developed to a systematic capability. An IC integrator can make use of internal hardware built in diagnostics to diagnose failures within or outside the IC as part of their safety case.

Examples: An IP develop according to a specific systematic capability (SC), analogue to digital convertor with internal diagnostic test modes to detect faults

3.1.4**Class 2 semiconductor**

Integrated circuit developed to a systematic capability. An IC integrator can make use of internal hardware built in diagnostics to diagnose failures within or outside the IC and internal HFT as part of their safety case.

Example: Integrated circuit (IC) / ASIC implementing a 1oo2 architecture

Note 1 - Class 0/1/2 semiconductor can be classified as type A or type B. See IEC 61508-2 7.4.4.1.2 and 7.4.4.1.3 for a description of type A and type B.

Note 2 - Safety features are e.g. integrity measures like diagnostics

Note 3 – class 2 is a superset of class 1

3.2 Selection of techniques and measures**3.2.1 M**

the technique or measure is required(mandatory) at this systematic capability level

3.2.2 HR

the technique or measure is highly recommended at this systematic capability level. If this technique or measure is not used, then the rationale behind not using it should be detailed and agreed with the independent assessor;

Note 1 – a suitable justification might occupy several pages.

Note 2 – for software IEC 61508-3 Annex C offers guidance in a proper selection of techniques and measures

3.2.3 R

the technique or measure is recommended at this systematic capability level. If this technique or measure is not used or none of possible alternatives is used, then the rationale behind not using it should be detailed and agreed with the independent assessor;

Note 1 – a suitable justification might occupy a paragraph

Note 2 – for software IEC 61508-3 Annex C offers guidance in a proper selection of techniques and measures

3.2.4 PR

the technique or measure has no recommendation for or against being used;

3.2.5 NR

the technique or measure is positively not recommended at this systematic capability level. If this technique or measure is used, then the rationale behind using it should be detailed;

4 E/E/PE system safety lifecycle requirements

The design of the semiconductor devices, shall meet all of the requirements a) to e) as follows:

- a) the requirements for hardware safety integrity comprising;
 - the architectural constraints on hardware safety integrity (see IEC 61508-2 7.4.4), and
 - the requirements for quantifying the effect of random failures (see IEC 61508-2 7.4.5);
 - b) For semiconductor classes 0,1,2 the relevant requirements from Annex A. In addition, for class 2 semiconductors the additional requirements from Annex B must be met.
 - c) the requirements for systematic safety integrity (systematic capability), which can be met by achieving one of the following compliance routes:
 - Route 1_S: compliance with the requirements for the avoidance of systematic faults (see IEC 61508-2 7.4.6 and IEC 61508-3) and the requirements for the control of systematic faults (see IEC 61508-2 7.4.7 and IEC 61508-3), or
 - Route 2_S: compliance with the requirements for evidence that the equipment is proven in use (see IEC 61508-2 7.4.10)
- NOTE 1 The “S” subscript in the above routes designates systematic safety integrity to distinguish it from Route 1_H, and Route 2_H for hardware safety integrity.
- Note 2 - while HDL (hardware definition languages) such as Verilog and VHDL are not software route 3S can be applied to HDL like artefacts
- d) the requirements for system behaviour on detection of a fault (see IEC 61508-27.4.8);
 - e) the requirements for data communication processes (see IEC 61508-2 7.4.11).
 - f) requirements for diagnostic function in conformance with IEC 61508-2 7.4.12, unless justification can be given that the same level of functional safety is reached.

5 Guidance on IP

IP (intellectual property) can be made available in the form or hard or soft (for instance Verilog or VHDL) macros to use in building a complete IC. For specific guidance on the use of IP see Annex E.

Annex A (normative)

Techniques and measures for integrated circuits

This annex covers the following topics

A.1 – General

A.2 - Design of safety related elements or components using class 0, 1, 2 semiconductors

A.3 – Class 0 semiconductor components

A.4 – Application of route 2_s to semiconductors

A.5 – Detailed design techniques for a new semiconductor

A.6 – Failure modes and distributions for semiconductors

A.6.1 – FMEDA for a semiconductor

A.6.1.1 – Definitions of safe, dangerous and no effect failures for semiconductors

A.6.2 – Soft errors on semiconductors

A.6.3 – Semiconductors featuring on diagnostics and safety mechanisms

A.6.4 - Interpretation of tables A.2 to A.14 for a semiconductor

A.7 – Safety manuals and safety datasheets for semiconductors

A.8 – Treatment of semiconductors developed to ISO 26262:2018

A.9 – Software implemented on semiconductors by the semiconductor manufacturer

A.10 – Multicore – hardware aspects

A.11 – Fault injection/insertion for semiconductors

A.12 – Reliability prediction for semiconductors

A.13 - Guidance on application and design of FPGA

A.14 – Failure of on-chip diagnostics

A.15 - References

A.1 General

An IC (integrated circuit) consists of at least one die which contains the active circuitry and that die is then typically packaged in a plastic package. However bare die sales are possible and multiple die in the one package are also common. In previous versions of this standard integrated circuits were referred to as ASICs.

A semiconductor can be type A or type B according to IEC 61508-2 7.4.4.1.2 and 7.4.4.1.3.

Note 1 – semiconductors include digital ASICs, FPGA, mixed signal and analog components such as data conversion devices. Semiconductor devices can be programmable or non-programmable.

Note 2 – the person designing an IC into a module or system or PCB will be referred to as an IC integrator in this Annex.

A detailed V-model of the IC development lifecycle is shown in Figure A.1. If another E/E/PE system safety lifecycle or development lifecycle is used, it shall be specified as part of the management of functional safety activities (see Clause 6 of IEC 61508-1), and all the objectives and requirements of each subclause of IEC 61508-2 shall be met.

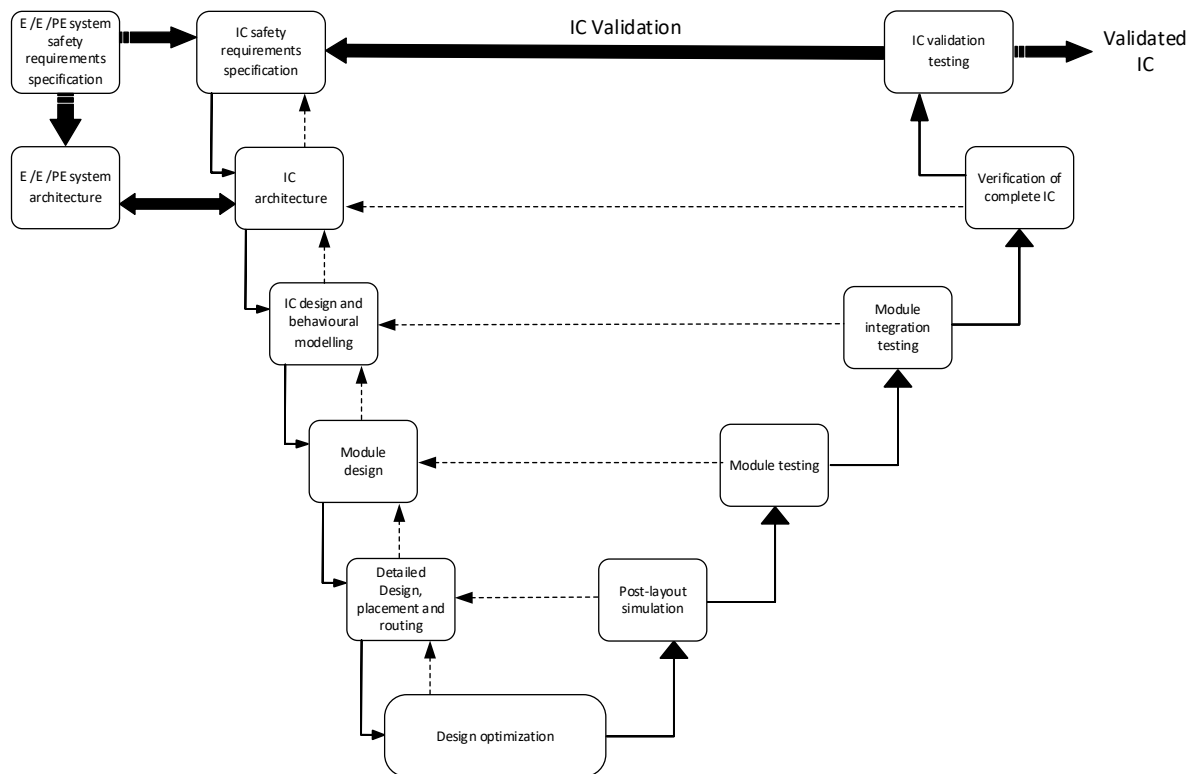


Figure A.1 – semiconductor development lifecycle (the V-Model)

NOTE 3 There are significant similarities between the digital IC description created in an HDL and the software design processes. IEC 61508-3 recommends the V-model for designing safety-related software. The V-model requires a clearly structured design process and a modular software structure for avoiding and controlling systematic faults. The digital IC development lifecycle for the design of IC in Figure A.1 follows this model. At first the requirements for the IC specification are derived from the system requirements. IC architecture, IC design and module design follow. The results of each step on the left-hand side of the V become the input to the next step and are also fed back to the preceding step for iteration where appropriate, until the final design is created. This design is verified against the corresponding design through post-layout simulation, module testing, module integration testing and verification of the complete IC. The results of any step may necessitate a revision to any of the preceding steps. Finally, the IC is validated after its integration into the E/E/PE safety-related system.

A.2 Requirements by semiconductor class

An IC integrator shall tailor their approach depending on the classes of IC used and the reliance placed on that IC to achieve their safety goals.

For ICs where a failure to danger would lead to an immediate increase in risk the following requirements and permissions are given.

Class 0 components – safety shall be taken care of “at the system level” using diverse redundancy and/or diagnostics external to the IC. See A.3 below for more information.

Class 1 components – the IC integrator can rely on internal diagnostics on the IC to diagnose failures within or without the IC and depending on the systematic capability to which the IC was designed redundancy may not be required.

Class 2 components - the IC integrator can rely on internal redundancy and internal diagnostics in the IC to diagnose failures within or outside the IC and depending on the systematic capability to which the IC was designed further external redundancy may not be required.

Semiconductors in classes 1,2 must be developed in compliance to all applicable requirements of IEC 61508 or have evidence that they meet the proven in use requirements (route 2_s from IEC 61508-2) or be developed to ISO 26262 with a suitable gap analysis and closure of all identified gaps. See figure A.2.

Figure A.2 below shows a selection chart for semiconductors. The first leg in the flow chart shows an IC developed in full compliance to IEC 61508 i.e. Route 1_s. For more details see main body of IEC 61508 parts 1 to 7 and IEC 61508-2-1. The second leg shows an argument based on proven in use i.e. route 2_s, see A.4 and IEC 61508-2 7.4.10 for more details. The third leg shows an argument made on an automotive gap analysis, see A.8 and IEC TR 61508-6-1. Legs 4,5 represent the paths for class 0 components, see A.3.

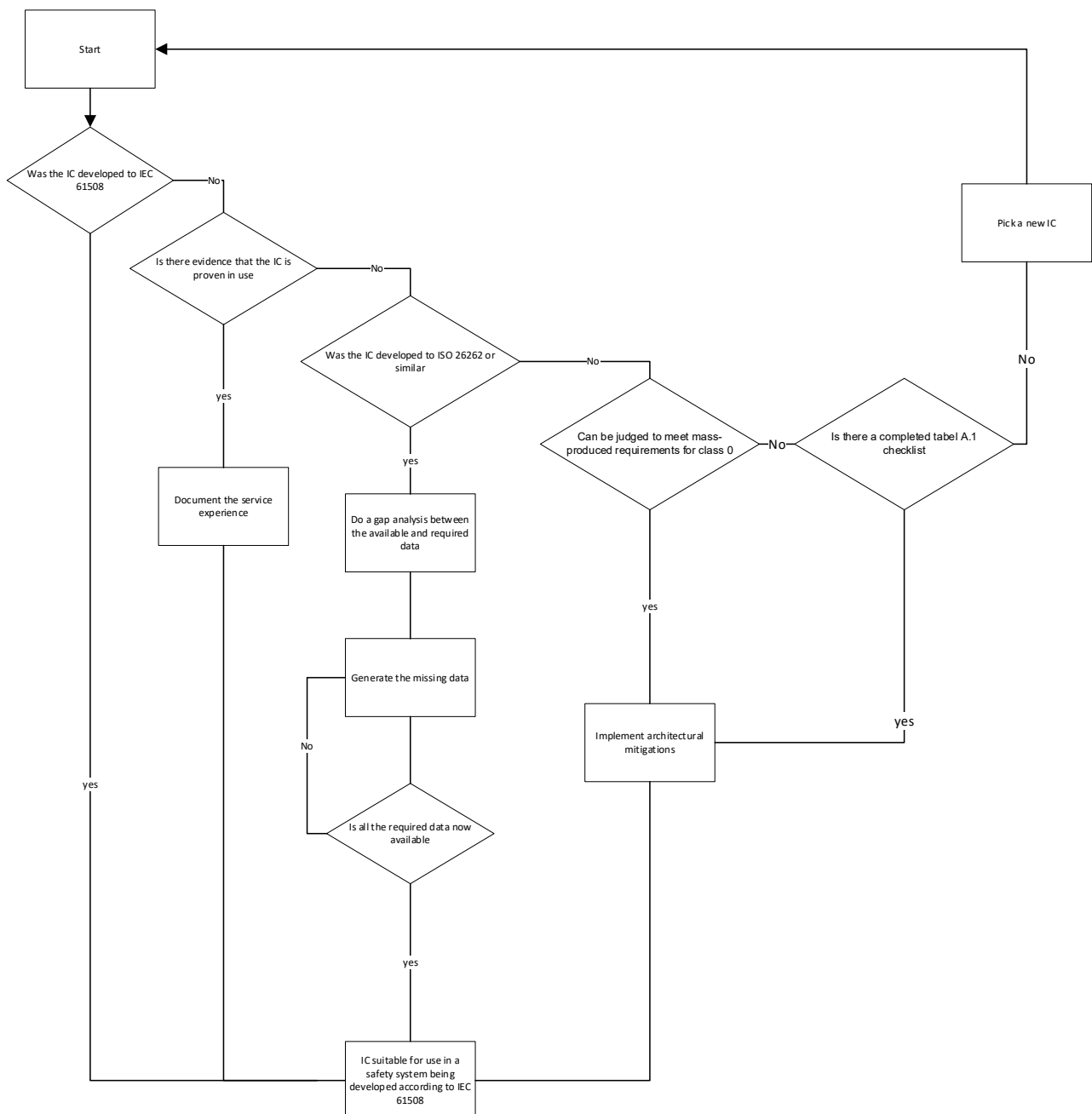


Figure A.2 – Semiconductor selection chart

Note 1 – class 0 semiconductor components replace the concept of mass-produced integrated circuits from IEC 61508-2:2010 7.4.6.1.

Note 2 – the last two legs in the flow chart are effectively the routes from IEC 61508-2:2010 7.4.6.

A.3 Class 0 semiconductor components

This standard does not contain specific requirements relating to the avoidance of systematic faults during the design of class 0 semiconductor component. This is because the likelihood of faults in such devices is minimised by extensive experience of use with significant feedback from users in combination with a semiconductor development process, which can be assumed to enforce stringent procedures and rigorous testing even if there is no evidence for the fulfilment of requirements from table A.1. Class 0 devices new to the market should not be used to build a safety system unless a completed table A.1 checklist is available. In case of doubt, at a minimum the device should be on the market for 1 year for SIL 1 and 2, and 2 years for SIL 3.

When using class 0 devices which don't have a valid route 1s, route 2s or automotive gap analysis argument a justification for using those devices should be made. The integrator shall justify why those devices are suitable to use in their application. The main concern for those designing in the integrated circuits should be systematic failure modes of the integrated circuits.

While temperature range, and other capabilities can be gauged from the standard datasheet and EMI testing can be done at the system level there is always the risk of unknown systematic failure modes internal to a class 0 device.

Release notes, errata sheets etc. must be available of the IC under consideration and must be observed by the IC integrator.

While it is impossible to define general rules on when standard components can be used in safety related system some general techniques are possible

- a) The use of diverse redundancy.
- b) The use of external diagnostics to address systematic failure modes of the item.
- c) The use of external means to achieve the safe state

In addition with both a) and b) the use of an SMOD (secondary means of disconnection) to achieve the safe state, rather than rely on something on the class 0 device itself, is necessary.

For the use of diverse redundancy, the expectation is that it is unlikely that both of the redundant items will have the same design flaw and fail in the same way at the same time. Evidence that this probability is low should be provided.

Example of such evidence might include.

- a) different design companies
- b) different architectures e.g. SAR ADC vs a SIGMA-DELTA
- c) different technologies e.g. FPGA and non-programmable logic

For the use of external diagnostics to address all systematic failure modes the evidence that this probability is low should be provided. Example of such evidence might include a qualitative FMEA showing how the failure modes are addressed. The diagnostic test interval requirements are those for detecting random hardware failures – see for instance IEC 61508-2:2010 7.4.5.3.

Without the use of these techniques concerns arise regarding

- Change control procedures on the manufacture of those integrated circuits.
- Notifications of failures found in those integrated circuits by other users.

In contrast if using components with a valid route 1s, route 2s or automotive gap analysis it may be possible to rely on

- On chip diagnostics

- On chip means to achieve a safe state e.g. asserting a reset pin
- IC manufacturer/designers' reliability predictions

without having to resort to “architectural mitigations” such as diverse redundancy or the use of external diagnostics.

Note systematic concerns dominate since for the hardware metrics, techniques such as identical redundancy can take care of HFT and SFF using two items and diagnostics by comparison.

A.4 Application of route 2s to semiconductors

The requirements from IEC 61508-2 7.4.10 can be used to satisfy the requirements for component classes 1,2.

Note – if the semiconductor contains software, then the requirements of IEC 61508-3 contain the proven in use requirements for that software.

A.5 Detailed design techniques for a new semiconductor

As part of the development of an integrated circuit according to route 1s this sub-clause presents a set of detailed design techniques for the detailed design phase of a semiconductor. These techniques can also be used to justify the use of a new class 0 semiconductor device, where there is no extensive experience of use.

In addition to the measures outlined in the table

NOTE 1 This normative annex is referenced by IEC 61508-2 7.4.6.7.

- a) All design activities and test arrangements, and software offline tools used for the functional simulation and the results of the simulation, should be documented.
- b) All software off-line support tools for the design and verification of the IC used should be evaluated per IEC 61508-3 7.4.4
- c) All activities and their results should be verified, for example by simulation, equivalence checks, timing analysis or checking the technology constraints.
- d) Measures for the reproducibility and automation of the design implementation process (script based, automated work and design implementation flow) should be used.
- e) For claims of on-chip redundancy see Annex E
- f) A quality management system as described in IEC 61508-1 shall be followed

Following the guidelines in this annex does not guarantee by itself the required systematic capability. It is important to consider:

- the consistency of the chosen techniques and measures, and how well they will complement each other;
- which techniques and measures are appropriate, for every phase of the development lifecycle; and
- which techniques and measures are most appropriate for the specific problems encountered during the development of each different E/E/PE safety-related system.

Note 2 – for FPGA/CPLD and such devices the techniques in the “Digital components including FPGA” should be followed by the IC manufacturer and the techniques from the “FPGA/CPLD/PLD application” column by the person programming the FPGA/CPLD device.

Note 3 – the achieved systematic capability can be different from that achieved in terms of the hardware metrics. For instance, a device may be designated as SIL 2/ SC 3 indicating that it was designed to meet SIL 2 in terms of the hardware safety integrity and SC 3 in terms of the systematic capability. Such an IC could be used with identical redundancy to meet the safety

565 requirements for SIL 3 in terms of both the systematic and random hardware fault tolerance
566 metrics.

567 **Table A.1 – Techniques and measures to avoid introducing faults during semiconductor**
568 **design and development**

569

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
Design Entry	<i>IC architecture</i>	1	<i>Structured Description</i>	See C.3	HR	HR	HR	HR	yes	yes	yes	yes
	<i>IC architecture</i>	2	<i>Design Description in an HDL</i>	See C.1	HR	HR	HR	HR	yes	Relevant to digital portion	not relevant	yes
	<i>IC architecture</i>	3	<i>Schematic Entry</i>	See C.2	NR	NR	NR	NR	yes	Guidance is good for digital portions, but schematic entry is the main operating mode for the analog portions	Schematic entry is the main design technique	yes
	<i>IC architecture</i>	4	<i>Design descriptions using Boolean equations</i>		R	R	NR	NR	yes	no	no	yes
	<i>IC architecture</i>	5a	<i>For circuit descriptions that use Boolean equations: manual inspection in designs with limited (low complexity)</i>		HR	HR	HR	HR	yes	no	no	yes
	<i>IC architecture</i>	5b	<i>For circuit descriptions that use Boolean equations: simulation of state transitions in design with higher complexity</i>		HR	HR	HR	HR	yes	no	No	yes
	<i>IC architecture</i>	6	<i>Application a design environment with extensive experience from use</i>		HR	HR	HR	HR	yes	yes	yes	yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	IC design and behavioural modelling, module design, design optimization	7	HDL simulation	See C.5	HR	HR	HR	HR	yes	HDL/analog circuit co-simulation at all SIL levels	Analog circuit simulation	yes
	IC design and behavioural modelling, module design, design optimization	8	Application of simulators with extensive experience from use	See C.4	HR	HR	HR	HR	yes	yes	yes	yes
	Module testing	9	Functional test on module level using HDL test benches	See C.6	HR	HR	HR	HR	yes	Relevant to digital portion	no	yes
	Module integration testing	10	Function test on top level	See C.7	HR	HR	HR	HR	yes	yes	yes	yes
	Verification of the complete IC	11	Functional test embedded in system environment	See C.8	R	R	HR	HR	yes	yes	yes	yes
	Detailed design, placement and routing	12	Restricted use of asynchronous constructs	See C.9	HR	HR	HR	HR	yes	Relevant to digital portion	no	yes
	Detailed design, placement and routing	13	Synchronisation of primary inputs and control of meta-stability	See C.10	HR	HR	HR	HR	yes	Relevant to digital portion	no	yes
	IC architecture	14	Design for testability depending on test coverage in percent	See C.11	R> 95%	R> 98%	R > 99%	R > 99%	yes	yes	yes	no
	IC architecture	15	Modularization	See C.12	R	R	HR	HR	yes	yes	no	yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	Module testing	16	Coverage of the verification scenarios	See C.13	R	R	HR	HR	yes	yes	yes	yes
	Detailed design, placement and routing	17	Observation of coding guidelines	See C.14	HR	HR	HR	HR	yes	Relevant to digital portion	no	yes
	Detailed design, placement and routing	18	Application of code checker	See C.15	HR	HR	HR	HR	yes	Relevant to digital portion	no	yes
	Detailed design, placement and routing	19	Defensive programming	See C.16	R	R	HR	HR	yes	Relevant to digital portion	no	yes
	All simulation phases	20	Documentation of simulation results	See C.17	HR	HR	HR	HR	yes	yes	yes	yes
	Detailed design, placement and routing	21a	Code inspection	See C.18	R	R	HR	HR	yes	Design reviews or walk throughs as opposed to code reviews	Design reviews or walk throughs as opposed to code reviews	yes
	Detailed design, placement and routing	21b	Walk-through	See C.19	R	R	HR	HR	yes	Design reviews or walk throughs as opposed to code reviews	Design reviews or walk throughs as opposed to code reviews	yes
	IC architecture	22a	Application of validated soft cores	See C.20	R	R	HR	HR	yes	Relevant to digital portion	no	yes
	Module testing	22b	Validation of soft cores	See C.21	R	R	HR	HR	yes	Relevant to digital portion	no	yes
	Module design	23	Application of schematic guidelines	See C.14	R	R	R	R	No	yes	yes	yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	Module design and Module testing	24	Verification of behavioural models	See C.47	R	R	R	R	yes	yes	yes	yes
	IC architecture	25	Everything on-chip shall be treated to the highest SIL level of anything on-chip unless sufficient independence can be shown	See Annex B	HR	HR	HR	HR	yes	yes	yes	yes
	IC architecture	26	On-chip software	See A.9	HR	HR	HR	HR	yes	where relevant	no	yes
	IC architecture	27	DFMEA	See C.48	R	R	R	R	yes	yes	yes	yes
	All	28	Requirements traceability	See C.40	HR	HR	HR	HR	yes	yes	yes	yes
	Design optimization	29	Use of matching and dummy devices	See C.49	R	R	R	R	no	yes	yes	no
	IC architecture	30	JTAG port lockout	See C.50	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	IC architecture	31	Debug port lockout	See C.50	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	IC architecture	32	Scan chain lockout feature	See C.50	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
Synthesis	Detailed design, placement and routing	37a	Simulation of the gate netlist to check timing constraints	See C.22	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	Detailed design, placement and routing	37b	Static analysis of the propagation delay	See C.23	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	Detailed design, placement and routing	38a	Verification of the gate netlist against a reference model by simulation	See C.24	R	R	HR	HR	yes	Relevant to the digital portion	no	yes
	Detailed design, placement and routing	38b	Comparison of the gate netlist with the reference model (formal equivalence check)	See C.25	R	R	HR	HR	yes	Relevant to the digital portion	no	no
	Detailed design, placement and routing	38c	Analysis of tool output in particular warnings and errors		R	R	R	R	yes	yes	yes	yes
	Detailed design, placement and routing	39	For PLD/CPLD in complex designs: check of design by simulation		R	R	HR	HR	no	no	no	yes
	Detailed design, placement and routing	40	Check of vendor requirements and constraints	See C.26	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	Detailed design, placement and routing	41	Documentation of synthesis constraints, tools and results	See C.27	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	Verification of the complete IC	42	DIE FMEDA	See A.6.1	HR	HR	HR	HR	yes	yes	yes	Yes
	IC architecture	43	Application of target libraries with extensive experience from use	See C.29	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	Detailed design, placement and routing	44	Script based procedures	See C.30	R	R	HR	HR	yes	Relevant to the digital portion	no	yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
Test	IC architecture	45	Implementation of test structures	See C.31	R > 95%	R>9 8%	R>9 9%	R>9 9%	yes	Relevant to the digital portion	No	no
	Detailed design, placement and routing	46a	Estimation of the test coverage by simulation (based on achieved test coverage in percent)	See C.32	R > 95%	R>9 8%	R>9 9%	R>9 9%	yes	Relevant to the digital portion	no	no
	Detailed design, placement and routing	46b	Estimation of the test coverage by application of ATPG tool (based on achieve test coverage in percent)	See C.33	R > 95%	R>9 8%	R>9 9%	R>9 9%	yes	Relevant to the digital portion	no	no
	Design optimization	47a	Simulation of the gate netlist, to check timing constraints	See C.22	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	Design optimization	47b	Static timing analysis of the propagation delay	See C.23	HR	HR	HR	HR	yes	Relevant to the digital portion	no	yes
	Detailed design, placement and routing	48a	verification of the gate netlist against a reference model by simulation	See C.24	R	R	HR	HR	yes	Relevant to the digital portion	no	yes
	Detailed design, placement and routing	48b	Comparison of the gate netlist with the reference model (formal equivalence check)	See C.25	R	R	HR	HR	yes	Relevant to the digital portion	no	yes
	Post-layout simulation	49	Simulation at the transistor level	See C.52	HR	HR	HR	HR	- good practice to give confidence	yes	-	no

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	Module integration testing	50	Mixed signal simulation	See C.53	HR	HR	HR	HR	no	yes	no	no
	Design optimization	51	Monte-Carlo simulations of the most sensitive blocks	See C.54	R	R	R	R	no	yes	yes	no
	Design optimization	52	Simulation across process corners	See C.55	HR	HR	HR	HR	yes	yes	yes	no
	Design optimization	53	Simulation across temperature	See C.56	HR	HR	HR	HR	yes	yes	yes	No
	Design optimization	54	Simulation of aging	See C.57	R	R	R	R	yes	yes - for analog portions	yes	No
	IC architecture	55	Estimation of analog test coverage	See C.58	R	R	R	R	no - already covered by 28a, 28b	yes - for analog portions	yes	No
	Design optimization	56	EMC simulation and analysis	See C.59	R	R	R	R	no	yes	yes	No
	Verification of the complete IC	58	Lifetime prediction for an assumed stated environment	See C.59	R	R	R	R	yes	yes	yes	No
	IC architecture	59	Soft error rate prediction	See A.5.3	HR	HR	HR	HR	yes	yes - for digital portion	No	yes
Layout	IC architecture	60a	Justification of extensive experience in use for applied hard cores	See C.34	HR	HR	HR	HR	yes	yes	yes	Yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	IC architecture	60b	Application of validated hard cores	See C.35	HR	HR	HR	HR	yes	yes	yes	yes
	Post layout simulation	61a	Simulation of the gate netlist, to check timing constraints	See C.22	HR	HR	HR	HR	yes	yes - for digital portion	No	yes
	Post layout simulation	61b	Static analysis of the propagation delay (STA)	See C.23	HR	HR	HR	HR	yes	yes - for digital portion	No	yes
	Post layout simulation	62a	Verification of the gate netlist against a reference model by simulation	See C.24	HR	HR	HR	HR	yes	yes - for digital portion	No	yes
	Post layout simulation	62b	Comparison of the gate netlist with the reference model (formal equivalence check)	See C.25	HR	HR	HR	HR	yes	yes - for digital portion	No	yes
	Post layout simulation	63	Design rule check (DRC)	See C.37	HR	HR	HR	HR	yes	yes	yes	yes
	Post layout simulation	64	Verification of layout vs schematic (LVS)	See C.38	HR	HR	HR	HR	yes	yes	yes	no
	IC architecture	65	Application design environment and application of cell libraries with extensive experience from use	See C.4	HR	HR	HR	HR	yes	yes	yes	yes

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
	IC architecture	66	Additional process qualification and conservative constraints for process technologies in use for less than 3 years	See C.39	HR	HR	HR	HR	yes	yes - for digital portion	No	no
	Post layout simulation	67	Analysis of the power network	See C.61	HR	HR	HR	HR	yes	yes	yes	no
	Post layout simulation	68	Clock tree balancing/skew reduction	See C.62	HR	HR	HR	HR	yes	yes - for digital portion	No	No
	Post layout simulation	69	Clock domain crossing analysis	See C.63	HR	HR	HR	HR	yes	yes - for digital portion	No	Yes
	Verification of the complete IC	70	Pin FMEDA	See A.6.1	HR	HR	HR	HR	yes	yes	yes	Yes
	Verification of the complete IC	71	Bonding diagram review	See C.64	HR	HR	HR	HR	yes	yes	yes	no
	Verification of the complete IC	72	Layout review	See C.65	HR	HR	HR	HR	yes	yes	yes	No
	Verification of the complete IC	73	Bond pad review	See C.66	HR	HR	HR	HR	yes	yes	yes	No
	Verification of the complete IC	74	ESD review	See C.67	HR	HR	HR	HR	yes	yes	yes	No
	Verification of the complete IC	75	EMC review	See C.68	R	R	R	R	yes	yes	yes	No

<i>Design phase</i>	<i>V model phase</i>	<i>Ref</i>	<i>Technique/Measure</i>	<i>Comment</i>	<i>SC 1</i>	<i>SC 2</i>	<i>SC 3</i>	<i>SC 4</i>	<i>Digital components including FPGA</i>	<i>Application to Analog/Mixed signal</i>	<i>Application to sensors and transducers including MEMS</i>	<i>FPGA/CPLD/PLD application</i>
	Verification of the complete IC	76	Current density review	See C.69	R	R	R	R	yes	yes	yes	No
	Verification of the complete IC	77	Reliability prediction	See A.12	HR	HR	HR	HR	yes	yes	yes	yes
	Verification of the complete IC	78	Latchup review	See C.70	R	R	R	R	yes	yes	yes	No
	Design optimization	79	Thermal simulations	See C.71	R	R	R	R	yes	yes	yes	No
	Design optimization , post-layout simulation	80	Stress analysis (package)	See C.72	R	R	R	R	yes	yes	yes	No
Chip manufacturing	IC architecture	81	Application of device series with extensive experience from use	See C.73	HR	HR	HR	HR	no	no	no	yes
	IC architecture	82	Manufacturing process with extensive experience from use	See C.42	HR	HR	HR	HR	yes	yes	yes	No
		83	Quality assurance for the process technology	See C.74	HR	HR	HR	HR	yes	yes	yes	no
		84	Quality control of the manufacturing process	See C.43	HR	HR	HR	HR	yes	yes	yes	no
		85	Manufacturing quality pass of the device	See C.44	R	R	HR	HR	yes	yes	yes	no
		86	Production quality pass of the device	See C.45	HR	HR	HR	HR	yes	yes	yes	no

Design phase	V model phase	Ref	Technique/Measure	Comment	SC 1	SC 2	SC 3	SC 4	Digital components including FPGA	Application to Analog/Mixed signal	Application to sensors and transducers including MEMS	FPGA/CPLD/PLD application
		87	Test coverage of the manufacturing test	See C.11	> 95%	>98 %	>99 %	>99 %	yes	yes	yes	no
		88	Quality standards	See C.46	HR	HR	HR	HR	yes	yes	yes	no
		89	Quality management system	See C.74	HR	HR	HR	HR	yes	yes	yes	no
	IC validation testing	90	Final verification and validation of the FPGA/PLD in the system	See C.75	HR	HR	HR	HR	No - for digital Yes - for FPGA	no	no	yes
		91	Final verification and validation during mass manufacturing, per-unit-check	See C.76	R	R	HR	HR	No - for digital Yes - for FPGA	no	no	yes
		92	Production test at the temperature extremes	See C.77	R	R	R	R	yes	yes	yes	no
		93	All safety relevant parameters to be specified min/max	See C.78	R	R	R	R	yes	yes	yes	no
		94	use 3 sigma limits on functional safety relevant parameters	See C.79	R	R	R	R	yes	yes	yes	no
	IC architecture	95	Die level traceability	See C.80	R	R	R	R	yes	yes	yes	No
		96	Justification of wafer probe strategy	See C.81	R	R	R	R	yes	yes	yes	No