



DPC: 25/30510635 DC

BSI Group Headquarters

389 Chiswick High Road London W4 4AL

Tel: +44 (0)20 8996 9000

Fax: +44 (0)20 8996 7400

www.bsigroup.com

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E-mail: admin.start@bsigroup.com

Introduction

This draft standard is based on national and international discussions. Your comments on this draft are invited and will assist in the preparation of the consequent standard.

For international standards, comments will be reviewed by the relevant UK national committee before sending the consensus UK vote and comments to the international committee, which will then decide appropriate action. If the international standard is approved, it is usual for the text to be published as a British Standard.

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Please indicate whether you consider the UK should submit a negative (with supporting technical reasons) or positive vote on this draft. Please indicate if you are aware of any reason why this draft standard should not be published as a British Standard.

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Template for comments and secretariat observations

Date: xx/xx/20xx	Document: ISO/DIS xxxx
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1	2	(3)	4	5	(6)	7
MB	Clause No./ Subclause No./Annex (e.g. 3.1)	Paragraph/ Figure/Table/Note	Type of comment	Comment (justification for change) by the MB	Proposed change by the MB	Secretariat observations on each comment submitted
	3.1	Definition 1	ed	Definition is ambiguous and needs clarifying.	Amend to read '...so that the mains connector to which no connection...'	
	6.4	Paragraph 2	te	The use of the UV photometer as an alternative cannot be supported as serious problems have been encountered in its use in the UK.	Delete reference to UV photometer.	



47/2950/CD

COMMITTEE DRAFT (CD)

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IEC TC 47 : SEMICONDUCTOR DEVICES

SECRETARIAT:
Korea, Republic of

SECRETARY:
Mr Cheolung Cha

OF INTEREST TO THE FOLLOWING COMMITTEES:

HORIZONTAL FUNCTION(S):

ASPECTS CONCERNED:

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TITLE:

Semiconductor devices - Performance evaluation of semiconductor processing components and inspection equipment - Part 3: Nano-scale wafer surface inspection method using UV light

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – PERFORMANCE EVALUATION OF SEMICONDUCTOR PROCESSING COMPONENTS AND INSPECTION EQUIPMENT–

Part 3: Nano-scale wafer surface inspection method using UV light

FOREWORD

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The text of this International Standard is based on the following documents:

Draft	Report on voting
XX/XX/FDIS	XX/XX/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available

at https://www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at <https://www.iec.ch/standardsdev/publications>.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under [webstore.iec.ch](https://www.iec.ch/webstore) in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

Recently, the semiconductor market continues to increase, and the demand and importance of semiconductor modules and equipment for manufacturing semiconductor devices are also continuously increasing. With the miniaturization of semiconductor manufacturing processes, the need to develop new semiconductor equipment is also increasing. Therefore, it is necessary to develop an international standard to evaluate the parts and modules used in semiconductor equipment. There are many semiconductor processing components: wafer, mask and pellicle, etc. These components have a significant impact on the performance, reliability, and manufacturing yield of semiconductor devices. Therefore, it is very important to establish the international standards for evaluating or inspecting the parts and modules used in semiconductor equipment.

IEC 6XXX series of standards is planned to focus on performance evaluation of semiconductor processing components and inspection equipment.

Part 1 focuses on the apparatus and its method for measuring the extreme ultraviolet (EUV) transmission of a pellicle used in the EUV lithography process to physically prevent particle contamination of the mask.

Part 2 deals with advanced techniques for inspecting nano-scale defects on wafers using white light interferometry. Thanks to recent development of wafer inspection techniques, even smaller defects can be detected by using UV light source and related optics. Part 3 describes the wafer inspection method by UV light.

The dimensional accuracy of the silicon dies after the dicing process is becoming more important as semiconductor device and packaging technologies have been advanced. Part 4 focuses on evaluation methods for dimensional accuracy of singulated dies by laser dicing process. Laser dicing is one of the most widely used wafer-cutting technologies in the semiconductor device manufacturing processes that require high dimensional accuracy. It is essential to assess the geometric characteristics of the laser-diced wafers and verify their compliance with design specifications.

The current structure of this International Standard is as follows.

Part 1: Transmittance evaluation method of EUV pellicle

Part 2: Nano-scale wafer surface inspection using white light interferometry

Part 3: Nano-scale wafer surface inspection method using UV light

Part 4: Evaluation methods for dimensional accuracy of laser dicing process