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(withdrawn 2002)



## **AES recommended practice for sound reinforcement systems - Communications interface (PA-422) (withdrawn 2002)**

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# **AES Recommended practice for sound-reinforcement systems — Communications interface (PA-422)**

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## **Abstract**

This Audio Engineering Society (AES) Standard specifies the electrical characteristics of a balanced-voltage circuit for the interchange of serial binary signals for the control of sound-reinforcement systems. It provides for interchange among data terminal equipment (DTE), that is, computers and microprocessors, and data circuit-terminating equipment (DCE). PA-422 is a mnemonic, signifying professional audio implementation of Electronics Industries Association EIA-422-A. Device control language is provided in an annex.

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[This foreword is not a part of AES Recommended practice for sound-reinforcement systems — Communications interface (PA-422), AES15-1991.]

### Foreword

This standard has been prepared by the Working Group on Sound System Control, a working group of the Audio Engineering Society Standards Committee. It is designed in the public interest to eliminate misunderstandings between manufacturers, consultants, purchasers, and users, and to facilitate interchangeability, integration, and improvement of products, thus allowing the selection and utilization of the proper product for a particular need.

The standard may involve patents on articles, materials, or processes. The AES assumes no liability to any patent owner, nor does it assume any obligation whatever to parties adopting the standard.

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1990 May

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The American National Standards Institute version of this standard has not been reprinted and remains available as ANSI S4.49-1991.

# AES Recommended practice for sound-reinforcement systems — Communications interface (PA-422)

## 1 Scope

This standard specifies the electrical characteristics of the balanced-voltage circuit that may be used when specified for the interchange of serial binary signals among data terminal equipment (DTE), that is, computers and microprocessors, and data circuit-terminating equipment (DCE) of, or in, any point-to-point interconnection of serial binary signals among digitally controlled equipment. The standard contains a device control language (DCL) for controlling communication among the various products. Annex A covers this device control language. The interface includes a driver and an interconnecting cable to a receiver. The electrical characteristics of the circuitry are similar to and expected to perform in the same manner as those of the Electronics Industries Association standard EIA-422-A, hence the mnemonic, PA-422 for professional audio use.

Minimum performance requirements for the interconnecting cable are furnished. Guidance is given with respect to limitations on the data rate imposed by the parameters of cable length, balance, and termination for individual installations.

## 2 Applicability

The provisions of this standard may be applied to the interfaces used among equipment where the information being conveyed is in the form of serial binary signals at the dc baseband level. This standard shall be referenced by the specifications and specific interface standards applying these electrical characteristics. Typical points of applicability for this standard are depicted in figure 1.

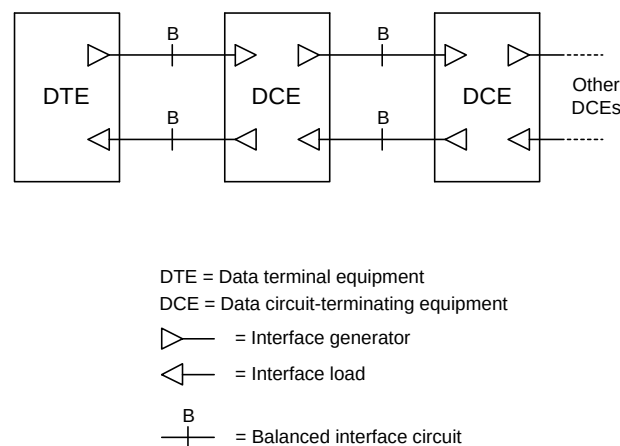


**Figure 1 – Applications of communications interface**

The balanced-voltage digital interface should be utilized on data, timing, or control circuits in appropriate applications. This is to ensure the elimination of any outside electrical interference which might disrupt the operation. The data rate of the signals can range up to over  $10^6$  bits per second. The maximum rate for an individual application is dependent on the cable type and length. While a restriction on maximum cable length is not established, guidelines are given with respect to conservative operating distances as a function of the data signaling rate (see Section 5).

In general, these conservative values may be exceeded where the installation is engineered to ensure that noise and ground potential values are held to a minimum.

In this standard, the term data signaling rate, expressed in units of bits/s, is the significant parameter. Data signaling rate is defined as  $1/T$ , where  $T$  is the minimum interval between two significant instants. In a binary system for which this standard is to apply, the data signaling rate, in bits per second, and the modulation rate, in baud, are numerically equal when the unit interval used in each determination is the minimum interval.

### 3 Electrical characteristics

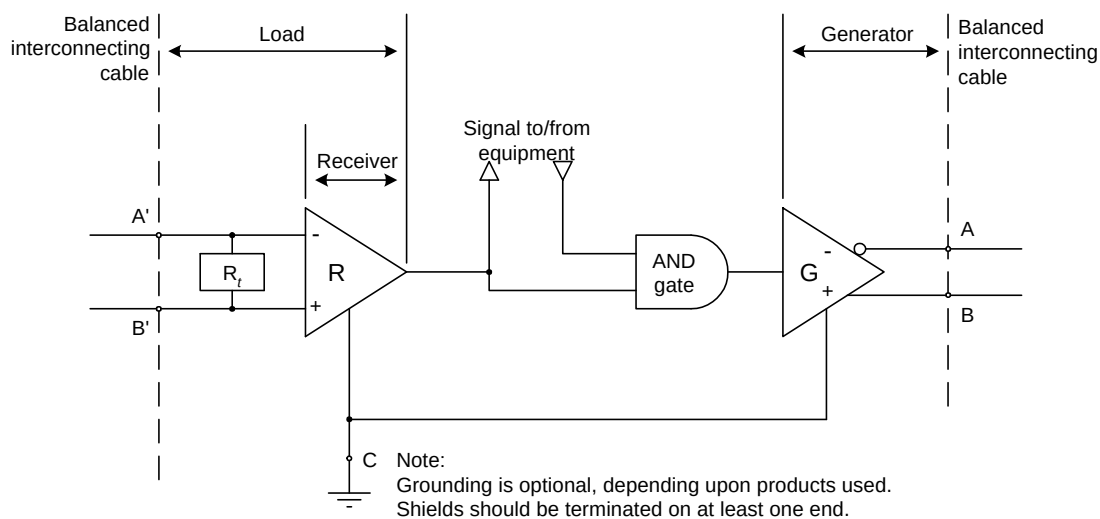
#### 3.1 Configuration

The balanced-voltage digital circuitry consists of three parts: the driver, the balanced interconnecting cable, and the load. For the electrical characteristics of these elements reference should be made to section 4.0 of EIA-422-A for balanced-voltage digital-interface circuits. Figure 2 shows the physical connections of a typical DCE for an interface with multiple DCEs. The nominal differential operating voltage between the balanced signal lines is 5 V and half of that voltage to ground. This is the operating voltage specified for the devices contained in the circuit shown in figure 2. The signaling sense of the voltages appearing across the interconnection cable is defined as follows.

**3.1.1** Terminal A of the driver shall be negative with respect to terminal B for a binary 1 (OFF) state.

**3.1.2** Terminal A of the driver shall be positive with respect to terminal B for a binary 0 (ON) state.

NOTE—Reversing of the cable pair for a particular circuit will cause inversion of the signals.



- $R_t$  = Cable termination resistance
- A,B = Generator interface points
- A',B' = Load interface points
- C = Circuit ground

**Figure 2 – Connections of multiple equipment**

#### 3.2 Driver

The driver has the capability to furnish the signal necessary to supply many parallel receivers. However, for the physical arrangement of multiple equipment throughout a facility it is best to use the method of linking depicted in figure 1.

### 3.3 Communications settings

The interface described in this standard utilizes a serial data bit transmission conforming to EIA-422-A, with one start bit, eight data bits, a parity bit, and one stop bit. The standard data rate used for this interface is 19 200 baud (or bit/s), although other data rates may be used provided that the nonstandard rate can be accommodated by all equipment on the interface.

### 3.4 Interface connections

The circuits used by this interface are listed in table 1 along with the sources (driver end) of the signal and the pin numbers for a nine-pin D-subminiature-type connector.

**Table 1 – Circuits used by interface**

| Symbol | Description         | Source | Terminal |          |
|--------|---------------------|--------|----------|----------|
|        |                     |        | A<br>(–) | B<br>(+) |
| GND    | Protective ground   | —      | 3        | —        |
| TxD    | Transmitted data    | DTE    | 9        | 8        |
| RxD    | Received data       | DCE    | 5        | 4        |
| DTR    | Data terminal ready | DTE    | 7        | 6        |
| DSR    | Data set ready      | DCE    | 2        | 1        |

## 4 Communication

### 4.1 Intelligent devices

The signal characteristics of an intelligent device (programmable element such as a microprocessor or microcontroller) applicable to this standard are shown in figure 3 and the terms defined in table 2. Figure 3 depicts the sequence of events in a typical transmission of data to and/or from a DCE and a DTE. The communication contains certain protocols that were established to be compatible with an intelligent programmable device. The initial conditions and the sequence of events as shown in figure 3 are as follows.

When there is no transmission under way, TxD, RxD, DSR, and DTR are in the OFF state on all equipment, including the DTE. The DTE initiates a transmission by sending an 8-bit equipment address code (EAC) on the TxD circuit.

The DCE unit corresponding to that EAC detects its address and responds by setting DSR to the ON state.

NOTE – If DTR is set, other devices not involved in the conversation must remain in the idle state to avoid conflict.

The DTE waits for DSR to be set to the ON state, indicating that a DCE has decoded the EAC, and then sets DTR to the ON state. The DCE detects the DTR change at its DSR input, and returns 2 bytes of data to the DTE. The first byte is its device-type (DT) code and the second is its manufacturer's identification (ID) code.

After verifying that the DT and ID codes are valid, the DTE transmits the first command to the device.

NOTE—The DCE's interpretation of the command determines the number of bytes (if any) that will follow. Some command codes have been preassigned. Their descriptions, along with examples of their usage, are given in Annex A. All other DCEs connected to the interface must ignore any data received since their address did not match the EAC.

The DTE then transmits the sequence of data bytes to the DCE on the TxD circuit.

NOTE—The type and quantity of device-specific data are defined by the manufacturing organization.