

ANSI/ESD SP5.3.2-2013

ESD Association Standard Practice

***for Electrostatic Discharge
Sensitivity Testing***

***Socketed Device Model (SDM)
Component Level***



*Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440*

*An American National Standard
Approved September 30, 2013*

ANSI/ESD SP5.3.2-2013

Reaffirmation of ANSI/ESD SP5.3.2-2008

***ESD Association Standard Practice
for Electrostatic Discharge Sensitivity Testing –***

***Socketed Device Model (SDM)
Component Level***

Approved June 16, 2013
ESD Association



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(This foreword is not part of ESD Association standard practice ANSI/ESD SP5.3.2-2013)

FOREWORD

This standard practice¹ provides a procedure for generating a "Socketed Device Model" (SDM) test on a component integrated circuit (IC) device. The term SDM was derived from socketed charge device model (S-CDM) test method, which refers to the charged device model (CDM) tests of an IC device mounted in a socket. This is in contrast to the CDM test method, ANSI/ESD S5.3.1, where the IC device is tested while in a dead-bug (or pins facing up) configuration and the package is in intimate contact with a charge plate during the charging process.

In this procedure, the device under test (DUT), socket, test fixture board, HV relays and other parts of the test simulator are charged and discharged during the test. The charge is uniquely stored in a distributive network of parasitic capacitance and inductance elements starting from the high voltage supply, the high voltage and ground relays, the pogo pins, the test fixture board, the socket and the DUT. Consequently, the discharge currents through the pin under test represent the charge stored in the IC device and the SDM test simulator's distributive network. The peak current will vary as the trace length on the test fixture board changes. The discharge waveform is unique for the 32-pin DIP and 512-pin PGA Test Fixture Boards (TFB). **Using a different size TFB will produce different waveform parameters including I_{p1} , t_r , t_d and t_z .**

ESD test equipment designed to meet this standard practice generates repeatable fast transient over damped current discharge waveforms for a given stress voltage. This unique test system provides valuable information regarding the relative ESD sensitivity of an IC device to a sub-nanosecond rise time and high current discharge from the pin of a socketed device to a ground potential.

This SDM standard practice provides guidance for setting up, verifying functionality, and performing SDM testing on components. If the methods defined in this standard practice are followed, then the data collected can be used to compare test results from identically designed and verified SDM test simulators.

At the time of publication, the ESD test equipment used for this standard practice is no longer manufactured. Purchase of this type of test equipment will have to be done on secondary or used equipment markets.

This standard practice was originally designated ANSI/ESD SP5.3.2-2004 and was approved on February 22, 2004. ANSI/ESD SP5.3.2-2008 was a reaffirmation of ANSI/ESD SP5.3.2-2004 and was approved on September 7, 2008. ANSI/ESD SP5.3.2-2013 is a reaffirmation of ANSI/ESD SP5.3.2-2008 and was approved on June 16, 2013. Two editorial changes were made from the 2008 version: a fifth paragraph was added to the foreword and the definition for positive clamp socket was removed from Section 3.0.

¹ **ESD Association Standard Practice (SP):** A procedure for performing one or more operations or functions that may or may not yield a test result. Note, if a test result is obtained it may not be reproducible.

At the time ANSI/ESD SP5.3.2-2013 was prepared, the 5.3.2 Device Testing (SDM) Subcommittee had the following members:

Michael Chaine, Chair Micron Technologies		
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Horst Gieser Fraunhofer EMFT	Vaughn Gross Green Mountain ESD Labs, LLC	Evan Grund Grund Technical Solutions, LLC
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