

ESDA/JEDEC Joint Standard

ANSI/ESDA/JEDEC JS-001-2024

Limited revision of ANSI/ESDA/JEDEC JS-001-2023



*For Electrostatic Discharge
Sensitivity Testing*

*Human Body Model (HBM)
Device Level*

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*An American National Standard
Approved September 17, 2024*

Published October 1, 2024

***ESDA/JEDEC Joint Standard for
Electrostatic Discharge
Sensitivity Testing
Human Body Model (HBM)
Device Level***

Approved

September 12, 2024 by EOS/ESD Association, Inc.

August 12, 2024 by JEDEC Solid State Technology Association



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Published by:
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218 West Court Street
Rome, NY 13440

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Printed in the United States of America
ISBN: 1-58537-351-6

(This foreword is not part of ESDA/JEDEC Joint Standard ESDA/JEDEC JS-001-2024)

FOREWORD

This joint standard was developed under the guidance of the JEDEC JC-14.1 committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The original content for the initial version (2010) was developed by a joint working group composed of members of the JEDEC ESD Task Group and ESDA Working Group 5.1 (Human Body Model). This version of the standard is intended to replace the human body model ESD standard ANSI/ESDA/JEDEC JS-001-2017.

The purpose has been modified to allow testing at package, wafer, or die level with a warning that results may be different.

Definitions have been improved or added to specify better HBM simulator definition and its parts (like terminal, channel, pin), no-connect pins, and exposed pads.

Low parasitic tester definition has been improved, specifying that the possibility of using a low parasitic system depends on the number of channels that meet waveform requirements; this also includes two-channel testers.

Text in several subsections of Section 6.0 has been revised to clarify the “equivalence” of using Table 2A, Table 2B, and pin-pair stressing and to specify that it is required to complete full pin to pin stress on a device having 10 pins or less, but it is allowed to use the same strategy on a device having a higher pin count. A reference for assigning withstand thresholds to a subset of pins has been included in the same section with more detail in Annex B.

The compendium for this document is ESDA/JEDEC JTR001, where legacy JS-001-2017 annexes C and D have been moved and expanded together with suggestions and other practical examples for helping the interpretation of this norm.

Minor changes include modifications in Table 1, Table 2A, and Table 2B, reference to JTR001 where appropriate, annex reordering, and editorial changes in the body and the images.

In this document, the following verbal forms are used:

- “shall” indicates a requirement
- “should” indicates a recommendation
- “may” indicates a permission
- “can” indicates a possibility or a capability

This standard is maintained and revised as a joint standard through a Memorandum of Understanding between JEDEC and ESDA. This standard is a living document. Revisions and updates will be made on a routine basis, driven by the needs of the electronic industry.

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This document was originally designated ANSI/ESDA/JEDEC JS-001-2010 and approved on January 13, 2010. ANSI/ESDA/JEDEC JS-001-2011 was a revision of ANSI/ESDA/JEDEC JS-001-2010 and was approved on March 4, 2011. ANSI/ESDA/JEDEC JS-001-2012 was a revision of ANSI/ESDA/JEDEC JS-001-2011 and was approved on November 16, 2011. ANSI/ESDA/JEDEC JS-001-2014 was a revision of ANSI/ESDA/JEDEC JS-001-2012 and was approved on January 13, 2014. ANSI/ESDA/JEDEC JS-001-2017 is a limited revision of ANSI/ESDA/JEDEC JS-001-2014 and was approved on December 8, 2016. ANSI/ESDA/JEDEC JS-001-2023 was a revision of ANSI/ESDA/JEDEC JS-001-2023 and was approved on February 7, 2023. ANSI/ESDA/JEDEC JS-001-2024 is a limited revision of ANSI/ESDA/JEDEC JS-001-2023 and was approved on September 12, 2024.

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ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Device Level

1.0 SCOPE AND PURPOSE**1.1 Scope**

This standard establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

All packaged semiconductor devices, thin film circuits, acoustic wave devices, optoelectronic devices, hybrid integrated circuits (HICs), discrete, and multi-chip modules (MCMs) containing any of these devices as well as unpackaged singulated bare die, and die which are still part of a wafer are to be evaluated according to this standard.

1.2 Purpose

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

1.3 Equivalency of Wafer or Die Level Results

HBM test results at the wafer or die level are considered valid and equivalent but may differ from testing in a package due to package parasitics, pins tied together in the package, or any other devices included in the package.

2.0 REFERENCED PUBLICATIONS

ESD ADV1.0, ESD Association's Glossary of Terms¹

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices²

ESDA/JEDEC JTR001-xx-xx, User Guide of ANSI/ESDA/JEDEC JS-001 Human Body Model Testing of Integrated Circuits

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms, and JESD99 JEDEC Standard –Terms, Definitions, and Letter Symbols for Microelectronic Devices. Terms separated by a semicolon (;) are considered to be synonyms. In this document, the term “pin” is used to represent any device pin, land, bump, ball, or die pad.

above-passivation layer (APL). A low-impedance metal plane built on the surface of a die above the passivation layer connecting a group of bumps or pins (typically power or ground).

NOTE: This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

associated non-supply pin. A non-supply pin (typically an input, output, or I/O pin) is associated with a supply pin group if either:

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- the current from the supply pin group (for example, VDDIO) is required for the function of an electrical circuit (I/O driver) that connects (high/low impedance) to that non-supply pin; or
- a parasitic path exists between a non-supply and supply pin group (for example, open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

cloned non-supply (IO) pin. Any of a set of input, output, or bidirectional pins using the same IO cell and electrical schematic and sharing the same associated supply pin group(s), including ESD power clamp(s).

coupled non-supply pin pair. Two pins, such as differential amplifier inputs or low-voltage differential signaling (LVDS) pins, having an intended direct current path in between, such as a pass gate or resistor.

NOTE: These pairs include analog and digital differential pairs and other special function pairs (for example, D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN, etc.).

ESD withstand voltage; withstand threshold. The highest voltage level not causing device failure with the device passing all tests performed at lower voltage levels.

NOTE: See note under “failure window” definition.

exposed pad. An exposed metal plate on an IC package.

NOTE: This metal plate may or may not be electrically connected to the die.

NOTE: If the exposed pad supports the die, it might be called a die attach pad or thermal pad (see ESDA/JEDEC JTR001 for further information).

failure window. An intermediate range of stress conditions inducing failure in a particular device type while the device type can pass some higher and lower stress conditions than this range.

NOTE: For example, a device with a failure window may pass a 500-volt test, fail a 1000-volt test, and pass a 2000-volt test. Hence, the failure window of the device is between 500 volts and 2000 volts. The withstand voltage of this device is 500 volts, as this is the highest passing level before the 1kV failure.

feedthrough. A direct or indirect (via a series resistor) connection from a pad cell layout allowing additional elements not included in the pad cell to make electrical connections to the bond pad (see Annex A).

HBM ESD tester; HBM simulator. Equipment that applies a simulated human body model (HBM) ESD stress to a device.

human body model (HBM) ESD. An electrostatic discharge (ESD) event meeting the waveform criteria specified in this standard approximating the discharge from the fingertip of a typical human being to a grounded device.

Ips (peak current value). The current value determined by linear extrapolation of the exponential current decay curve back to the time (t_{max}) when the current actually peaked ($I_{ps_{max}}$).

NOTE: The linear extrapolation should be based on the current waveform data over a 40-nanosecond period beginning at t_{max} (see Figure 2A).

Ips_{max} (peak current maximum value). The highest current value measured.

NOTE: This value includes the overshoot or ringing components due to internal test simulator RLC parasitics (see Figure 2A).

N-channel low parasitic HBM simulator. A simulator with similar in-specification waveforms for both polarities and terminal A/B orientations when performing the procedure in Section 5.2.2 on a pair of pins formed by a single pin and one pin of a pin group with N pins connected to N channels of the tester.

no-connect pin. A package interconnect (pin, bump, or ball) not electrically connected to a die.

NOTE: In practice, some pins are labeled as “no-connect” but are actually connected to the die and, therefore, should not be classified as no-connect pins for ESD testing.

non-socketed tester. An HBM simulator making contact with the device under test (DUT) pins (or balls, lands, bumps, or die pads) with test probes rather than placing the DUT in a socket.

non-supply pin. A pin that is not categorized as a supply pin or a no-connect.

NOTE: Non-supply pins include pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins, and VPP pins on EPROM memory. Most non-supply pins transmit or receive information, such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

package plane. A low-impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground). There may be multiple package planes (sometimes referred to as islands) for each power and ground group.

pin. Any terminal, land, lead, bump, ball, or exposed pad on the package that may make an electrical connection to the die.

pre-pulse voltage. A voltage occurring at the device under test (DUT) immediately prior to the generation of the HBM current pulse (see Annex C.2).

pulse generation circuit. The circuit network that produces a human body discharge current waveform.

NOTE: The circuit network includes a pulse generator with its test equipment internal path up to the contact pad of the test fixture.

NOTE: This circuit is also referred to as a dual-polarity pulse source.

ringing. A high-frequency oscillation superimposed on a waveform.

shorted non-supply pin. Any non-supply pin (typically an input, output, or I/O pin) that is metalically connected (typically < 3 ohms) on the chip or within the package to another non-supply pin (or set of non-supply pins).

socketed tester. A simulator that makes contact with DUT pins (or balls, lands, bumps, or die pads) using a DUT socket mounted on a test fixture board.

specification limit (SPL). The HBM limit value set by customer requirements or internal targets (see Annex A).

spurious current pulse. A small HBM shaped pulse following the main current pulse, typically defined as a percentage of I_{psmax} .

step-stress-test hardening. The process of increasing the ESD withstand threshold by applying stress incrementally from low voltage to higher values.

NOTE: This hardening occurs when a device subjected to increasing ESD voltage step-stresses can withstand higher stress levels than when another device expected to have the same threshold is evaluated using no step-stressing.

NOTE: For example, a device may fail at 1000 volts if subjected to a single stress but fail at 3000 volts if stressed incrementally from 250 volts.

supply pin. Any device pin that provides operating current to that device.

NOTE: Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current reference levels). For ESD testing, power and ground pins are treated as supply pins.

terminal. Output (A) or return (B) of the simulator pulse source.

test fixture board. A specialized circuit board with one or more device sockets connecting the DUT(s) to the HBM simulator.

tester channel. A path connecting the pulse source of the simulator to the DUT pin.

t_{max} . The time when the current is at its maximum value (I_{psmax}) (see Figure 2A).

trailing current pulse. A current pulse that occurs after the HBM current pulse has decayed (see Annex C.1).

NOTE: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

two-channel tester. An HBM simulator that has two tester channels.

V1. The minimum HBM stress voltage step at which at least one of the selected cloned non-supply pins fails (see Annex A).

V2. The estimation of the minimum HBM stress voltage step at which all selected cloned non-supply pins would fail (see Annex A).

VM. The minimum HBM stress voltage step at which 50% or greater of the selected cloned non-supply pins fail (see Annex A).

4.0 APPARATUS AND REQUIRED EQUIPMENT

4.1 Waveform Verification Equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current probe, and high-voltage resistor load. The maximum time between calibrations shall be according to company quality management system requirements.

Equipment capable of verifying the pulse waveforms defined in this standard test method includes but is not limited to, an oscilloscope, evaluation loads, and a current probe.

4.1.1 Oscilloscope

A digital oscilloscope is recommended, but analog oscilloscopes are also permitted. The oscilloscope shall meet the following requirements to ensure accurate current waveform capture:

- Minimum sensitivity of 100 milliamperes per major division when used in conjunction with the current probe specified in Section 4.1.2.
- Minimum bandwidth of 350 MHz.
- Recommended minimum channels: 2
- Vertical accuracy: $\leq 2.5\%$
- Time base accuracy: $\leq 0.01\%$
- For analog scopes, the minimum writing rate of one major division per nanosecond.

4.1.1.1 Additional Requirements for Digital Oscilloscopes

- Minimum sampling rate: 1 GS/s
- Minimum vertical resolution: 8-bit
- Minimum record length: 10 k points

4.1.2 Current Probe

- Minimum bandwidth of 200 MHz
- Minimum peak pulse capability of 8 amperes
- Rise time of less than 1 nanosecond
- Capable of accepting a solid conductor as specified in Section 4.1.3.
- Provides an output voltage per signal current as required in Section 4.1.1.
- Low-frequency 3-dB-point below 10 kHz (for example, Tektronix CT2) for measurement of the decay constant τ_d (see Section 5.2.3.1 and Table 1). Results using a current probe with a low-frequency 3-dB-point of 25 kHz (for example, Tektronix CT1) to measure decay constant τ_d are acceptable if τ_d is found to be between 130 and 170 ns.

NOTE: Decay time of 170 ns is still a valid value but it is strongly suggested to check the equipment.

NOTE: Depending on pre-charge voltage it may be necessary to add an attenuator to keep the signal within the oscilloscope maximum range.

4.1.3 Evaluation Loads

Two evaluation loads are necessary to verify tester functionality:

- Load 1: A solid 18-24 AWG (non-US standard wire size 0.25 to 0.75 mm² cross-section) tinned copper wire (shorting load) as short as practical to span the distance between the two farthest pins in the socket contacted by the probes of a non-socketed tester. The wire should be long enough to pass through the current probe.
- Load 2: 500 ohms, $\pm 1\%$, minimum 4000-volt rating.

NOTE: Care should be used in the selection of the 500-ohm resistor to avoid resistors with high inductance, such as wire wound resistors, or resistors with high parallel capacitance.

4.1.4 Attenuator

Attenuator(s) with a precision of ± 0.5 dB, at least 1-GHz bandwidth, and an impedance of 50 ohms ± 5 ohms.

NOTE: A 20-dB attenuator is usually suitable to cover all ranges.

4.2 Human Body Model Simulator

A simplified schematic of the HBM simulator or tester is given in Figure 1. The performance of the tester is influenced by parasitic capacitance and inductance. Thus, the construction of a tester using this schematic does not guarantee that it will provide the HBM pulse required for this standard. The waveform capture procedures and requirements described in Section 5.0 determine the acceptability of the equipment for use.

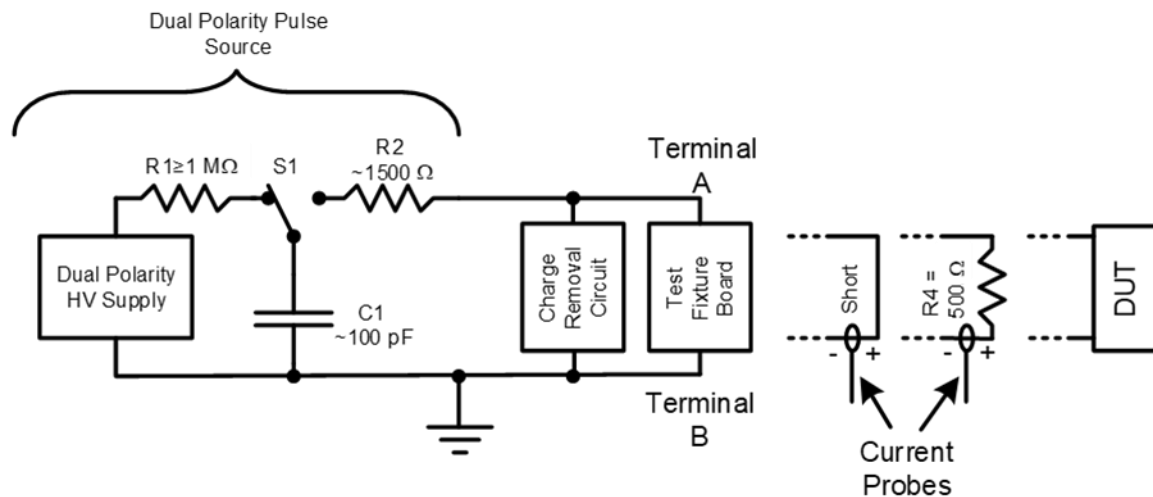


Figure 1: Simplified HBM Simulator Circuit with Loads

NOTES:

1. The current probes are specified in Section 4.1.2.
2. The shorting load (Short) and 500-ohm resistor (R4) are evaluation loads specified in Section 4.1.3.
3. Reversal of Terminals A and B to achieve dual-polarity performance is not permitted except under conditions described in, Sections 6.5.1.3 and 6.7.
4. The charge removal circuit ensures a slow removal of any charges that might remain on the device, thus avoiding the possibility of a charged device model discharge. A simple example is a 10-kilohm or larger resistor (possibly in series with a switch) in parallel with the test fixture board. This resistor may also be useful to control parasitic pre-pulse voltages (see Annex C.2 and Annex C.3).
If a switch is used to activate the charge removal circuit, it should be activated after the end of the HBM pulse, unless it is also being used to control pre-pulse voltages. In this case, it will be connected prior to the HBM pulse and remain connected until the stress cycle is completed. Additional charge removal circuits may also be used to remove any unwanted charge through other not previously grounded pins on the device under test.
5. The dual polarity pulse source (generator) shall be designed to avoid recharge transients and double pulses.
6. Stacking of DUT socket adapters (piggybacking or the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard defined in Table 1.
7. Values in this figure are nominal.

4.2.1 HBM Test Equipment Parasitic Properties

Some HBM simulators have been found to incorrectly classify HBM sensitivity levels due to parasitic artifacts or uncontrolled voltages unintentionally built into the HBM simulator's environment. Annex C describes methods for determining if these effects are present and optional mitigation techniques. See Annex C.5 for a procedure to determine if an HBM simulator is considered an N-channel low-parasitic HBM simulator for a device with N pins simultaneously connected to the simulator.

5.0 STRESS TEST EQUIPMENT QUALIFICATION AND ROUTINE VERIFICATION

5.1 Overview of Required HBM Tester Evaluations

The HBM tester and test fixture boards shall be qualified, re-qualified, and periodically verified as described in this section. A flow chart for this procedure is given in Annex D. The safety precautions described in Section 5.8 should be followed at all times.

5.2 Measurement Procedures

5.2.1 Reference Pin Pair Determination

The two pins of each socket on a test fixture board that make up the reference pin pair are:

1. The socket pin with the shortest wiring path of the test fixture to the pulse generation circuit (Terminal B).
2. The socket pin with the longest wiring path of the test fixture from the pulse generation circuit (Terminal A) to the ESD stress socket (see Figure 1).

This information is typically provided by the equipment or test fixture board manufacturer. If more than one pulse generation circuit is connected to a socket, there will be more than one reference pin pair.

It is strongly recommended that on non-positive clamp fixtures, feed through test point pads be added on these paths to connect either the shorting load or 500-ohm load resistor during waveform verification measurements. These test points should be added as close as possible to the socket(s), and if the test fixture board uses more than one pulse generator, multiple feed through test points should be added for each pulse generator's longest and shortest paths.

NOTE: A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting load to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

5.2.2 Waveform Capture with Current Probe

To capture a current waveform between two socket pins (usually the reference pin pair), use the shorting load (see Section 4.1.3, Load 1) for the short-circuit measurement or the 500-ohm resistor (see Section 4.1.3, Load 2) for the 500-ohm current measurement and the current probe (see Section 4.1.2).

NOTE: At high stress voltages, an attenuator (see Section 4.1.4) may be necessary to prevent off-scale measurements on the oscilloscope and avoid oscilloscope damage. At low stress levels, especially at the 50-volt and 125-volt levels, an attenuator should not be used when signal levels reach the lower limits of the oscilloscope voltage sensitivity.

5.2.2.1 Short-Circuit Current Waveform

Place the current probe around the shorting load, as close to Terminal B as practical, observing the polarity shown in Figure 1. Attach the shorting load between the pins to be measured, with the current probe as close to Terminal B as practical, observing the polarity shown in Figure 1. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification, or periodic verification.

- a. For positive clamp sockets, insert the shorting load between the socket pins connected to Terminals A and B and hold it in place by closing the clamp.

- b. For non-positive clamp sockets, attach the shorting load between the socket pins connected to Terminals A and B. If it is not possible to make contact within the socket, connect the shorting load between the reference pin pair feed through test points, if available.

NOTE: The socket design is important as some socket types may include contact springs (coils) in their design. These springs can add more parasitic inductance to the signal path and may affect the HBM waveform. Selecting sockets that minimize the use of springs (coils) is recommended, but if this is not possible, then keeping their length as short as possible is recommended.

- c. For non-socketed testers, the shorting load with the inductive current probe is placed on an insulating surface, and the simulator Terminal A and Terminal B probes are placed on the ends of the wires.

5.2.2.2 500-Ohm Load Current Waveform

Place the current probe around the 500-ohm resistor's lead, observing the polarity shown in Figure 1. Attach the 500-ohm resistor between the pins to be measured with the current probe as close to Terminal B as practical. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification, or periodic verification.

- a. For socketed testers, follow procedures according to socket type as described in Section 5.2.2.1.
- b. For non-socketed testers, place the test load and current probe on an insulating surface and connect the tester's probes to the ends of the test load.

5.2.3 Determination of Waveform Parameters

The captured waveforms are used to determine the parameter values listed in Table 1.

5.2.3.1 Short-Circuit Waveform

Typical short-circuit waveforms are shown in Figures 2A, 2B, and 4. The parameters I_{ps} (peak current), t_r (pulse rise time), t_d (pulse decay time), and I_R (ringing) are determined from these waveforms. Ringing may prevent the simple determination of I_{ps} . A graphical technique for determining I_{ps} and I_R is described in Section 5.2.3.3 and Figure 4. The negative reciprocal of the exponent of e , from an exponential fit to the decaying region after any oscillations may also be used to determine t_d as described in Section 5.2.3.4.

5.2.3.2 500-Ohm Load Waveform

A typical 500-ohm load waveform is shown in Figure 3. The parameters I_{pr} (peak current with 500-ohm load) and t_{rr} (pulse rise time with 500-ohm load) are determined from this waveform.

5.2.3.3 Graphical Determination of I_{ps} and I_R (see Figure 4)

5.2.3.3.1 A line is drawn (manually or using numerical methods such as least squares) through the HBM ringing waveform from t_{max} to $t_{max} + 40$ ns to interpolate the value of the curve for a more accurate derivation of the peak current value (I_{ps}). t_{max} is the time when $I_{ps_{max}}$ occurs (see definition for t_{max} in Section 3 and Figure 2A).

5.2.3.3.2 The maximum deviation of the measured current above the straight-line fit is Ring1. The maximum deviation of the measured current below the straight-line fit is Ring2. The maximum ringing current during a short-circuit waveform measurement is defined as:

$$I_R = |Ring1| + |Ring2|$$