

Australian Standard® 2547.2.2—1986

SEMICONDUCTOR DEVICES Part 2.2—INTEGRATED CIRCUITS— DIGITAL



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AUSTRALIAN STANDARD

**SEMICONDUCTOR DEVICES—
Part 2.2
INTEGRATED CIRCUITS—
DIGITAL**

AS 2547.2.2—1986

First published 1986

See also Preface



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PREFACE

This standard was prepared by the Association's Committee on Semiconductors and Devices. It is reproduced from IEC 748.2:1985 and is one of the standards prepared by IEC/TC 47, Semiconductor Devices.

This standard is one of a series of standards published under the generic specification AS 2547. This standard supersedes:

- the existing AS 2547 series (published in 1982 and 1983 and identical with equivalent parts of IEC 147 published between 1966 and 1981);
- AS C366, Part 4—1978 and Part 5—1978 (equivalent to IEC 147-5 and IEC 147-5A);
- AS C367 (endorsement of IEC 148—1969);
- AS 1967 (identical to IEC 147-ID and IE).

The purpose of IEC 747 is to reorganize the material originally presented in the IEC 147* series and IEC 148†, on semiconductor devices and letter symbols representing them, into one device-oriented publication. This is now republished as follows:

- (a) Specific requirements for integrated circuits—now IEC 748.
- (b) Mechanical and climatic test methods—now IEC 749.

It was in view of the above reorganization that Committee TE/12 agreed to integrate the entire series into one series of Australian standards using the generic designation AS 2547. The relationship with the three IEC standards is as follows:

- (i) Part 1.1 onwards—identical with the IEC 747 series.
- (ii) Part 2.1 onwards—identical with the IEC 748 series.
- (iii) Part 3.1—identical with IEC 749.

For the purpose of this Australian standard and all other standards in this AS 2547 series, the text of the reproduced IEC Publications should be modified as follows:

- A. *Terminology.* The words 'Australian Standard' should replace the words 'IEC Publication' wherever they appear.
- B. *Cross-references.* The reference to IEC Publications should be replaced by references to the appropriate Australian Standards as follows:

<i>Reference to IEC Publications</i>		<i>Appropriate Australian Standard</i>	
IEC 27	Letter symbols to be used in electrical technology	AS 1046	Letter Symbols for Use in Electrotechnology
IEC 50	International Electro-technical Vocabulary	AS 1852	International Electro-technical Vocabulary
IEC 191	Mechanical standardization of semiconductor devices	AS C379	Mechanical Standardization of Semiconductor Devices
IEC 319	Presentation of reliability data on electronic components	AS 2350	Presentation of Reliability Data on Electronic and Similar Components
IEC 747	Semiconductor devices. Discrete devices and integrated circuits	AS 2547	Semiconductor Devices
747.1	Part 1—General	1.1	Discrete Devices—General
747.2	Part 2—Rectifier diodes	1.2	Discrete Devices—Rectifier Diodes
747.3	Signal (including switching) and regulator diodes	1.3	Discrete Devices—Signal (Including Switching) and Regulator Diodes
747.4	R.F. Diodes	1.4	Discrete Devices—R.F. Diodes
747.5	Optoelectronic devices	1.5	Discrete Devices—Optoelectronic Devices

* IEC 147, Essential ratings and characteristics of semiconductor devices and general principles of measuring methods.

† IEC 148, Letter symbols for semiconductor devices and integrated microcircuits.

747.6	Thyristors	1.6	Discrete Devices—Thyristors
747.7	Bipolar transistors	1.7	Discrete Devices—Bipolar Transistors
747.8	Field-effect transistors	1.8	Discrete Devices—Field-effect Transistors
747.9	Miscellaneous devices	1.9	Discrete Devices—Miscellaneous Devices
747.10	Generic specification for discrete devices and integrated circuits (QC 700 000)	1.10	Generic Specification for Discrete Devices and Integrated Circuits (QC 700 000)
747.11	Sectional specification for discrete devices (QC 750 000)	1.11	Sectional Specification for Discrete Devices (QC 750 000)
IEC 748	Semiconductor Devices. Integrated circuits	AS 2547	Semiconductor Devices
748.1	General	2.1	Integrated Circuits—General
748.2	Digital integrated circuits	2.2	Integrated Circuits—Digital
748.3	Analogue integrated circuits	2.3	Integrated Circuits—Analogue
748.4	Interface integrated circuits	2.4	Integrated Circuits—Interface
IEC 749	Semiconductor devices. Mechanical and climatic test methods	3.1	Mechanical and Climatic Test Methods

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1		Reference to 748-1, VIII, Three, 2 (which is 147-4, II, Two, art. 4)
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STANDARDS ASSOCIATION OF AUSTRALIA

Australian Standard
for
SEMICONDUCTOR DEVICES

PART 2.2—INTEGRATED CIRCUITS—DIGITAL

CHAPTER I: GENERAL

1. Introductory note

As a rule, it will be necessary to use Publications 747-1 and 748-1 together with the present publication.

In Publications 747-1 and 748-1, the user will find all basic information on:

- terminology;
- letter symbols;
- essential ratings and characteristics;
- measuring methods;
- acceptance and reliability.

2. Scope

The present publication gives standards for the following categories or sub-categories of devices:

- Combinatorial and sequential digital circuits.
- Integrated circuit memories.
- Integrated circuit microprocessors.
- Charge-transfer devices.

CHAPTER II: TERMINOLOGY AND LETTER SYMBOLS

1. Terminology for combinatorial and sequential integrated circuits

1.1 General terms

Explanatory note

A signal is a physical representation of information. A digital signal is the time-dependent behaviour or variation of a physical quantity with a finite number of non-overlapping ranges of values. A digital signal can be used for transmission of information or for information processing. Taking into account common practice, simplified definitions have been chosen below. Referring to digital circuits, this will generally produce no ambiguity or misunderstanding.

1.1.1 Digital signal

The variation with time of a physical quantity, having a finite number of non-overlapping ranges of values, that is used for transmission or the processing of information.

Notes 1. — The physical quantity may be voltage, or current, or impedance, etc.

2. — For convenience, each range of values can be represented by a single value, e.g. the nominal value.

1.1.2 Binary signal

A digital signal with only two possible ranges of values.

Note. — For convenience, each range of values can be represented by a single value, e.g. the nominal value.

1.1.3 Low range (of a binary signal)

The range of least positive (most negative) levels of a binary signal.

Note. — This range is often denoted by "L-range" and any level in the range by "L-level".

1.1.4 High range (of a binary signal)

The range of most positive (least negative) levels of a binary signal.

Note. — This range is often denoted by "H-range" and any level in the range by "H-level".

1.1.5 Input terminal

A terminal by means of which an applied signal may modify the output configuration (output pattern) of the circuit:

- either directly;
- or indirectly by modifying the ways in which the circuit reacts to signals at other terminals.

1.1.6 Three-state output

An output of a binary circuit that is a relatively low-impedance source or sink at the high and low levels and, in addition, under appropriate input conditions, provides a high-impedance state approaching an open-circuit.

Note. — In function tables and function (sequential) matrices, the abbreviation Z should be used for the high-impedance state.

1.2 Terms related to functions

1.2.1 Input configuration (input pattern) (of a binary circuit)

A combination of the L-levels and H-levels at the input terminals at a given instant.

1.2.2 Output configuration (output pattern) (of a binary circuit)

A combination of the L-levels and H-levels at the output terminals at a given instant.

Note. — When there is no possibility of ambiguity, the output configuration (output pattern) may be represented by the level (expressed as L-level or H-level) of the signal at a stated output terminal of the circuit (the reference output terminal).

1.2.3 Function table

A representation of the necessary or possible relations between the values of the digital signals at the inputs and the outputs of a digital circuit, these values of the digital signals being indicated either by using electrical values directly or by stating the electrical significance of the symbols (e.g., L and H for binary circuits).

Generally:

- every column indicates the values of the digital signals at an input or at an output of the digital circuit;
- every line indicates the combination of values of the digital signals at the input(s) and the resulting values of the digital signals at the output(s);
- whenever the value of the digital signal at an output is not determined, it should be indicated by a question mark;
- whenever the value of a digital signal at an input has no influence, it should be indicated by the symbol L/H or X.

1.2.4 Truth table (for a relation between digital variables)

A representation of the logic relationship between one or more independent digital variables and one or more dependent digital variables, by means of a table which, for each possible combination of the values of the independent variables, gives the appropriate values of the dependent variables.

Note. — The distinction between “function table” and “truth table” is fundamentally necessary, because the same digital circuit may fulfil several different logic operations, according to the arbitrary choice of the assignment of the values of the digital variables to the values of the digital electrical quantities.

1.2.5 Excitation

An input configuration (input pattern), or change in input configuration (input pattern), that can:

- cause the circuit to change its output configuration (output pattern), either directly, or in conjunction with an already existing state of preparedness;
- or put the circuit in a state of preparedness;
- or either cancel or modify an already existing state of preparedness.

Notes 1. — The repetition, or reiteration, of a given excitation will not necessarily produce the same effect.

2. — In some cases, an excitation can also maintain an output configuration (output pattern) which it could have produced.

1.2.6 Active level (of a digital input signal to a sequential circuit)

A level of a digital input signal which can produce excitation.

1.2.7 *Active transition (of a digital input signal to a sequential circuit)*

A transition from one level of a digital input signal to another level, which can produce excitation.

Note. — An active transition may also be subject to limitations arising from the slope of the signal.

1.2.8 *Stable output configuration (output pattern) (of a sequential circuit)*

An output configuration (output pattern), in which the circuit will remain after the excitation that produced it, or any other that could have maintained it, has been replaced by an input configuration (input pattern) which is not an excitation,

or:

an output configuration (output pattern) which the circuit takes up in the absence of excitation.

Note. — Any short persistence of the output configuration (output pattern) due to undesired effects such as capacitance, storage and propagation times, etc., is ignored.

1.2.9 *Pseudo-stable output configuration (output pattern) (of a sequential circuit)*

An output configuration (output pattern) which does not persist after the excitation that produced it, or other excitations that have maintained it, have been replaced by an input configuration (input pattern) which is not an excitation.

Note. — Any short persistence of the output configuration (output pattern) due to undesired effects such as capacitance, storage and propagation times, etc., is ignored.

1.2.10 *Meta-stable output configuration (output pattern) (of a sequential circuit)*

An output configuration (output pattern) which persists, for a limited duration only, after the appropriate excitation has been applied.

Notes 1. — The duration of the meta-stable output configuration (output pattern) will depend on the design of the circuit, may depend on the duration of the excitation that produced it and may be affected by further excitation.

2. — Any short persistence of the output configuration (output pattern) due to undesired effects such as capacitance, storage and propagation times, etc., is ignored.

1.2.11 *Function (sequential) matrix*

A table having several inputs which gives the possible output configurations for each input configuration(s) and from which the output configuration(s) resulting from a transition from each individual input configuration to any other input configuration can be read directly.

Note. — Where appropriate, a function (sequential) matrix may be completed by additional data or details concerning time conditions (e.g., transition times for the input levels, delay time, duration of the input configuration to produce a desired new output configuration).

1.2.12 *Preparatory input terminal*

An input terminal through which an applied digital signal can modify the manner in which the circuit reacts to signals at other input terminals, without directly causing a change of the output configuration (output pattern) of the circuit.

1.2.13 *Enable input*

An input that when active permits one or more specific operations to be commenced.

Notes 1. — An “enable” signal may either:

- a) permit one or more operations to be performed while the signal is maintained at a specified level, or
- b) operate a latch that will allow an operation to continue even after the “enable” signal has been removed.

2. — “Enable” is a generic term. It may be qualified by suitable descriptive adjectives as required.

1.2.14 *Chip-enable input*

An enable input that when inactive causes the integrated circuit to be in a reduced-power stand-by mode.

1.2.15 *Chip-select input*

An enable input that when inactive prevents both input and output of data to and from the integrated circuit.

1.2.16 *Output enable input*

An enable input that when inactive prevents the output of data from the integrated circuit.

Note. — When not enabled, the outputs will assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

1.2.17 *Write-enable input*

An input that when active permits data to be entered into a memory for storage.

1.2.18 *Disable input; inhibit input*

An input that when active prevents one or more specific operations from being performed.

Note 1. — These are alternative names for an enable input emphasizing the complementary or negative aspect.

- 2. — When inactive, an enable input disables or prevents the operations that it would permit if active. Conversely, when inactive, a disable input permits the operation(s) to be performed that it would prevent if active.

1.2.19 *Level-operated input*

An input that continues to be active (to cause excitation) as long as it remains at an active level.

1.2.20 *Transition-operated input*

An input that is active (causes excitation) only on one of the two directions of transition or an input that causes excitation only if the rate of change from one level to another is sufficiently large.

1.2.21 *Set*

- (1) (ISO) To cause a counter to take the state corresponding to a specified number.
- (2) (ISO) To place a storage device into a specified state, usually other than that denoting zero.

Note. — Contrast with “reset”.

1.2.22 *Reset*

- (1) (ISO) To cause a counter to take the state corresponding to a specified initial number.
- (2) (ISO) To restore a storage device to a prescribed initial state, not necessarily that denoting zero.

Note. — Contrast with “set”.

1.3 *Types of circuits*

1.3.1 *Digital circuit*

A circuit which is designed to operate by means of digital signals at the input(s) and at the output(s).

Notes 1. — In this definition, it is understood that “inputs” and “outputs” exclude static power supplies.

2. — In some digital circuits, e.g. certain types of astable circuits, the input(s) need not exist.

1.3.2 *Binary circuit*

A digital circuit designed to operate with binary signals.

Note. — The pairs of ranges of values of the binary signals may be different at different terminals.

1.3.3 *Combinatorial (digital) circuit*

A digital circuit in which there exists one, and only one, combination of the digital signals at the outputs for each possible combination of digital signals at the inputs.

1.3.4 *Sequential (digital) circuit*

A digital circuit in which there exists at least one combination of the digital signals at the inputs for which there is more than one corresponding combination of the digital signals at the outputs.

Note. — These combinations at the outputs are determined by previous history (as a result of internal memory, delay, etc.).

1.3.5 *Elementary combinatorial circuit*

A binary combinatorial (digital) circuit which has only one output terminal, and in which the output signal accepts the value occurring only once in the function if, and only if, the signals applied to all the input terminals are either all in the H-range or all in the L-range.

Notes 1. — Because the output signal value (occurring only once in the function table) can lie either in the H-range or in the L-range, there are four types of elementary combinatorial circuits. According to the assignment of the signal values L and H to the binary values 0 and 1 of Boolean algebra, the following logic operations can be realized by means of the four types of elementary combinatorial circuits: AND, OR, NAND, NOR.

2. — Non-elementary combinatorial circuits can be formed by combining elementary combinatorial circuits or by combining elementary combinatorial circuits with inverters.

1.3.6 *Bistable circuit*

A sequential circuit which has two, and only two, stable output configurations (output patterns).

Notes 1. — This broad classification can be divided into sub-classes according to the numbers and kinds of pseudo-stable and meta-stable output configurations (output patterns) available and the number of applications of appropriate excitations required to change from one stable output configuration (output pattern) to the other.

2. — A stable output configuration (output pattern) of a bistable circuit can be expressed by the L-level or the H-level of the reference output terminal.
3. — The term "bistable circuit" is used as a generic term to cover the whole range of sequential circuits with two, and only two, stable output configurations.
It may be used by itself for any kind or class of bistable circuits, when such use does not result in ambiguity or misunderstanding. In particular, the abbreviated term "bistable circuit" is often used for the single excitation bistable circuits.

1.3.6.1 *Edge-triggered (transition-operated) bistable circuit*

A bistable circuit having one or more transition-operated inputs.

1.3.6.2 *Pulse-triggered bistable circuit*

A bistable circuit requiring that a signal at a preparatory input be set up with respect to a first transition of a signal at a triggering input and be held with respect to a second transition occurring at the same triggering input and possibly causing the outputs to change state.

Note. — This definition does not preclude the possibilities that minimum set-up and/or hold times may be negative.

1.3.6.3 *Data-lock-out bistable circuit*

A bistable circuit requiring that the signals at the preparatory inputs be set up and held with respect to that transition of the triggering-input signal that does not cause the outputs to change state.

1.3.7 *Monostable circuit*

A sequential circuit which has only one stable output configuration (output pattern).

- Notes 1.* — The definition above is given in its most general form. In present usage, the term "monostable circuit" implies that there is at least one meta-stable output configuration (output pattern) in addition to the stable output configuration (output pattern).
2. — In general, such circuits may have one or more meta-stable and/or pseudo-stable output configurations (output patterns).

1.3.8 *Expander circuit*

An auxiliary circuit which can be used to expand the number of inputs of equal influence of an associated circuit without modifying the function of the associated circuit.

1.3.9 *Binary inverter*

Binary circuit which has only one input terminal and one output terminal, and in which a signal value L (H) at the input produces a signal value H (L) at the output.

1.3.10 *Master-slave arrangement*

An arrangement of two bistable circuits such that one of them, called the "slave", reproduces the output configuration of the other circuit, called the "master". The transfer of information from the master to the slave is produced by means of an appropriate signal.

1.3.11 *Register*

An arrangement of bistable circuits by means of which information may be accepted, stored, and retrieved.

Note. — The register may form part of another memory and is of a specified capacity.

1.3.12 *Shift register*

A register that, by means of an appropriate control signal, can transfer information between consecutive bistable circuits with the sequence being preserved.

1.3.13 *Counter*

A sequential circuit for storing numbers that permits such numbers to be incremented or decremented by a defined constant, including unity.

1.3.14 *Digital decoder (integrated circuit)*

An arrangement of logic elements (or the equivalent) that selects one or more output channels according to the combination of input signals present.

1.3.15 *Programmable logic array (PLA)*

An integrated circuit consisting of an array of combinatorial logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions.

Note. — The PLA is typically a large set of AND gates driving several OR gates.

1.4 *Terms related to ratings and characteristics*

1.4.1 *(Input) threshold voltage*

The input voltage level that, when crossed, enables an output to change its logic state.

Note. — The term hysteresis, often used in data sheets, denotes the difference between the positive-going and negative-going threshold voltages.

$$V_{\text{hys}} = V_{\text{IT+}} - V_{\text{IT-}}$$

$$\text{or: } V_{\text{hys}} = V_{\text{ITP}} - V_{\text{ITN}}$$

1.4.1.1 *Positive-going (input) threshold voltage $V_{\text{IT+}}$, V_{ITP}*

The input threshold voltage when the input voltage is rising.

Note. — See Note to Sub-clause 1.4.1.

1.4.1.2 *Negative-going (input) threshold voltage $V_{\text{IT-}}$, V_{ITN}*

The input threshold voltage when the input voltage is falling.

Note. — See Note to Sub-clause 1.4.1.

1.4.2 *Input loading factor (of a bipolar digital circuit)*

A factor which indicates the ratio of the input current of a specified input terminal of a digital circuit to the input current of a particular circuit which is chosen as a reference load.

Note. — The reference load should preferably be chosen in such a way that the input loading factor becomes an integer.

1.4.3 *Output loading capability (of a bipolar digital circuit)*

A factor which indicates the ratio of the maximum output current of a specified output terminal of a digital circuit to the input current of a particular circuit which is chosen as a reference load.

Note. — The reference load should preferably be chosen in such a way that the output loading capability becomes an integer.

1.4.4 Set-up time

The time interval between application of a signal that is maintained at a specified input terminal and a specified subsequent active transition at another input terminal.

- Notes 1.* — The set-up time is measured between the instants at which the magnitudes of the two signals pass through specified values within the transition of the signal levels.
2. — The set-up time is the actual time between two signals and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
3. — The set-up time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which interval correct operation of the digital circuit is guaranteed.

1.4.5 Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

- Notes 1.* — The hold time is measured between the instants at which the magnitudes of the two signals pass through specified values within the transition of the signal levels.
2. — The hold time is the actual time between two signals and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
3. — The hold time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which interval correct operation of the digital circuit is guaranteed.

1.4.6 Resolution time

The time interval between the cessation of one input pulse and the commencement of the next input pulse applied to the same input terminal.

- Notes 1.* — The resolution time is measured between the instants at which the magnitude of the input signal passes through specified values within the transition of the signal levels.
2. — The resolution time is the actual time between two pulses and may be insufficient to ensure that both pulses are recognized. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

1.4.7 High-level to low-level (low-level to high-level) propagation time

The time interval between specified reference points on the input and on the output pulses, when the output is going to the low-(high-)level and when the device is driven and loaded by typical devices of stated types.

- Notes 1.* — In some circumstances, the driving and the loading circuits may be replaced for test purposes by equivalent networks which must be specified.
2. — The mean value between the upper limit of the input low range and the lower limit of the input high range is generally used as the specified reference level.

1.4.8 High-level to low-level (low-level to high-level) transition time

The time interval between specified reference points on the edge of the output pulse when the output is going to the low-(high-)level and when a specified input signal is applied through a specified network and the output is loaded by another specified network.

1.4.9 Enable time

The time interval from a specified point on the transition of the enabling signal to a specified point on an output waveform that represents the commencement of the intended operation.

1.4.10 Disable time

The time interval from a specified point on the transition of the disabling signal to a specified point on an output waveform that represents the cessation of the affected operation.

1.4.11 Output enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

1.4.12 Output disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

1.4.13 Pulse duration (width)

The time interval between the specified reference points on the two transitions of the pulse waveform.

1.4.14 Valid time

The time interval during which an output signal is valid or during which an input signal must be valid.

1.4.15 Output data-valid time

The time interval during which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

1.4.16 Equivalent input (output) capacitance (of a binary circuit)

The capacitance of a discrete capacitor that causes the same effect on the waveform of a digital signal as the capacitive component of the input (output) impedance of a binary circuit.

2. Examples**2.1 Elementary combinatorial circuits****2.1.1 Types of elementary combinatorial circuits and their function tables****a) L-AND, H-OR circuit**

Inputs	Output
A B C	Q
L L L.... L	L
All combinations with H	H

b) L-NAND, H-NOR circuit

Inputs	Output
A B C	Q
L L L.... L.....	H
All combinations with H	L

c) H-AND, L-OR circuit

Inputs	Output
A B C	Q
H H H.... H.....	H
All combinations with L.....	L

d) H-NAND, L-NOR circuit)

Inputs	Output
A B C	Q
H H H.... H.....	L
All combinations with L.....	H

e) Binary inverter

Input	Output
L	H
H	L

2.1.2 Realization of logic operations by means of elementary combinatorial circuits

(for two possible assignments of the signal values L and H to the binary values 0 and 1 of Boolean algebra)

Circuit		Assignment	
Type	Name	L ≐ 1 H ≐ 0	L ≐ 0 H ≐ 1
a	L-AND, H-OR	AND	OR
b	L-NAND, H-NOR	NAND	NOR
c	L-OR, H-AND	OR	AND
d	L-NOR, H-NAND	NOR	NAND

2.2 *Principle of characterizing bistable circuits and related sequential digital circuits, shown by examples using letter designations*

Foreword

Two different ways of presenting the (sequential) function matrices are quoted.

2.2.1 *Preamble*

2.2.1.1 If the signal applied to the input terminal concerned is:

- active when it is at the H-level,
 - or active during the transition from the L-level to the H-level,
- then the letter which represents the input is used without a bar.

Examples: R, S, J...

If the signal applied to the input terminal concerned is:

- active when it is at the L-level (i.e. NOT AT THE H-LEVEL),
 - or active during the transition from the H-level to the L-level (i.e. NOT DURING THE TRANSITION FROM THE L-LEVEL TO THE H-LEVEL),
- then the letter which represents the input is used with a bar.

Examples: $\bar{R}$, $\bar{S}$, $\bar{J}$...

In cases of level/transition-operated circuits where the above gives rise to contrary indications, priority is given to the transition.

2.2.1.2 The output terminals of a bistable circuit are denoted by Q and Q*, where Q is the reference-output terminal.

2.2.1.3 Normally, in the two stable output configurations (output patterns) of a bistable circuit, the levels at the terminals Q and Q* are complementary.

The pseudo-stable output configuration (output pattern) is stated by the letters H or L or combinations thereof, to be put in brackets following the letters RS, when it occurs.

If, in the pseudo-stable output configuration (output pattern), the levels at Q and Q* are complementary, both the letters H and L are used, the first letter designating the level at Q.

If, in the pseudo-stable output configuration (output pattern), the levels at Q and Q* are the same, only one letter is used to designate these levels.

Examples: RS(H), RS(L), RS(HL), RS(LH).

If not required, the brackets and letters between them can be omitted.

2.2.1.4 All other types of RS, R_GS_G, JK, J_TK_T circuits, etc., can be described in a manner analogous to the examples that follow.

2.2.2 *Circuits*

2.2.2.1 *RS (L) circuit*

A circuit having two level-operated input terminals R and S. Either input signal can be active in the H-level only.

The input configuration (input pattern) $(R, S) = (L, H)$ produces the output configuration (output pattern) $(Q, Q^*) = (H, L)$. The return of the input signal at the S terminal to the L-level produces no action.

The input configuration (input pattern) $(R, S) = (H, L)$ produces the output configuration (output pattern) $(Q, Q^*) = (L, H)$. The return of the input signal at the R terminal to the L-level produces no action.

The input configuration (input pattern) $(R, S) = (H, H)$ produces the pseudo-stable output configuration (output pattern) $(Q, Q^*) = (L, L)$. The simultaneous return of both input signals from the H-level to the L-level produces a non-foreseeable stable output configuration (output pattern).

Note. — In some cases, the input configuration (input pattern) $(R, S) = (H, H)$ may not be permitted due to technical reasons.

Function (sequential) matrices:

R	L		H			
S	L	H	L	H	L	H
	①	①	3	2	H	L
	②	1	3	②	L	H
	?	1	③	2	L	L

R	L		H			
S	L	H	L	H	L	H
					H	L
					L	H
	?				L	L

Timing diagram:

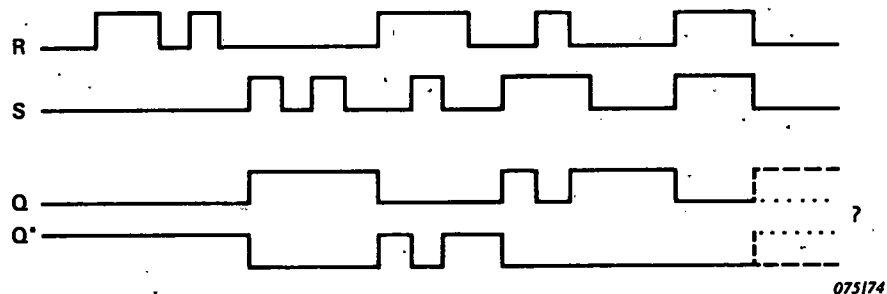


FIGURE 1

2.2.2.2 $\bar{R}\bar{S}$ (H) circuit

A circuit having two level-operated input terminals $\bar{R}$ and $\bar{S}$. Either input signal can be active in the L-level only.

The input configuration (input pattern) $(\bar{R}, \bar{S}) = (H, L)$ produces the output configuration (output pattern) $(Q, Q^*) = (H, L)$. The return of the input signal at the S terminal to the H-level produces no action.

The input configuration (input pattern) $(\bar{R}, \bar{S}) = (L, H)$ produces the output configuration (output pattern) $(Q, Q^*) = (L, H)$. The return of the input signal at the R terminal to the H-level produces no action.

The input configuration (input pattern) $(\bar{R}, \bar{S}) = (L, L)$ produces the pseudo-stable output configuration (output pattern) $(Q, Q^*) = (H, H)$. The simultaneous return of both input signals from the L-level to the H-level produces a non-foreseeable stable output configuration (output pattern).

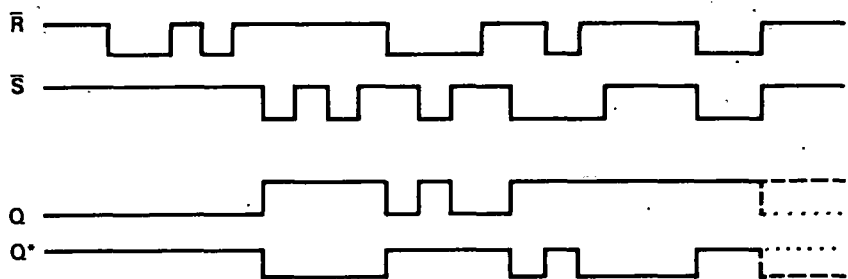
Note. — In some cases, the input configuration (input pattern) $(\bar{R}, \bar{S}) = (L, L)$ may not be permitted due to technical reasons.

Function (sequential) matrices:

$\bar{R}$	L		H			
$\bar{S}$	L	H	L	L	Q	Q*
	3	2	①	①	H	L
	3	②	②	1	L	H
	③	2	?	1	H	H

$\bar{R}$	L		H			
$\bar{S}$	L	H	L	L	Q	Q*
					H	L
					L	H
					H	H

Timing diagram:



076174

FIGURE 2

2.2.2.3 T circuit

A circuit having one input terminal, T, which is transition-operated.

When the signal applied to the input terminal changes from the L-level to the H-level, it produces change-over of the output configuration (output pattern).

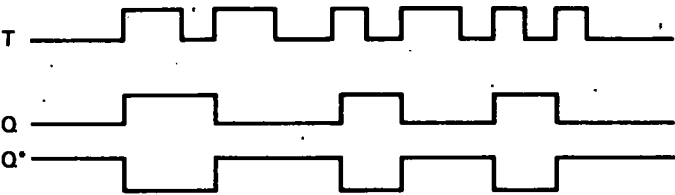
The return of the input signal from the H-level to the L-level produces no action.

Function (sequential) matrices:

T	L	H	Q	Q*
	①	2	L	H
	3	②	H	L
	③	4	H	L
	1	④	L	H

T	L	H	Q	Q*
			L	H
			H	L
			H	L
			L	H

Timing diagram:



077174

FIGURE 3

2.2.2.4 $\bar{T}$ circuit

A circuit having one input terminal, $\bar{T}$, which is transition-operated.

When the signal applied to the input terminal $\bar{T}$ changes from the H-level to the L-level, it produces change-over of the output configuration (output pattern).

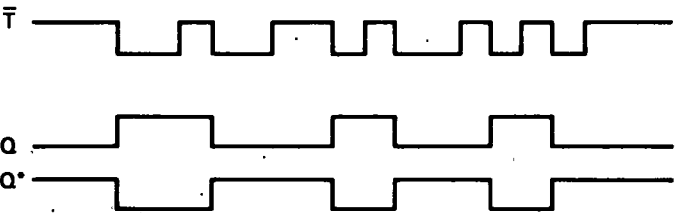
The return of the input signal from the L-level to the H-level produces no action.

Function (sequential) matrices:

$\bar{T}$	L	H	Q	Q*
	2	①	L	H
	②	3	H	L
	4	③	H	L
	④	1	L	H

$\bar{T}$	L	H	Q	Q*
			L	H
			H	L
			H	L
			L	H

Timing diagram:



078174

FIGURE 4

2.2.2.5 General T_G circuit

A circuit having one transition-operated input terminal, T, and one level-operated input terminal, G.

While the G input signal has the H-level, the circuit functions like a T circuit.

While the G input signal has the L-level, the T input signal has no effect on the output configuration (output pattern).

The simultaneous change of both input signals produces a non-foreseeable output configuration (output pattern) if the T input signal changes from the L-level to the H-level and the G input signal changes, either from the L-level to the H-level, or from the H-level to the L-level.

Function (sequential) matrices:

G	L		H			
T	L	H		L	Q	Q*
	①	3	?	2	L	H
	1	?	4	②	L	H
	1	③	③	2	L	H
	6	④	④	5	H	L
	6	?	3	⑤	H	L
	⑥	4	?	5	H	L

G	L		H			
T	L	H		L	Q	Q*
	⊗	?	?	⊗	L	H
	⊗	?	⊗	⊗	L	H
	⊗	⊗	⊗	⊗	L	H
	⊗	⊗	⊗	⊗	H	L
	⊗	?	⊗	⊗	H	L
	⊗	?	?	⊗	H	L

Timing diagram:

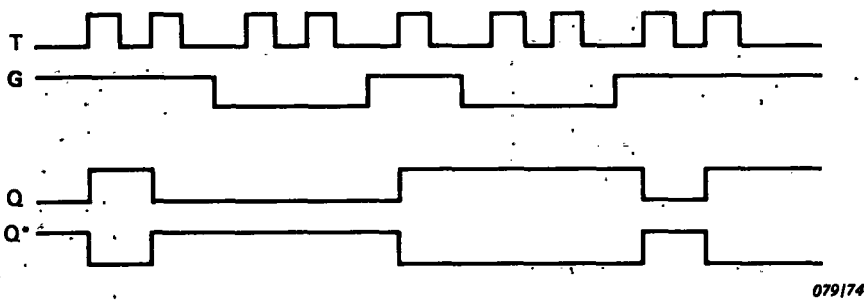


FIGURE 5

Timing diagram of general T_G circuit (continued):

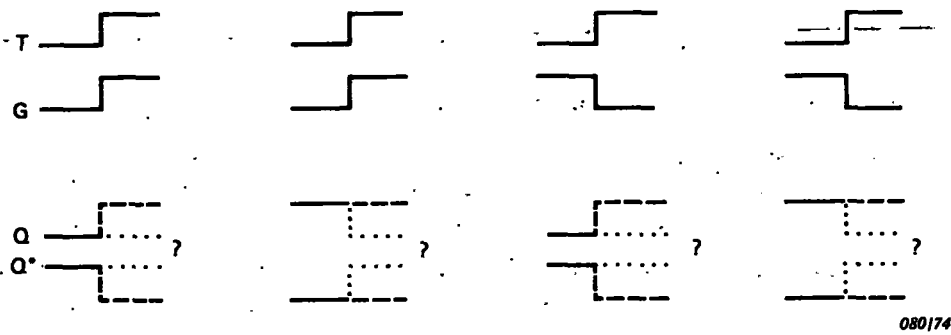


FIGURE 6

Function (sequential) matrices of the T_G circuit with T delayed with respect to G :

G	L	H	L/H		
T	H			L	H
	2	3	①	L	H
	②	②	1	L	H
	③	③	4	H	L
	3	2	④	H	L

G	L	H	L/H		
T	H			L	H
				L	H
				L	H
				H	L
				H	L

Function (sequential) matrices of the T_G circuit with G delayed with respect to T :

G	L	L/H	H		
T	L	H	L	L	H
	①	①	2	L	H
	1	3	②	L	H
	③	③	4	H	L
	3	1	④	H	L

G	L	L/H	H		
T	L	H	L	L	H
				L	H
				L	H
				H	L
				H	L

2.2.2.6 (Transition-operated) JK circuit

A circuit having two transition-operated input terminals, J and K, for which the input signals are active during the change from the L-level to the H-level.

When the signal applied to the K input terminal changes from the L-level to the H-level, it produces the output configuration (output pattern) $(Q, Q^*) = (H, L)$. The return of the input signal at the J terminal to the L-level produces no action.

When the signal applied to the J input terminal changes from the L-level to the H-level, it produces the output configuration (output pattern) $(Q, Q^*) = (L, H)$. The return of the input signal at the K terminal to the L-level produces no action.

The simultaneous change of both input signals from the L-level to the H-level produces change-over of the output configuration (output pattern).

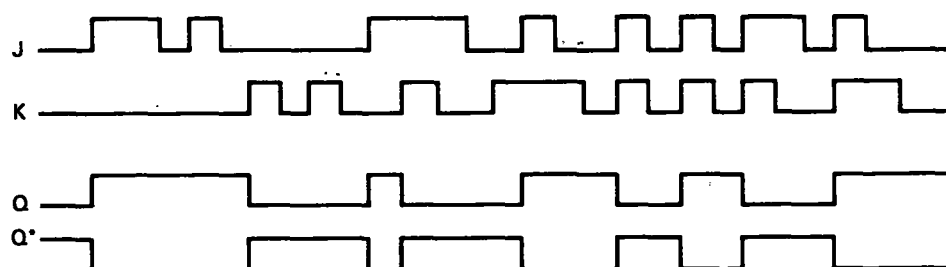
The return of either, or both, input signals to the L-level produces no action.

Function (sequential) matrices:

K	L		H			
J	L	H		L	Q	Q*
	①	4	3	①	L	H
	1	②	②	1	L	H
	4	4	③	③	H	L
	④	④	2	1	H	L

K	L		H			
J	L	H		L	Q	Q*
	⊗	⊗	⊗	⊗	L	H
	⊗	⊗	⊗	⊗	L	H
	⊗	⊗	⊗	⊗	H	L
	⊗	⊗	⊗	⊗	H	L

Timing diagram:



081/74

FIGURE 7.

2.2.2.7 (Transition-operated) $\bar{J}\bar{K}$ circuit

Description analogous to 2.2.2.6, but where the input signals are active during the change from H-level to L-level.

2.2.2.8 D_G circuit

A circuit having two level-operated input terminals D and G.

While the G input signal has the H-level, the level at the reference-output terminal Q is the same as the level of the D input signal.

When the G input signal changes from the H-level to the L-level, the output configuration (output pattern) is maintained.

While the G input signal has the L-level, the D input signal has no effect.

The simultaneous change of both input signals produces a non-foreseeable output configuration (output pattern) if the G input signal changes from the H-level to the L-level and the D input signal changes either from the L-level to the H-level, or from the H-level to the L-level.

Function (sequential) matrices (these matrices apply only for the case where D is delayed with respect to G):

G	L	H			
D	L/H	H	L	Q	Q*
	1	2	1	L	H
	2	2	1	H	L

G	L	H			
D	L/H	H	L	Q	Q*
				L	H
				H	L

Timing diagram:

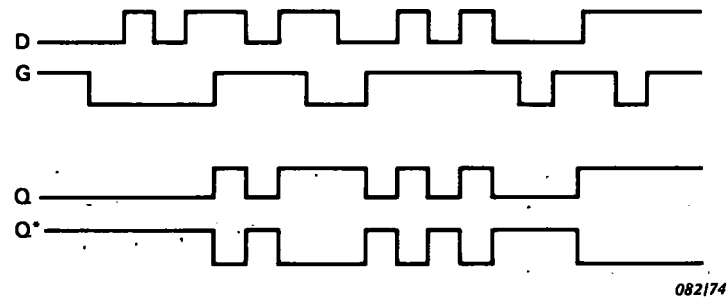


FIGURE 8

2.2.2.9 $D_{\overline{G}}$ circuit

A circuit having two level-operated input terminals, D and $\overline{G}$.

While the $\overline{G}$ input signal has the L-level, the level at the reference output terminal Q is the same as the level of the D input signal.

When the $\overline{G}$ input signal changes from the L-level to the H-level, the output configuration (output pattern) is maintained.

While the $\overline{G}$ input signal has the H-level, the D input signal has no effect.

The simultaneous change of both input signals produces a non-foreseeable output configuration (output pattern) if the $\overline{G}$ input signal changes from the L-level to the H-level and the D input signal changes either from the L-level to the H-level, or from the H-level to the L-level.

Function (sequential) matrices (these matrices apply only for the case where D is delayed with respect to $\overline{G}$):

$\overline{G}$	L		H		
D	L	H	L/H	Q	Q*
	1	2	1	L	H
	1	2	2	H	L

$\overline{G}$	L		H		
D	L	H	L/H	Q	Q*
				L	H
				H	L

Timing diagram:

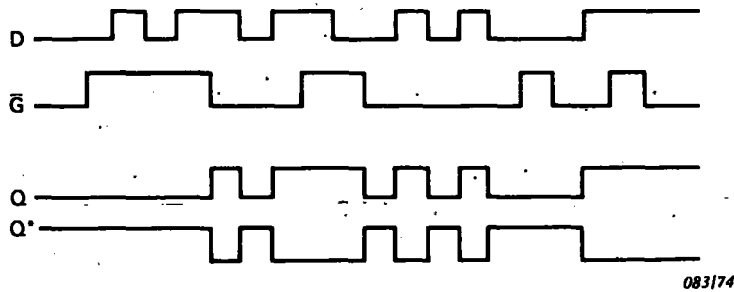


FIGURE 9

2.2.2.10 D_T circuit

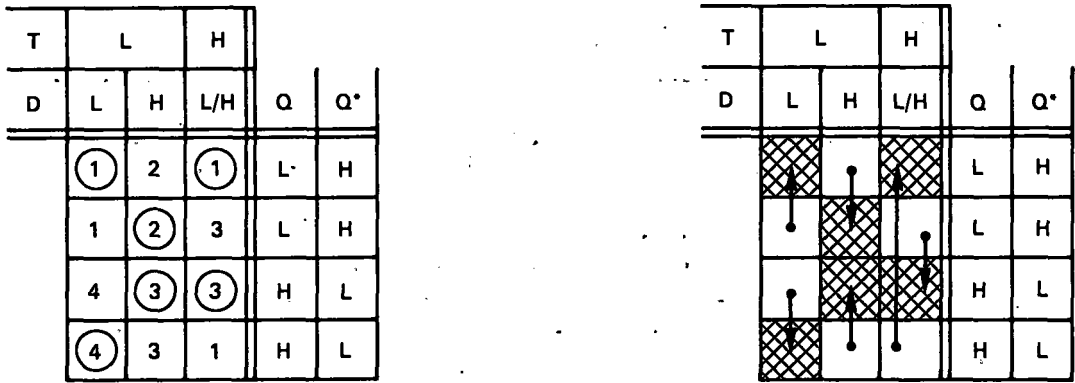
A circuit having one level-operated input terminal, D, and one transition-operated input terminal, T.

The change of the T input signal from the L-level to the H-level produces at the reference output terminal Q a level which is the same as the level of the D input signal.

When the T input signal changes from the H-level to the L-level, the output configuration (output pattern) is maintained.

While the T input signal has either the L-level or the H-level, the D input signal has no effect.

Function (sequential) matrices (the following matrices apply only for the case where D is delayed with respect to T):



Timing diagram:

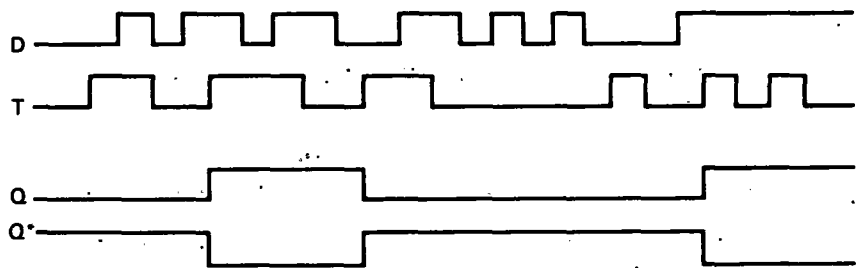


FIGURE 10

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2.2.2.11 $D_{\bar{T}}$ circuit

A circuit having one level-operated input terminal, D, and one transition-operated input terminal, $\bar{T}$.

The change of the $\bar{T}$ input signal from the H-level to the L-level produces at the reference output terminal Q a level which is the same as the level of the D input signal.

When the $\bar{T}$ input signal changes from the L-level to the H-level, the output configuration (output pattern) is maintained.

While the $\bar{T}$ input signal has either the H-level or the L-level, the D input signal has no effect.

Function (sequential) matrices (the following matrices apply for the case where D is delayed with respect to $\bar{T}$):

$\bar{T}$	L		H			
D	L/H	H	L		Q	Q*
	1	2	1		L	H
	3	2	1		L	H
	3	3	4		H	L
	1	3	4		H	L

$\bar{T}$	L		H			
D	L/H	H	L		Q	Q*
					L	H
					L	H
					H	L
					H	L

Timing diagram:

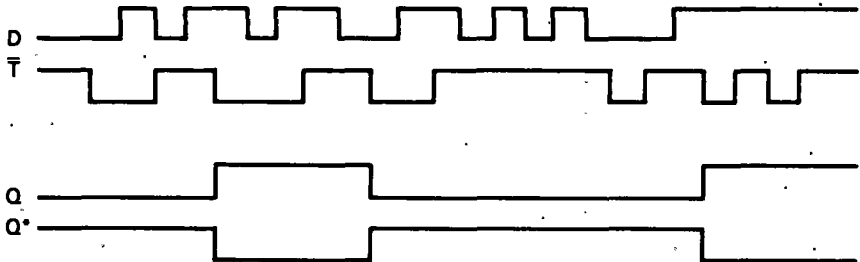


FIGURE 11

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2.2.2.12 $R_G S_G (L)$ circuit

A circuit having three level-operated input terminals R, S and G for which H is the active level.

While the G input signal has the H-level, the circuit functions as a RS (L) circuit.

When the G input signal changes from the H-level to the L-level, the output configuration (output pattern) is maintained, provided that it is not pseudo-stable.

When the output configuration (output pattern) is pseudo-stable, i. e. $(Q, Q^*) = (L, L)$, the change of the G input signal from the H-level to the L-level produces a non-foreseeable output configuration (output pattern).

While the G input signal has the L-level, the R and S input signals have no effect.

Function (sequential) matrices:

G	L				H					
R	L		H				L			
S	L	H		L		H		L	Q	Q*
	①	2	2	①	①	5	4	①	L	H
	1	②	②	1	1	5	4	?	L	H
	4	4	③	③	1	5	4	?	H	L
	④	④	3	3	1	5	④	④	H	L
	?	?	?	?	1	⑤	4	?	L	L

G	L				H				
R	L		H				L		
S	L	H		L	H		L	Q	Q'
								L	H
								?	L
								?	H
									H
	?	?	?	?				?	L

Timing diagram:

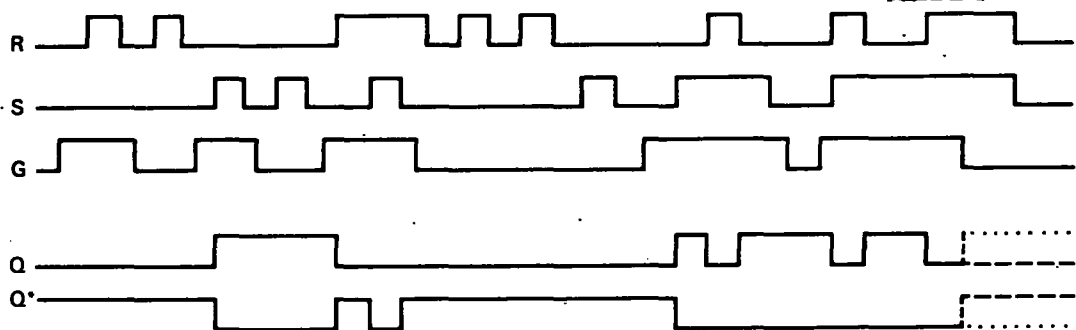


FIGURE 12

086174

2.2.2.13 $R_G S_G (L), \overline{R}_G \overline{S}_G (H)$ and $\overline{R}_G \overline{S}_G (H)$ circuits

Descriptions analogous to 2.2.2.12.

2.2.2.14 $J_T K_T$ circuit

A circuit having two level-operated input terminals, J and K, and one transition-operated input terminal, T.

When the T input signal changes from the L-level to the H-level, an output configuration (output pattern) corresponding to the levels of the J and K input signals is produced as follows:

For the input configuration (input pattern) (J, K) = (L, H),
the output configuration (output pattern) (Q, Q*) = (L, H).

For the input configuration (input pattern) (J, K) = (H, L),
the output configuration (output pattern) (Q, Q*) = (H, L).

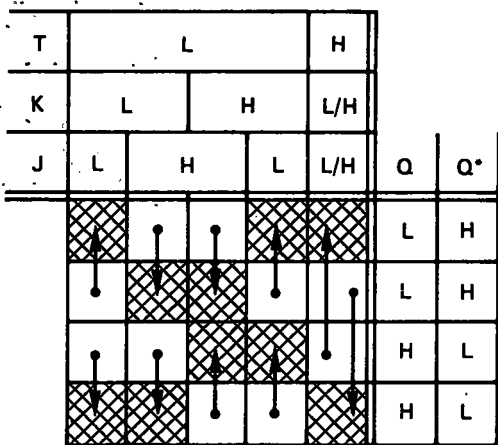
For the input configuration (input pattern) (J, K) = (H, H),
change of the output configuration (output pattern).

For the input configuration (input pattern) (J, K) = (L, L),
the output configuration (output pattern) is maintained.

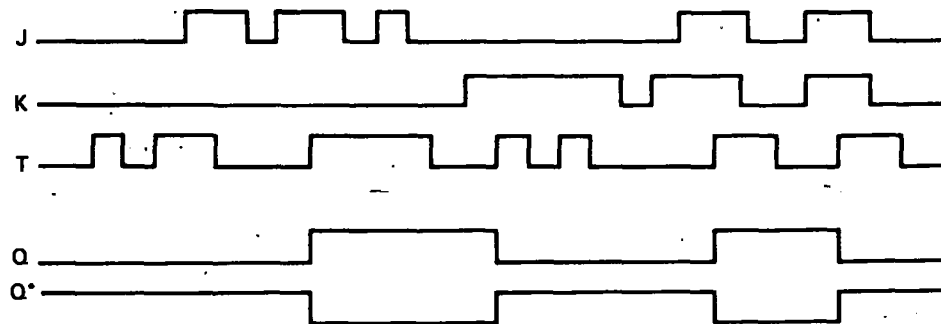
The return for the T input signal from the H-level to the L-level has no effect. When the T input signal has either the H-level or the L-level, the J and K input signals have no effect.

Function (sequential) matrices (the following matrices apply only for the case where J and K are delayed with respect to T):

T	L				H		
K	L		H		L/H		
J	L	H		L	L/H	Q	Q*
	1	2	2	1	1	L	H
	1	2	2	1	4	L	H
	4	4	3	3	1	H	L
	4	4	3	3	4	H	L



Timing diagram:



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FIGURE 13

Note. — Definitions for the other classes of $J_T K_T$ circuits are still under consideration.

2.2.2.15 $J_T K_T$, $J_T \bar{K}_T$ and $\bar{J}_T \bar{K}_T$ circuits

Descriptions analogous to 2.2.2.14.

2.2.2.16 $\bar{R}\bar{S}$ (H) $J_T K_T$ circuit

Function (sequential) matrices:

R̄S			JK				T				
S̄	L	H	H				H				
R̄	L	H	L	H				H			
T	X		H				L				
J	X		H		L		X				
K	X		L	H		L	X	Q	Q*		
3	4	①	2	2	①	①	①	L	H		
3	4	1	②	②	1	1	4	L	H		
③	4	1	?	?	?	?	?	H	H		
3	④	1	④	5	5	④	④	H	L		
3	4	1	4	⑤	⑤	4	1	H	L		

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$\overline{R}\overline{S}$			JK			T			
$\overline{S}$	L	H	H			H			
$\overline{R}$	L	H	L	H			H		
T	X		H			L			
J	X		H		L	X			
K	X		L	H	L	X	Q	Q*	

	L	H
	L	H
	H	H
	H	L
	H	L

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3. Terminology for integrated circuit memories

3.1 General terms

3.1.1 Memory cell (or memory element)

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

3.1.2 *Integrated circuit memory*

An integrated circuit consisting of memory cells (elements) and usually including associated circuits such as those for address selection, amplifiers, etc.

3.1.3 *Storage zone of data*

A subdivision of the memory, including one or several memory cells, that is the smallest part of the memory that can be selected.

Note. — The content of a storage zone of data is usually called a "word".

3.1.4 *Address*

A group of bits that identifies a particular storage zone of data

or:

the appropriate electrical signals applied to the inputs to access this storage zone.

3.1.5 *Destructive readout*

A reading process that causes the loss of stored information from the storage zone that has been read.

3.1.6 *Block*

A continuous range of memory addresses.

Note. — The number of addresses included in the range is frequently equal to 2^n .

3.1.7 *Erase*

To remove information from a memory.

3.2 *General terms relating to memory function and organization*

3.2.1 *Organization of information storage*

3.2.1.1 *Bit-oriented organization*

An arrangement in which the storage zones each consist of one memory cell.

3.2.1.2 *Word-oriented organization*

An arrangement in which the storage zones each consist of a defined number of memory cells that form a word.

3.2.1.3 *Block-oriented organization*

An arrangement in which the storage zones form a block:

Note. — The storage zones in a block may each contain a different number of memory cells.

3.2.2 *Presentation of information*

3.2.2.1 *Parallel presentation of information*

The simultaneous transmission of several bits of data on separate channels or bus lines.

3.2.2.2 *Serial presentation of information*

The transmission of several bits of data in succession on a single channel or bus line.

3.2.3 *Mode of addressing*

3.2.3.1 *Parallel addressing*

The selection of a storage zone by the simultaneous presentation of each bit of the address.

3.2.3.2 *Serial addressing*

The selection of a storage zone by the presentation in succession of each bit of the address.

3.2.3.3 *Multiplexed addressing, serial-parallel addressing*

The selection of a storage zone by the presentation of several groups of bits that together constitute the address, the bits of each group being presented in parallel and the groups themselves being presented in series.

3.3 *Types of memories*

3.3.1 *Read-only memory (ROM)*

A memory in which the contents are intended to be read only and not to be altered during normal operation.

Note. — Unless otherwise qualified, the term "read-only memory" implies that the data content is determined by its structure and is unalterable.

3.3.1.1 *Fixed-programmed read-only memory*

A read-only memory in which the data content of each cell (element) is determined during manufacture, and is thereafter unalterable.

a) *Mask-programmed read-only memory*

A fixed-programmed read-only memory in which the data content of each cell (element) is determined during manufacture by the use of a mask.

3.3.1.2 *Field-programmable read-only memory*

A read-only memory that, after being manufactured, can have the data content of each memory cell (element) altered.

a) *Programmable read-only memory (PROM)*

A field-programmable read-only memory that can have the data content of each memory cell (element) altered once only.

b) Reprogrammable read-only memory

A field-programmable read-only memory that can have the data content of each memory cell (element) altered more than once.

3.3.2 Read/write memory

A memory in which each cell (element) may be selected by applying appropriate electrical input signals, and in which the stored data may be either:

- a) sensed at appropriate output terminals, or
- b) changed in response to other appropriate electrical input signals.

3.3.3 Random-access memory (RAM)

A memory that permits access to any of its address locations in any desired sequence.

Note. — By common usage, this term usually denotes a “read/write” memory; but it could also apply to a “read-only” memory.

3.3.4 Static read/write memory

A memory in which the data content is retained in the absence of control signals.

Notes 1. — The words “read/write” may be omitted from the term when no misunderstanding may occur.
2. — A static memory may use dynamic addressing and/or sensing circuits.

3.3.5 Dynamic read/write memory

A memory in which the cells (elements) require the repetitive application of control signals in order to retain the data stored.

Notes 1. — The words “read/write” may be omitted from the term when no misunderstanding may occur.
2. — Such repetitive application of the control signals is normally called a refresh operation.
3. — A dynamic memory may use static addressing and/or sensing circuits.
4. — This definition applies whether or not the control signals are generated inside or outside the memory.

3.3.6 Volatile memory

A memory in which the data content is lost when power is no longer supplied to it.

3.3.7 Serial access memory

A memory in which storage zones can only be accessed in a predetermined sequence.

3.3.8 Content addressable memory (CAM) (associative memory)

A memory that responds with all the data in a storage zone if a portion of that data matches the data used for addressing the memory.

Note. — If a match could occur in more than one storage zone, then usually the data read out will be that contained in the storage zone having the lowest address value.

3.4 Terms related to ratings and characteristics

3.4.1 Cycle

A sequence of operations necessary to perform one of the functions of the memory.

In general, four possible cycles can be identified, i.e.:

- a) Read.
- b) Write.
- c) Read-write.
- d) Write-read.

3.4.2 Cycle time (see Notes 1, 2 and 3)

The time interval necessary to perform one cycle, i.e. the time interval between the start of a cycle and the end of that cycle.

a) Read cycle time

The time interval between the start and the end of a read cycle.

b) Write cycle time

The time interval between the start and the end of a write cycle.

c) Read-write cycle time

The time interval between the start of a cycle in which the memory is read and new data are entered, and the end of that cycle.

Note. — The term “read-modify-write cycle” is sometimes used as an alternative title for “read-write cycle”; however, this usage is deprecated because “read-modify-write” is also used in another context to indicate that data are extracted, processed, and then re-entered into the memory.

d) Write-read cycle time

The time interval between the start of a cycle in which data are entered and the memory is then read, and the end of that cycle.

Notes 1. — These times are the actual time intervals between two pulses, and may be insufficient for the completion of operations within the memory. In each case, a minimum value is specified that is the shortest time in which the memory will perform its corresponding function(s) correctly.

2. — The “end of a cycle” is to be understood as the earliest instant at which any subsequent cycle can start with correct functioning of the memory.

3. — A cycle is always performed for a constant address.

3.4.3 Write recovery time (see Note 1 to Sub-clause 3.4.2)

The time interval between the termination of a write pulse and the initiation of a new cycle, this time interval being provided for the memory to recover from a write operation and operate correctly.

3.4.4 Sense recovery time

The time interval needed to switch a memory from a write mode to a read mode, and to obtain valid data signals at the output.

3.4.5 Access time

The time interval between the application of a specific input pulse, other necessary inputs being already present, and the availability of valid data signals at an output.

The access time can only be defined with reference to an output signal (read operation).

Note. — Examples of various access times are:

Address access time: time between address input and data output.

Enable access time: time between enable input and data output.

Read access time: time between read input and data output.

In general, there are two values for each access time, depending on whether the output goes to the high level or to the low level.

3.4.6 Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

Note. — The refresh time interval is the actual time between two refresh operations and may be insufficient to protect the stored data. A maximum value is specified that is the longest interval for which correct operation is guaranteed.

3.4.7 Precharge time (of a dynamic memory)

The time interval between specified transitions at one or more inputs that allows the internal nodes of the circuit to be charged or discharged to predetermined voltage levels prior to the start of a new cycle.

Note. — This defines the actual precharge time interval, which is determined by the system in which the device is to operate. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed.

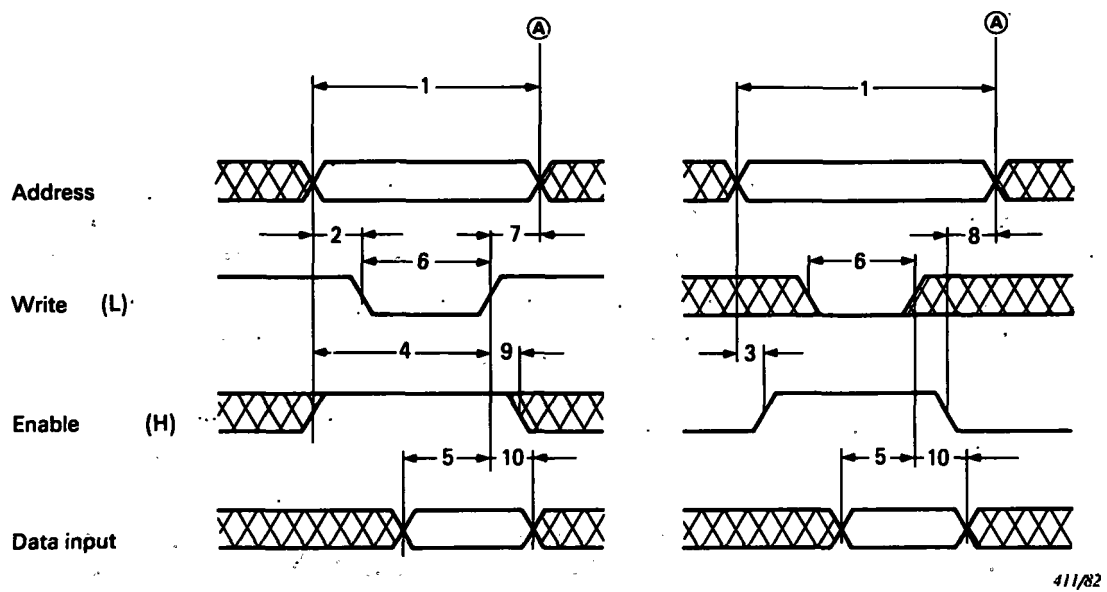
3.5 Typical waveforms for static read/write memories

Note:

Four waveform diagrams are shown to illustrate the definitions of “cycle times” (given in Sub-clause 3.4.2) for four modes of operation. These diagrams are examples only; they are for static memories, and do not necessarily represent any particular memory device.

They are not intended to indicate the precise points on the waveforms between which the various times are measured. These points shall be part of the specification for a particular integrated circuit.

The diagrams also include some additional terms to assist understanding, though no formal titles or definitions exist for those additional terms at present.



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Typical waveforms

- 1 = write cycle time
- 2 = address set-up time before write
- 3 = address set-up time before enable
- 4 = enable set-up time before (end of) write
- 5 = data-in set-up time before (end of) write

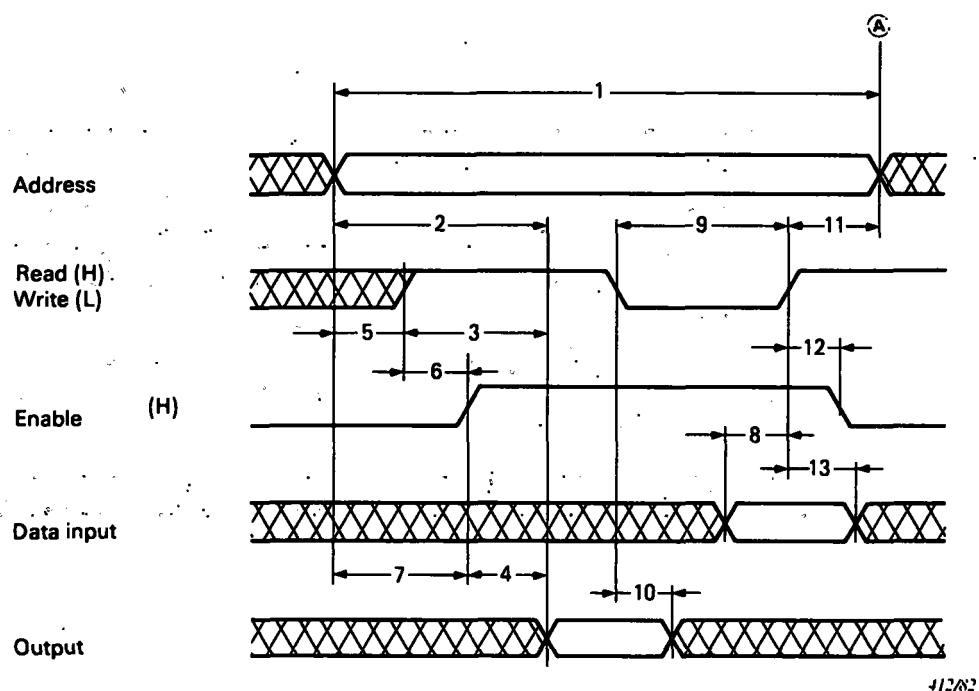
- 6 = write pulse duration
- 7 = address hold time after write
- 8 = address hold time after enable
- 9 = enable hold time after write
- 10 = data-in hold time after write

Point A is the earliest instant at which a subsequent cycle can start.

The active levels for the write and enable inputs are indicated by the letters in parentheses (H or L).


 { input: irrelevant
 output: unknown or changing

FIG. 15. — Write cycle.



Typical waveforms

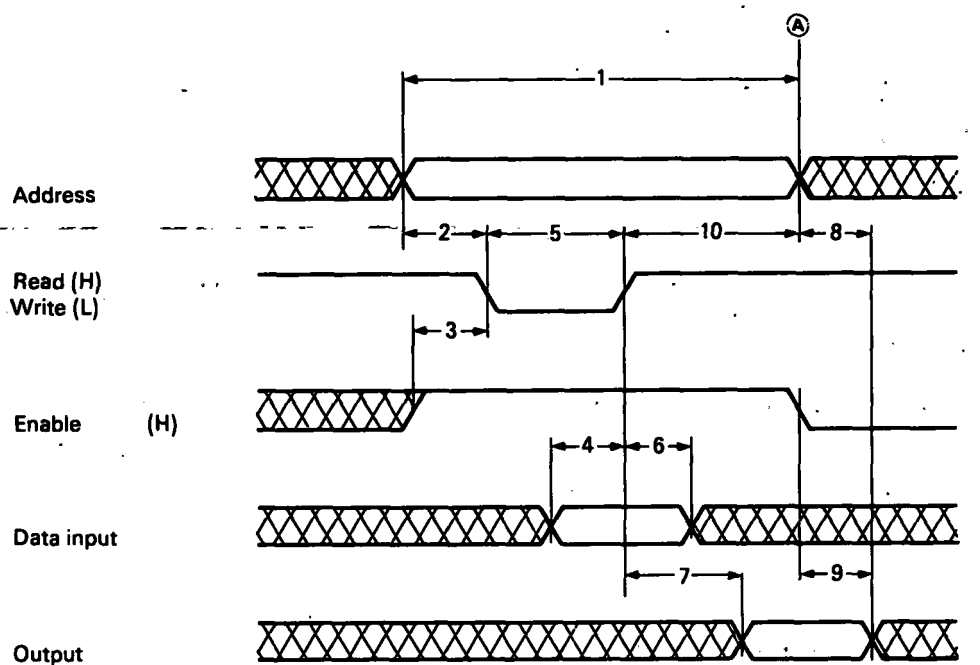
- 1 = read-write cycle time
- 2 = address access time
- 3 = read access time
- 4 = enable access time
- 5 = address set-up time before read
- 6 = read set-up time before enable
- 7 = address set-up time before enable
- 8 = data-in set-up time before (end of) write
- 9 = write pulse duration
- 10 = output valid time after read
- 11 = address hold time after write
- 12 = enable hold time after write
- 13 = data-in hold time after write

Point A is the earliest instant at which a subsequent cycle can start.

The active levels for the read/write and enable inputs are indicated by the letters in parentheses (H or L).


 { input: irrelevant
 output: unknown or changing

FIG. 16. — Read-write cycle.



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Typical waveforms

- 1 = write-read cycle time
- 2 = address set-up time before write
- 3 = enable set-up time before write
- 4 = data-in set-up time before (end of) write
- 5 = write pulse duration
- 6 = data-in hold time after write
- 7 = sense recovery time
- 8 = output valid time after address
- 9 = output valid time after enable
- 10 = write recovery time

Point A is the earliest instant at which a subsequent cycle can start.

The active levels for the write-read and enable inputs are indicated by the letters in parentheses (H or L).

 { input: irrelevant
 output: unknown or changing

FIG. 17. — Write-read cycle.

4. Terminology for integrated circuit microprocessors

4.1 *Integrated circuit microprocessor*

An integrated circuit capable of:

- operating on coded instructions, and
- carrying out, in accordance with the instructions, all of:
 - a) the acceptance of coded data for processing and/or storage;
 - b) arithmetic and logical operations on the input data together with any relevant data stored in the internal registers of the microprocessor integrated circuit and/or in external memories;
 - c) the delivery of coded data, and
- accepting and/or delivering signals controlling and/or describing the operation or state of the microprocessor integrated circuit.

Note. — The instructions may be fed in, built in or held in an internal memory.

5. Terminology for charge-transfer devices

5.1 *Device names*

5.1.1 *Charge-transfer device (CTD)*

A device in which operation depends on the effective movement of discrete packets of charge along or beneath the semiconductor surface, or through the interconnections on the semiconductor surface.

Note. — This effective movement may be produced by changing the region in which a controlling electric field is produced.

5.1.2 *Bucket-brigade device (BBD)*

A charge-transfer device that stores charge in discrete regions in a semiconductor and transfers this charge as a packet through a series of switching devices that interconnect these regions.

Notes 1. — This term and its abbreviation may be preceded by bipolar, J-FET, MOS, SOS, etc., according to the technology used for the switching devices.

2. — This device operates by re-creating the packet of charge at each position formed by an internal capacitance.

5.1.3 *Charge-coupled device (CCD)*

A charge-transfer device that stores charge in potential wells and transfers this charge almost completely as a packet by translating the position of the potential wells.

Note. — This device operates by changing the position of the same packet of charge.

5.1.4 *Charge-transfer image sensor*

A charge-transfer device in which an image is converted into packets of charge that can be transferred as the electrical representation of the image.

5.2 General terms

5.2.1a) Bias charge (for analogue signal applications)

A charge that defines the no-signal level in the analogue case and that is inserted into all potential wells (see Figures 18a and 18b).

Notes 1. — The term "background charge" is sometimes used, mainly in imaging devices.

2. — The charge is usually inserted electrically, or by radiation.

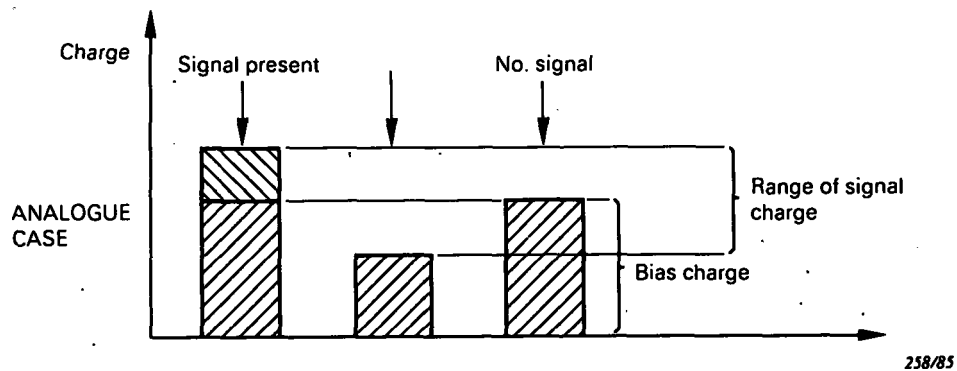


FIGURE 18a

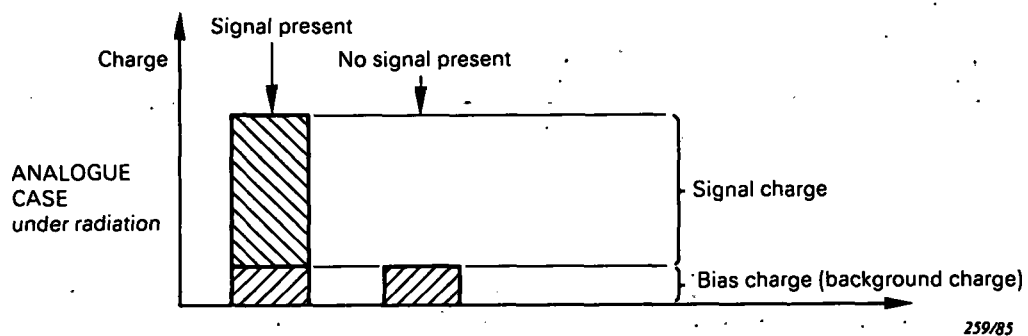


FIGURE 18b

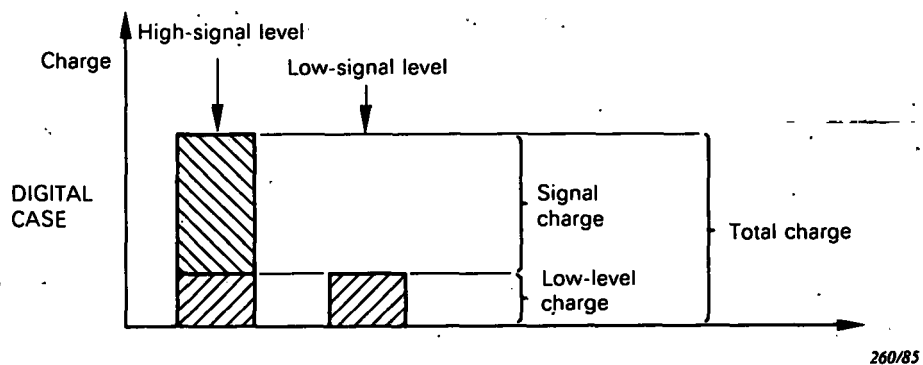


FIGURE 18c

FIG. 18. — Diagram illustrating nomenclature.