AS IEC 61131.9:2014
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AS IEC 61131.9:2014

Australian STANDARD

Programmable controllers

Part 9: Single-drop digital communication interface for small sensors and actuators (SDCI)

STANDARDS Australia

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- Australian Petroleum Production and Exploration Association
- Australian Safety Critical Systems Association
- Consult Australia
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- Institute of Chemical Engineers Australia
- Institute of Instrumentation, Control and Automation Australia
- ISACA
- Process Control Society
- University of Queensland
- Workplace Health and Safety Queensland

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PREFACE

This Standard was prepared by the Standards Australia Committee IT-006, Industrial Process Measurement, Control and Automation.

The objective of this Standard is to specify a single-drop digital communication interface technology for small sensors and actuators (SDCIs) (commonly known as IO-Link™), which extends the traditional digital input and digital output interfaces as defined in AS IEC 61131.2 towards a point-to-point communication link. This technology enables the transfer of parameters to Devices and the delivery of diagnostic information from the Devices to the automation system.

This Standard should be read in conjunction with the other parts of the AS IEC 61131 series.

This Standard is identical with, and has been reproduced from, IEC 61131-9, Ed. 1.0 (2013), *Programmable controllers*—Part 9: *Single-drop digital communication interface for small sensors and actuators (SDCI).*

As this Standard is reproduced from an International Standard, the following applies:

(a) In the source text 'this part of IEC 61131' should read 'this Australian Standard'.

(b) A full point substitutes for a comma when referring to a decimal marker.

References to International Standards should be replaced by references to Australian or Australian/New Zealand Standards, as follows:

Reference to International Standard		*Australian Standard*	
IEC		AS	
60947	Low-voltage switchgear and controlgear	60947	Low-voltage switchgear and controlgear
60947-5-2	Part 5-2: Control circuit devices and switching elements—Proximity switches	60947.5.2	Part 5.2: Control circuit devices and switching elements—Proximity switches
		AS/NZS IEC	
61000	Electromagnetic compatibility (EMC)	61000	Electromagnetic compatibility (EMC)
61000-4-2	Part 4-2: Testing and measurement techniques—Electrostatic discharge immunity test	61000.4.2	Part 4.2: Testing and measurement techniques—Electrostatic discharge immunity test
61000-4-3	Part 4-3: Testing and measurement techniques—Radiated radio-frequency electromagnetic field immunity test	61000.4.3	Part 4.3: Testing and measurement techniques—Radiated radio-frequency electromagnetic field immunity test
61000-4-4	Part 4-4: Testing and measurement techniques—Electrical fast transient/burst immunity test	61000.4.4	Part 4.4: Testing and measurement techniques—Electrical fast transient/burst immunity test
		AS/NZS	
61000-4-5	Part 4-5: Testing and measurement techniques—Surge immunity test	61000.4.5	Part 4.5: Testing and measurement techniques—Surge immunity test
		AS/NZS IEC	
61000-4-6	Part 4-6: Testing and measurement techniques—Immunity to conducted disturbances, induced by radio-frequency fields	61000.4.6	Part 4.6: Testing and measurement techniques—Immunity to conducted disturbances, induced by radio-frequency fields

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IEC		AS/NZS	
61000-6-2	Part 6-2: Generic standards—Immunity for industrial environment	61000.6.2	Part 6.2: General standards—Immunity for industrial environment
61000-6-4	Part 6-4: Generic standards—Emission standard for industrial environments	61000.6.4	Part 6.4: Generic standards—Emission standard for industrial environments
		AS IEC	
61131	Programmable controllers	61131	Programmable controllers
61131-1	Part 1: General information	61131.1	Part 1: General information
61131-2	Part 2: Equipment requirements and tests	61131.2	Part 2: Equipment requirements and tests

Only normative references that have been adopted as Australian or Australian/New Zealand Standards have been listed.

The terms ‘normative’ and ‘informative’ are used to define the application of the annex to which they apply. A normative annex is an integral part of a standard, whereas an informative annex is only for information and guidance.

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Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

CONTENTS

1 Scope ... 18
2 Normative references ... 18
3 Terms, definitions, symbols, abbreviated terms and conventions ... 19
3.1 Terms and definitions ... 19
3.2 Symbols and abbreviated terms ... 23
3.3 Conventions ... 25
3.3.1 General ... 25
3.3.2 Service parameters ... 25
3.3.3 Service procedures ... 26
3.3.4 Service attributes ... 26
3.3.5 Figures ... 26
3.3.6 Transmission octet order ... 26
3.3.7 Behavioral descriptions ... 27
4 Overview of SDCI (IO-Link™) ... 27
4.1 Purpose of technology ... 27
4.2 Positioning within the automation hierarchy ... 28
4.3 Wiring, connectors and power ... 29
4.4 Communication features of SDCI ... 29
4.5 Role of a Master ... 31
4.6 SDCI configuration ... 32
4.7 Mapping to fieldbuses ... 32
4.8 Standard structure ... 32
5 Physical Layer (PL) ... 33
5.1 General ... 33
5.1.1 Basics ... 33
5.1.2 Topology ... 33
5.2 Physical layer services ... 34
5.2.1 Overview ... 34
5.2.2 PL services ... 35
5.3 Transmitter/Receiver ... 37
5.3.1 Description method ... 37
5.3.2 Electrical requirements ... 37
5.3.3 Timing requirements ... 41
5.4 Power supply ... 44
5.4.1 Power supply options ... 44
5.4.2 Power-on requirements ... 45
5.5 Medium ... 45
5.5.1 Connectors ... 45
5.5.2 Cable ... 47
6 Standard Input and Output (SIO) ... 48
7 Data link layer (DL) ... 48
7.1 General ... 48
7.2 Data link layer services ... 50
7.2.1 DL-B services ... 50

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

Documents
Document Sharing Hub

7.2.2 DL-A services ... 61
7.3 Data link layer protocol ... 66
7.3.1 Overview ... 66
7.3.2 DL-mode handler ... 67
7.3.3 Message handler ... 75
7.3.4 Process Data handler ... 82
7.3.5 On-request Data handler ... 85
7.3.6 ISDU handler ... 88
7.3.7 Command handler ... 92
7.3.8 Event handler ... 95
8 Application layer (AL) ... 98
8.1 General ... 98
8.2 Application layer services ... 99
8.2.1 AL services within Master and Device ... 99
8.2.2 AL Services ... 100
8.3 Application layer protocol ... 108
8.3.1 Overview ... 108
8.3.2 On-request Data transfer ... 108
8.3.3 Event processing ... 114
8.3.4 Process Data cycles ... 117
9 System management (SM) ... 118
9.1 General ... 118
9.2 System management of the Master ... 118
9.2.1 Overview ... 118
9.2.2 SM Master services ... 120
9.2.3 SM Master protocol ... 125
9.3 System management of the Device ... 133
9.3.1 Overview ... 133
9.3.2 SM Device services ... 135
9.3.3 SM Device protocol ... 141
10 Device ... 148
10.1 Overview ... 148
10.2 Process Data Exchange (PDE) ... 149
10.3 Parameter Manager (PM) ... 149
10.3.1 General ... 149
10.3.2 Parameter manager state machine ... 149
10.3.3 Dynamic parameter ... 151
10.3.4 Single parameter ... 152
10.3.5 Block parameter ... 153
10.3.6 Concurrent parameterization access ... 155
10.3.7 Command handling ... 155
10.4 Data Storage (DS) ... 155
10.4.1 General ... 155
10.4.2 Data Storage state machine ... 155
10.4.3 DS configuration ... 157
10.4.4 DS memory space ... 157
10.4.5 DS Index_List ... 158
10.4.6 DS parameter availability ... 158
10.4.7 DS without ISDU ... 158

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

10.4.8 DS parameter change indication ... 158
10.5 Event Dispatcher (ED) ... 158
10.6 Device features ... 158
10.6.1 General ... 158
10.6.2 Device backward compatibility ... 159
10.6.3 Protocol revision compatibility ... 159
10.6.4 Factory settings ... 159
10.6.5 Application reset ... 159
10.6.6 Device reset ... 159
10.6.7 Visual SDCI indication ... 159
10.6.8 Parameter access locking ... 160
10.6.9 Data Storage locking ... 160
10.6.10 Device parameter locking ... 160
10.6.11 Device user interface locking ... 160
10.6.12 Offset time ... 160
10.6.13 Data Storage concept ... 161
10.6.14 Block Parameter ... 161
10.7 Device design rules and constraints ... 161
10.7.1 General ... 161
10.7.2 Process Data ... 161
10.7.3 Communication loss ... 161
10.7.4 Direct Parameter ... 161
10.7.5 ISDU communication channel ... 162
10.7.6 DeviceID rules related to Device variants ... 162
10.7.7 Protocol constants ... 162
10.8 IO Device description (IODD) ... 163
10.9 Device diagnosis ... 163
10.9.1 Concepts ... 163
10.9.2 Events ... 164
10.9.3 Visual indicators ... 165
10.10 Device connectivity ... 166
11 Master ... 166
11.1 Overview ... 166
11.1.1 Generic model for the system integration of a Master ... 166
11.1.2 Structure and services of a Master ... 166
11.2 Configuration Manager (CM) ... 169
11.2.1 General ... 169
11.2.2 Configuration parameter ... 171
11.2.3 State machine of the Configuration Manager ... 173
11.3 Data Storage (DS) ... 175
11.3.1 Overview ... 175
11.3.2 DS data object ... 175
11.3.3 DS state machine ... 175
11.3.4 Parameter selection for Data Storage ... 181
11.4 On-Request Data exchange (ODE) ... 181
11.5 Diagnosis Unit (DU) ... 182
11.6 PD Exchange (PDE) ... 183
11.6.1 General ... 183
11.6.2 Process Data mapping ... 183

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

11.6.3 Process Data invalid/valid qualifier status ... 184
11.7 Port and Device configuration tool (PDCT) ... 185
11.7.1 General ... 185
11.7.2 Basic layout examples ... 185
11.8 Gateway application ... 186
11.8.1 General ... 186
11.8.2 Changing Device configuration including Data Storage ... 186
11.8.3 Parameter server and recipe control ... 186
11.8.4 Anonymous parameters ... 186
11.8.5 Virtual port mode DIwithSDCI ... 187
Annex A (normative) Codings, timing constraints, and errors ... 190
Annex B (normative) Parameter and commands ... 211
Annex C (normative) ErrorTypes (ISDU errors) ... 228
Annex D (normative) EventCodes (diagnosis information) ... 233
Annex E (normative) Data types ... 236
Annex F (normative) Structure of the Data Storage data object ... 247
Annex G (normative) Master and Device conformity ... 248
Annex H (informative) Residual error probabilities ... 254
Annex I (informative) Example sequence of an ISDU transmission ... 256
Annex J (informative) Recommended methods for detecting parameter changes ... 258
Bibliography ... 259

Figure 1 – Example of a confirmed service ... 26
Figure 2 – Memory storage and transmission order for WORD based data types ... 27
Figure 3 – SDCI compatibility with IEC 61131-2 ... 27
Figure 4 – Domain of the SDCI technology within the automation hierarchy ... 28
Figure 5 – Generic Device model for SDCI (Master's view) ... 29
Figure 6 – Relationship between nature of data and transmission types ... 30
Figure 7 – Object transfer at the application layer level (AL) ... 31
Figure 8 – Logical structure of Master and Device ... 32
Figure 9 – Three wire connection system ... 33
Figure 10 – Topology of SDCI ... 34
Figure 11 – Physical layer (Master) ... 34
Figure 12 – Physical layer (Device) ... 35
Figure 13 – Line driver reference schematics ... 37
Figure 14 – Receiver reference schematics ... 37
Figure 15 – Reference schematics for SDCI 3-wire connection system ... 38
Figure 16 – Voltage level definitions ... 38
Figure 17 – Switching thresholds ... 39
Figure 18 – Format of an SDCI UART frame ... 41
Figure 19 – Eye diagram for the 'H' and 'L' detection ... 42
Figure 20 – Eye diagram for the correct detection of a UART frame ... 42
Figure 21 – Wake-up request ... 44
Figure 22 – Power-on timing for Power1 ... 45

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Figure 23 – Pin layout front view 46
Figure 24 – Class A and B port definitions 47
Figure 25 – Reference schematic for effective line capacitance and loop resistance 47
Figure 26 – Structure and services of the data link layer (Master) 49
Figure 27 – Structure and services of the data link layer (Device) 49
Figure 28 – State machines of the data link layer 67
Figure 29 – Example of an attempt to establish communication 67
Figure 30 – Failed attempt to establish communication 68
Figure 31 – Retry strategy to establish communication 68
Figure 32 – Fallback procedure 69
Figure 33 – State machine of the Master DL-mode handler 70
Figure 34 – Submachine 1 to establish communication 71
Figure 35 – State machine of the Device DL-mode handler 73
Figure 36 – SDCI message sequences 75
Figure 37 – Overview of M-sequence types 76
Figure 38 – State machine of the Master message handler 77
Figure 39 – Submachine "Response 3" of the message handler 78
Figure 40 – Submachine "Response 8" of the message handler 78
Figure 41 – Submachine "Response 15" of the message handler 78
Figure 42 – State machine of the Device message handler 81
Figure 43 – Interleave mode for the segmented transmission of Process Data 83
Figure 44 – State machine of the Master Process Data handler 83
Figure 45 – State machine of the Device Process Data handler 85
Figure 46 – State machine of the Master On-request Data handler 86
Figure 47 – State machine of the Device On-request Data handler 87
Figure 48 – Structure of the ISDU 88
Figure 49 – State machine of the Master ISDU handler 90
Figure 50 – State machine of the Device ISDU handler 91
Figure 51 – State machine of the Master command handler 93
Figure 52 – State machine of the Device command handler 94
Figure 53 – State machine of the Master Event handler 96
Figure 54 – State machine of the Device Event handler 97
Figure 55 – Structure and services of the application layer (Master) 98
Figure 56 – Structure and services of the application layer (Device) 99
Figure 57 – OD state machine of the Master AL 109
Figure 58 – OD state machine of the Device AL 110
Figure 59 – Sequence diagram for the transmission of On-request Data 112
Figure 60 – Sequence diagram for On-request Data in case of errors 113
Figure 61 – Sequence diagram for On-request Data in case of timeout 113
Figure 62 – Event state machine of the Master AL 114
Figure 63 – Event state machine of the Device AL 115
Figure 64 – Single Event scheduling 116
Figure 65 – Sequence diagram for output Process Data 117

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Figure 66 – Sequence diagram for input Process Data 118
Figure 67 – Structure and services of the Master system management 119
Figure 68 – Sequence chart of the use case "port x setup" 120
Figure 69 – Main state machine of the Master system management 126
Figure 70 – SM Master submachine CheckCompatibility_1 128
Figure 71 – Activity for state "CheckVxy" 130
Figure 72 – Activity for state "CheckCompV10" 130
Figure 73 – Activity for state "CheckComp" 131
Figure 74 – Activity (write parameter) in state "RestartDevice" 131
Figure 75 – SM Master submachine CheckSerNum_3 132
Figure 76 – Activity (check SerialNumber) for state CheckSerNum_3 133
Figure 77 – Structure and services of the system management (Device) 134
Figure 78 – Sequence chart of the use case "INACTIVE – SIO – SDCI – SIO" 135
Figure 79 – State machine of the Device system management 142
Figure 80 – Sequence chart of a regular Device startup 145
Figure 81 – Sequence chart of a Device startup in compatibility mode 146
Figure 82 – Sequence chart of a Device startup when compatibility fails 147
Figure 83 – Structure and services of a Device 148
Figure 84 – The Parameter Manager (PM) state machine 150
Figure 85 – Positive and negative parameter checking result 152
Figure 86 – Positive block parameter download with Data Storage request 153
Figure 87 – Negative block parameter download 154
Figure 88 – The Data Storage (DS) state machine 156
Figure 89 – Data Storage request message sequence 157
Figure 90 – Cycle timing 160
Figure 91 – Event flow in case of successive errors 165
Figure 92 – Device LED indicator timing 165
Figure 93 – Generic relationship of SDCI technology and fieldbus technology 166
Figure 94 – Structure and services of a Master 168
Figure 95 – Relationship of the common Master applications 168
Figure 96 – Sequence diagram of configuration manager actions 170
Figure 97 – Ports in MessageSync mode 171
Figure 98 – State machine of the Configuration Manager 173
Figure 99 – Main state machine of the Data Storage mechanism 175
Figure 100 – Submachine "UpDownload_2" of the Data Storage mechanism 176
Figure 101 – Data Storage submachine "Upload_7" 177
Figure 102 – Data Storage upload sequence diagram 177
Figure 103 – Data Storage submachine "Download_10" 178
Figure 104 – Data Storage download sequence diagram 178
Figure 105 – State machine of the On-request Data Exchange 181
Figure 106 – System overview of SDCI diagnosis information propagation via Events 183
Figure 107 – Process Data mapping from ports to the gateway data stream 184
Figure 108 – Propagation of PD qualifier status between Master and Device 184

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Figure 109 – Example 1 of a PDCT display layout 185
Figure 110 – Example 2 of a PDCT display layout 186
Figure 111 – Alternative Device configuration 187
Figure 112 – Virtual port mode "DIwithSDCI" 188
Figure A.1 – M-sequence control 190
Figure A.2 – Checksum/M-sequence type octet 191
Figure A.3 – Checksum/status octet 192
Figure A.4 – Principle of the checksum calculation and compression 193
Figure A.5 – M-sequence TYPE_0 194
Figure A.6 – M-sequence TYPE_1_1 194
Figure A.7 – M-sequence TYPE_1_2 195
Figure A.8 – M-sequence TYPE_1_V 195
Figure A.9 – M-sequence TYPE_2_1 196
Figure A.10 – M-sequence TYPE_2_2 196
Figure A.11 – M-sequence TYPE_2_3 196
Figure A.12 – M-sequence TYPE_2_4 197
Figure A.13 – M-sequence TYPE_2_5 197
Figure A.14 – M-sequence TYPE_2_6 197
Figure A.15 – M-sequence TYPE_2_V 198
Figure A.16 – M-sequence timing 201
Figure A.17 – I-Service octet 203
Figure A.18 – Check of ISDU integrity via CHKPDU 205
Figure A.19 – Examples of request formats for ISDUs 206
Figure A.20 – Examples of response ISDUs 206
Figure A.21 – Examples of read and write request ISDUs 207
Figure A.22 – Structure of StatusCode type 1 208
Figure A.23 – Structure of StatusCode type 2 208
Figure A.24 – Indication of activated Events 209
Figure A.25 – Structure of the EventQualifier 209
Figure B.1 – Classification and mapping of Direct Parameters 211
Figure B.2 – MinCycleTime 213
Figure B.3 – M-sequence Capability 214
Figure B.4 – RevisionID 215
Figure B.5 – ProcessDataIn 215
Figure B.6 – Index space for ISDU data objects 217
Figure B.7 – Structure of the Offset Time 226
Figure E.1 – Coding examples of UIntegerT 237
Figure E.2 – Coding examples of IntegerT 239
Figure E.3 – Singular access of StringT 240
Figure E.4 – Coding example of OctetStringT 241
Figure E.5 – Definition of TimeT 241
Figure E.6 – Example of an ArrayT data structure 243
Figure E.7 – Example 2 of a RecordT structure 245

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

Documents
Document Sharing Hub

Figure E.8 – Example 3 of a RecordT structure 245
Figure E.9 – Write requests for example 3 246
Figure G.1 – Test setup for electrostatic discharge (Master) 250
Figure G.2 – Test setup for RF electromagnetic field (Master) 250
Figure G.3 – Test setup for fast transients (Master) 251
Figure G.4 – Test setup for RF common mode (Master) 251
Figure G.5 – Test setup for electrostatic discharges (Device) 252
Figure G.6 – Test setup for RF electromagnetic field (Device) 252
Figure G.7 – Test setup for fast transients (Device) 252
Figure G.8 – Test setup for RF common mode (Device) 253
Figure H.1 – Residual error probability for the SDCI data integrity mechanism 254
Figure I.1 – Example for ISDU transmissions *(1 of 2)* 256

Table 1 – Service assignments of Master and Device 35
Table 2 – PL_SetMode 35
Table 3 – PL_WakeUp 36
Table 4 – PL_Transfer 36
Table 5 – Electric characteristics of a receiver 39
Table 6 – Electric characteristics of a Master port 39
Table 7 – Electric characteristics of a Device 40
Table 8 – Dynamic characteristics of the transmission 43
Table 9 – Wake-up request characteristics 44
Table 10 – Power-on timing 45
Table 11 – Pin assignments 46
Table 12 – Cable characteristics 47
Table 13 – Cable conductor assignments 48
Table 14 – Service assignments within Master and Device 50
Table 15 – DL_ReadParam 51
Table 16 – DL_WriteParam 51
Table 17 – DL_Read 52
Table 18 – DL_Write 53
Table 19 – DL_ISDUTransport 54
Table 20 – DL_ISDUAbort 55
Table 21 – DL_PDOutputUpdate 55
Table 22 – DL_PDOutputTransport 56
Table 23 – DL_PDInputUpdate 57
Table 24 – DL_PDInputTransport 57
Table 25 – DL_PDCycle 58
Table 26 – DL_SetMode 58
Table 27 – DL_Mode 59
Table 28 – DL_Event 60
Table 29 – DL_EventConf 60
Table 30 – DL_EventTrigger 61

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Table 31 – DL_Control 61
Table 32 – DL-A services within Master and Device 62
Table 33 – OD 62
Table 34 – PD 63
Table 35 – EventFlag 64
Table 36 – PDInStatus 65
Table 37 – MHInfo 65
Table 38 – ODTrig 66
Table 39 – PDTrig 66
Table 40 – Wake-up procedure and retry characteristics 69
Table 41 – Fallback timing characteristics 70
Table 42 – State transition tables of the Master DL-mode handler 71
Table 43 – State transition tables of the Device DL-mode handler 74
Table 44 – State transition table of the Master message handler 79
Table 45 – State transition tables of the Device message handler 82
Table 46 – State transition tables of the Master Process Data handler 84
Table 47 – State transition tables of the Device Process Data handler 85
Table 48 – State transition tables of the Master On-request Data handler 86
Table 49 – State transition tables of the Device On-request Data handler 88
Table 50 – FlowCTRL definitions 89
Table 51 – State transition tables of the Master ISDU handler 90
Table 52 – State transition tables of the Device ISDU handler 92
Table 53 – Control codes 93
Table 54 – State transition tables of the Master command handler 93
Table 55 – State transition tables of the Device command handler 94
Table 56 – Event memory 95
Table 57 – State transition tables of the Master Event handler 96
Table 58 – State transition tables of the Device Event handler 97
Table 59 – AL services within Master and Device 99
Table 60 – AL_Read 100
Table 61 – AL_Write 101
Table 62 – AL_Abort 102
Table 63 – AL_GetInput 102
Table 64 – AL_NewInput 103
Table 65 – AL_SetInput 104
Table 66 – AL_PDCycle 104
Table 67 – AL_GetOutput 105
Table 68 – AL_NewOutput 105
Table 69 – AL_SetOutput 106
Table 70 – AL_Event 107
Table 71 – AL_Control 108
Table 72 – States and transitions for the OD state machine of the Master AL 109
Table 73 – States and transitions for the OD state machine of the Device AL 111

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Table 74 – State and transitions of the Event state machine of the Master AL 114
Table 75 – State and transitions of the Event state machine of the Device AL 115
Table 76 – SM services within the Master 121
Table 77 – SM_SetPortConfig 121
Table 78 – Definition of the InspectionLevel (IL) 122
Table 79 – Definitions of the Target Modes 123
Table 80 – SM_GetPortConfig 123
Table 81 – SM_PortMode 124
Table 82 – SM_Operate 125
Table 83 – State transition tables of the Master system management 127
Table 84 – State transition tables of the Master submachine CheckCompatibility_1 128
Table 85 – State transition tables of the Master submachine CheckSerNum_3 132
Table 86 – SM services within the Device 136
Table 87 – SM_SetDeviceCom 136
Table 88 – SM_GetDeviceCom 137
Table 89 – SM_SetDeviceIdent 138
Table 90 – SM_GetDeviceIdent 139
Table 91 – SM_SetDeviceMode 140
Table 92 – SM_DeviceMode 141
Table 93 – State transition tables of the Device system management 142
Table 94 – State transition tables of the PM state machine 150
Table 95 – Definitions of parameter checks 152
Table 96 – State transition table of the Data Storage state machine 156
Table 97 – Overview of the protocol constants for Devices 162
Table 98 – Classification of Device diagnosis incidents 164
Table 99 – Timing for LED indicators 165
Table 100 – Internal variables and Events to control the common Master applications 169
Table 101 – State transition tables of the Configuration Manager 174
Table 102 – States and transitions of the Data Storage state machines 179
Table 103 – State transition table of the ODE state machine 181
Table 104 – State transitions of the state machine "DIwithSDCI" 188
Table A.1 – Values of communication channel 190
Table A.2 – Values of R/W 191
Table A.3 – Values of M-sequence types 191
Table A.4 – Data types for user data 192
Table A.5 – Values of PD status 192
Table A.6 – Values of the Event flag 193
Table A.7 – M-sequence types for the STARTUP mode 198
Table A.8 – M-sequence types for the PREOPERATE mode 198
Table A.9 – M-sequence types for the OPERATE mode (legacy protocol) 199
Table A.10 – M-sequence types for the OPERATE mode 199
Table A.11 – Recommended MinCycleTimes 201
Table A.12 – Definition of the nibble "I-Service" 203

Accessed by MONASH UNIVERSITY LIBRARY on 12 Jun 2015 (Document currency not guaranteed when printed)

AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Table A.13 – ISDU syntax 204
Table A.14 – Definition of nibble Length and octet ExtLength 204
Table A.15 – Use of Index formats 205
Table A.16 – Mapping of EventCodes (type 1) 208
Table A.17 – Values of INSTANCE 209
Table A.18 – Values of SOURCE 210
Table A.19 – Values of TYPE 210
Table A.20 – Values of MODE 210
Table B.1 – Direct Parameter page 1 and 2 212
Table B.2 – Types of MasterCommands 213
Table B.3 – Possible values of MasterCycleTime and MinCycleTime 214
Table B.4 – Values of ISDU 214
Table B.5 – Values of SIO 215
Table B.6 – Permitted combinations of BYTE and Length 215
Table B.7 – Implementation rules for parameters and commands 217
Table B.8 – Index assignment of data objects (Device parameter) 218
Table B.9 – Coding of SystemCommand (ISDU) 219
Table B.10 – Data Storage Index assignments 220
Table B.11 – Structure of Index_List 221
Table B.12 – Device locking possibilities 222
Table B.13 – Device status parameter 224
Table B.14 – Detailed Device Status (Index 0x0025) 225
Table B.15 – Time base coding and values of Offset Time 226
Table C.1 – ErrorTypes 228
Table C.2 – Derived ErrorTypes 231
Table D.1 – EventCodes 233
Table D.2 – Basic SDCI EventCodes 235
Table E.1 – BooleanT 236
Table E.2 – BooleanT coding 236
Table E.3 – UIntegerT 237
Table E.4 – IntegerT 237
Table E.5 – IntegerT coding (8 octets) 238
Table E.6 – IntegerT coding (4 octets) 238
Table E.7 – IntegerT coding (2 octets) 238
Table E.8 – IntegerT coding (1 octet) 238
Table E.9 – Float32T 239
Table E.10 – Coding of Float32T 239
Table E.11 – StringT 240
Table E.12 – OctetStringT 240
Table E.13 – TimeT 241
Table E.14 – Coding of TimeT 242
Table E.15 – TimeSpanT 242
Table E.16 – Coding of TimeSpanT 242

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AVA Documents
Document Sharing Hub

Full document details: AS IEC 61131.9-2014

Table E.17 – Structuring rules for ArrayT 243
Table E.18 – Example for the access of an ArrayT 243
Table E.19 – Structuring rules for RecordT 244
Table E.20 – Example 1 for the access of a RecordT 244
Table E.21 – Example 2 for the access of a RecordT 244
Table E.22 – Example 3 for the access of a RecordT 245
Table F.1 – Structure of the stored DS data object 247
Table F.2 – Associated header information for stored DS data objects 247
Table G.1 – EMC test conditions for SDCI 248
Table G.2 – EMC test levels 249
Table J.1 – Proper CRC generator polynomials 258

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INTRODUCTION

0.1 General

IEC 61131-9 is part of a series of standards on programmable controllers and the associated peripherals and should be read in conjunction with the other parts of the series.

Where a conflict exists between this and other IEC standards (except basic safety standards), the provisions of this standard should be considered to govern in the area of programmable controllers and their associated peripherals.

The increased use of micro-controllers embedded in low-cost sensors and actuators has provided opportunities for adding diagnosis and configuration data to support increasing application requirements.

The driving force for the SDCI (IO-Link™[1]) technology is the need of these low-cost sensors and actuators to exchange this diagnosis and configuration data with a controller (PC or PLC) using a low-cost, digital communication technology while maintaining backward compatibility with the current DI/DO signals.

In fieldbus concepts, the SDCI technology defines a generic interface for connecting sensors and actuators to a Master unit, which may be combined with gateway capabilities to become a fieldbus remote I/O node.

Any SDCI compliant Device can be attached to any available interface port of the Master. SDCI compliant Devices perform physical to digital conversion in the Device, and then communicate the result directly in a standard format using "coded switching" of the 24 V I/O signalling line, thus removing the need for different DI, DO, AI, AO modules and a variety of cables.

Physical topology is point-to-point from each Device to the Master using 3 wires over distances up to 20 m. The SDCI physical interface is backward compatible with the usual 24 V I/O signalling specified in IEC 61131-2. Transmission rates of 4,8 kbit/s, 38,4 kbit/s and 230,4 kbit/s are supported.

The Master of the SDCI interface detects, identifies and manages Devices plugged into its ports.

Tools allow the association of Devices with their corresponding electronic I/O Device Descriptions (IODD) and their subsequent configuration to match the application requirements.

The SDCI technology specifies three different levels of diagnostic capabilities: for immediate response by automated needs during the production phase, for medium term response by operator intervention, or for longer term commissioning and maintenance via extended diagnosis information.

The structure of this standard is described in 4.8.

Conformity with IEC 61131-9 cannot be claimed unless the requirements of Annex G are met.

Terms of general use are defined in IEC 61131-1 or in the IEC 60050 series. More specific terms are defined in each part.

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0.2 Patent declaration

The International Electrotechnical Commission (IEC) draws attention to the fact that it is claimed that compliance with this document may involve the use of patents concerning the point-to-point serial communication interface for small sensors and actuators as follows, where the [xx] notation indicates the holder of the patent right:

DE 10030845B4 EP 1168271B1 US 6889282B2	[AB]	Fieldbus connecting system for actuators or sensors
EP 1203933 B1	[FE]	Sensor device for measuring at least one variable
DE 10 2004 035 831.1	[SI]	Operational status of a computer system is checked by comparison of actual parameters with reference values and modification to software if needed
DE 102 119 39 A1 US 2003/0200323 A1	[SK]	Coupling apparatus for the coupling of devices to a bus system

IEC takes no position concerning the evidence, validity and scope of these patent rights.

The holders of these patents rights have assured the IEC that they are willing to negotiate licences either free of charge or under reasonable and non-discriminatory terms and conditions with applicants throughout the world. In this respect, the statements of the holders of these patent rights are registered with IEC.

Information may be obtained from:

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ISO (www.iso.org/patents) and IEC (http://patents.iec.ch) maintain on-line data bases of patents relevant to their standards. Users are encouraged to consult the databases for the most up to date information concerning patents.

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AUSTRALIAN STANDARD

Programmable controllers

Part 9:
Single-drop digital communication interface for small sensors and actuators (SDCI)

1 Scope

This part of IEC 61131 specifies a single-drop digital communication interface technology for small sensors and actuators SDCI (commonly known as IO-Link™[2]), which extends the traditional digital input and digital output interfaces as defined in IEC 61131-2 towards a point-to-point communication link. This technology enables the transfer of parameters to Devices and the delivery of diagnostic information from the Devices to the automation system.

This technology is mainly intended for use with simple sensors and actuators in factory automation, which include small and cost-effective microcontrollers.

This part specifies the SDCI communication services and protocol (physical layer, data link layer and application layer in accordance with the ISO/OSI reference model) for both SDCI Masters and Devices.

This part also includes EMC test requirements.

This part does not cover communication interfaces or systems incorporating multiple point or multiple drop linkages, or integration of SDCI into higher level systems such as fieldbuses.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60947-5-2, *Low-voltage switchgear and controlgear – Part 5-2: Control circuit devices and switching elements – Proximity switches*

IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

IEC 61000-4-3, *Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques – Radiated, radio-frequency, electromagnetic field immunity test*

IEC 61000-4-4, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 61000-4-5, *Electromagnetic compatibility (EMC) – Part 4-5: Testing and measurement techniques – Surge immunity test*

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IEC 61000-4-6, *Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields*

IEC 61000-4-11, *Electromagnetic compatibility (EMC) – Part 4-11: Testing and measurement techniques – Voltage dips, short interruptions and voltage variations immunity tests*

IEC 61000-6-2, *Electromagnetic compatibility (EMC) – Part 6-2: Generic standards – Immunity for industrial environments*

IEC 61000-6-4, *Electromagnetic compatibility (EMC) – Part 6-4: Generic standards – Emission standard for industrial environments*

IEC 61076-2-101, *Connectors for electronic equipment – Product requirements – Part 2-101: Circular connectors – Detail specification for M12 connectors with screw-locking*

IEC 61131-1, *Programmable controllers – Part 1: General information*

IEC 61131-2, *Programmable controllers – Part 2: Equipment requirements and tests*

IEC/TR 62390, *Common automation device – Profile guideline*

ISO/IEC 646:1991, *Information technology – ISO 7-bit coded character set for information interchange*

ISO/IEC 2022, *Information technology – Character code structure and extension techniques*

ISO/IEC 10646, *Information technology – Universal Multiple-Octet Coded Character Set (UCS)*

ISO/IEC 10731, *Information technology – Open Systems Interconnection – Basic Reference Model – Conventions for the definition of OSI services*

ISO/IEC 19505 (all parts), *Information technology – Object Management Group Unified Modeling Language (OMG UML)*

ISO 1177, *Information processing – Character structure for start/stop and synchronous character oriented transmission*

IEEE Std 754-2008, *IEEE Standard for Floating-Point Arithmetic*

Internet Engineering Task Force (IETF): RFC 5905 – *Network Time Protocol Version 4: Protocol and Algorithms Specification;* available at < www.ietf.org >

3 Terms, definitions, symbols, abbreviated terms and conventions

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 61131-1 and IEC 61131-2, as well as the following apply.

3.1.1
address
part of the M-sequence control to reference data within data categories of a communication channel

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3.1.2
application layer
AL
<SDCI> part of the protocol responsible for the transmission of Process Data objects and On-Request Data objects

3.1.3
block parameter
consistent parameter access via multiple Indices or Subindices

3.1.4
checksum
<SDCI> complementary part of the overall data integrity measures in the data link layer in addition to the UART parity bit

3.1.5
CHKPDU
integrity protection data within an ISDU communication channel generated through XOR processing the octets of a request or response

3.1.6
coded switching
SDCI communication, based on the standard binary signal levels of IEC 61131-2

3.1.7
COM1
SDCI communication mode with transmission rate of 4,8 kbit/s

3.1.8
COM2
SDCI communication mode with transmission rate of 38,4 kbit/s

3.1.9
COM3
SDCI communication mode with transmission rate of 230,4 kbit/s

3.1.10
COMx
one out of three possible SDCI communication modes COM1, COM2, or COM3

3.1.11
communication channel
logical connection between Master and Device

Note 1 to entry: Four communication channels are defined: process channel, page and ISDU channel (for parameters), and diagnosis channel.

3.1.12
communication error
unexpected disturbance of the SDCI transmission protocol

3.1.13
cycle time
time to transmit an M-sequence between a Master and its Device including the following idle time

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3.1.14
Device
single passive peer to a Master such as a sensor or actuator

Note 1 to entry: Uppercase "Device" is used for SDCI equipment, while lowercase "device" is used in a generic manner.

3.1.15
Direct Parameters
directly (page) addressed parameters transferred acyclically via the page communication channel without acknowledgement

3.1.16
dynamic parameter
part of a Device's parameter set defined by on-board user interfaces such as teach-in buttons or control panels in addition to the static parameters

3.1.17
Event
instance of a change of conditions in a Device

Note 1 to entry: Uppercase "Event" is used for SDCI Events, while lowercase "event" is used in a generic manner.

Note 2 to entry: An Event is indicated via the Event flag within the Device's status cyclic information, then acyclic transfer of Event data (typically diagnosis information) is conveyed through the diagnosis communication channel.

3.1.18
fallback
transition of a port from coded switching to switching signal mode

3.1.19
inspection level
degree of verification for the Device identity

3.1.20
interleave
segmented cyclic data exchange for Process Data with more than 2 octets through subsequent cycles

3.1.21
ISDU
indexed service data unit used for acyclic acknowledged transmission of parameters that can be segmented in a number of M-sequences

3.1.22
legacy Device or Master
Device or Master designed in accordance with [8][3]

3.1.23
M-sequence
sequence of two messages comprising a Master message and its subsequent Device message

3.1.24
M-sequence control
first octet in a Master message indicating the read/write operation, the type of the communication channel, and the address, for example offset or flow control

[3] Numbers in square brackets refer to the Bibliography.

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3.1.25
M-sequence error
unexpected or wrong message content, or no response

3.1.26
M-sequence type
one particular M-sequence format out of a set of specified M-sequence formats

3.1.27
Master
active peer connected through ports to one up to n Devices and which provides an interface to the gateway to the upper level communication systems or PLCs

Note 1 to entry: Uppercase "Master" is used for SDCI equipment, while lowercase "master" is used in a generic manner.

3.1.28
message
<SDCI> sequence of UART frames transferred either from a Master to its Device or vice versa following the rules of the SDCI protocol

3.1.29
On-request Data
acyclically transmitted data upon request of the Master application consisting of parameters or Event data

3.1.30
physical layer
first layer of the ISO-OSI reference model, which provides the mechanical, electrical, functional and procedural means to activate, maintain, and de-activate physical connections for bit transmission between data-link entities

Note 1 to entry: Physical layer also provides means for wake-up and fallback procedures.

[SOURCE: ISO/IEC 7498-1:1994, 7.7.2, modified – text extracted from subclause, note added]

3.1.31
port
communication medium interface of the Master to one Device

3.1.32
port operating mode
state of a Master's port that can be either INACTIVE, DO, DI, FIXEDMODE, or SCANMODE

3.1.33
Process Data
input or output values from or to a discrete or continuous automation process cyclically transferred with high priority and in a configured schedule automatically after start-up of a Master

3.1.34
Process Data cycle
complete transfer of all Process Data from or to an individual Device that may comprise several cycles in case of segmentation (interleave)

3.1.35
single parameter
independent parameter access via one single Index or Subindex

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3.1.36
SIO
port operation mode in accordance with digital input and output defined in IEC 61131-2 that is established after power-up or fallback or unsuccessful communication attempts

3.1.37
static parameter
part of a Device's parameter set to be saved in a Master for the case of replacement without engineering tools

3.1.38
switching signal
binary signal from or to a Device when in SIO mode (as opposed to the "coded switching" SDCI communication)

3.1.39
system management
SM
<SDCI> means to control and coordinate the internal communication layers and the exceptions within the Master and its ports, and within each Device

3.1.40
UART frame
<SDCI> bit sequence starting with a start bit, followed by eight bits carrying a data octet, followed by an even parity bit and ending with one stop bit

3.1.41
wake-up
procedure for causing a Device to change its mode from SIO to SDCI

3.1.42
wake-up request
WURQ
physical layer service used by the Master to initiate wake-up of a Device, and put it in a receive ready state

3.2 Symbols and abbreviated terms

Δf_{DTRM}	permissible deviation from data transfer rate (measured in %)
ΔVS	power supply ripple (measured in V)
AL	application layer
BEP	bit error probability
C/Q	connection for communication (C) or switching (Q) signal (SIO)
CL_{eff}	effective total cable capacity (measured in nF)
CQ	input capacity at C/Q connection (measured in nF)
DI	digital input
DL	data link layer
DO	digital output
f_{DTR}	data transfer rate (measured in bit/s)
H/L	high/low signal at receiver output
I/O	input / output
ILL	input load current at input C/Q to $V0$ (measured in A)
IODD	IO Device Description (see 10.8)
IQ	driver current in saturated operating status ON (measured in A)

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IQH	driver current on high-side driver in saturated operating status ON (measured in A)
IQL	driver current on low-side driver in saturated operating status ON (measured in A)
$IQPK$	maximum driver current in unsaturated operating status ON (measured in A)
$IQPKH$	maximum driver current on high-side driver in unsaturated operating status ON (measured in A)
$IQPKL$	maximum driver current on low-side driver in unsaturated operating status ON (measured in A)
IQQ	quiescent current at input C/Q to $V0$ with inactive output drivers (measured in A)
IQ_{WU}	amplitude of Master's wake-up request current (measured in A)
IS	supply current at $V+$ (measured in A)
$ISIR$	current pulse supply capability at $V+$ (measured in A)
LED	light emitting diode
L-	power supply (-)
L+	power supply (+)
N24	24 V extra power supply (-)
n_{WU}	wake-up retry count
On/Off	driver's ON/OFF switching signal
OD	on-request data
OVD	signal overload detect
P24	24 V extra power supply (+)
PD	process data
PDCT	port and device configuration tool
PL	physical layer
PLC	programmable logic controller
PS	power supply (measured in V)
r	time to reach a stable level with reference to the beginning of the start bit (measured in T_{BIT})
RL_{eff}	loop resistance of cable (measured in Ω)
s	time to exit a stable level with reference to the beginning of the start bit (measured in T_{BIT})
SDCI	single-drop digital communication interface
SIO	standard input output (digital switching mode) [IEC 61131-2]
SM	system management
t_1	UART frame transfer delay on Master (measured in T_{BIT})
t_2	UART frame transfer delay on Device (measured in T_{BIT})
t_A	response delay on Device (measured in T_{BIT})
T_{BIT}	bit time (measured in s)
t_{CYC}	cycle time on M-sequence level (measured in s)
t_{DF}	fall time (measured in s)
T_{DMT}	delay time while establishing Master port communication (measured in T_{BIT})
T_{DR}	rise time (measured in s)
T_{DSIO}	delay time on device for transition to SIO mode following wake-up request (measured in s)
T_{DWU}	wake-up retry delay (measured in s)
$t_{M\text{-}sequence}$	M-sequence duration (measured in T_{BIT})
t_{idle}	idle time between two M-sequences (measured in s)
t_H	detection time for high level (measured in s)
t_L	detection time for low level (measured in s)
t_{ND}	noise suppression time (measured in s)
T_{RDL}	wake-up readiness following power ON (measured in s)
T_{REN}	receive enable (measured in s)

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T_{SD}	device detect time (measured in s)
T_{WU}	pulse duration of wake-up request (measured in s)
UART	universal asynchronous receiver transmitter
UML	Unified Modelling Language [ISO/IEC 19505]
$V+$	voltage at L+
$V0$	voltage at L-
$VD+_L$	voltage drop on the line between the L+ connections on Master and Device (measured in V)
$VD0_L$	voltage drop on the line between the L- connections on Master and Device (measured in V)
VDQ_L	voltage drop on the line between the C/Q connections on Master and Device (measured in V)
$VHYS$	hysteresis of receiver threshold voltage (measured in V)
VI	input voltage at connection C/Q with reference to $V0$ (measured in V)
VIH	input voltage range at connection C/Q for high signal (measured in V)
VIL	input voltage range at connection C/Q for low signal (measured in V)
VRQ	residual voltage on driver in saturated operating status ON (measured in V)
$VRQH$	residual voltage on high-side driver in operating status ON (measured in V)
$VRQL$	residual voltage on low-side driver in saturated operating status ON (measured in V)
VTH	threshold voltage of receiver with reference to $V0$ (measured in V)
$VTHH$	threshold voltage of receiver for safe detection of a high signal (measured in V)
$VTHL$	threshold voltage of receiver for safe detection of a low signal (measured in V)
WURQ	wake-up request pulse

3.3 Conventions

3.3.1 General

The service model, service primitives, and the diagrams shown in this standard are entirely abstract descriptions. The implementation of the services may reflect individual issues and can be different.

3.3.2 Service parameters

Service primitives are used to represent service provider/consumer interactions (ISO/IEC 10731). They convey parameters which indicate the information available in the provider/ consumer interaction. In any particular interface, not each and every parameter needs to be explicitly stated.

The service specification in this standard uses a tabular format to describe the component parameters of the service primitives. The parameters which apply to each group of service primitives are set out in tables. Each table consists of up to five columns:

1) parameter name;
2) request primitive (.req);
3) indication primitive (.ind);
4) response primitive (.rsp); and
5) confirmation primitive (.cnf).

One parameter (or component of it) is listed in each row of each table. Under the appropriate service primitive columns, a code is used to specify the type of usage of the parameter on the primitive specified in the column.

M Parameter is mandatory for the primitive.

U Parameter is a user option and can or cannot be provided depending on dynamic usage of the service user. When not provided a default value for the parameter is assumed.

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C Parameter is conditional upon other parameters or upon the environment of the service user.

– Parameter is never present.

S Parameter is a selected item.

Some entries are further qualified by items in brackets. These may be:

a) a parameter-specific constraint "(=)" indicates that the parameter is semantically equivalent to the parameter in the service primitive to its immediate left in the table;

b) an indication that some note applies to the entry "(n)" indicates that the following note "n" contains additional information related to the parameter and its use.

3.3.3 Service procedures

The procedures are defined in terms of:

- the interactions between application entities through the exchange of protocol data units; and
- the interactions between a communication layer service provider and a communication layer service consumer in the same system through the invocation of service primitives.

These procedures are applicable to instances of communication between systems which support time-constrained communications services within the communication layers.

3.3.4 Service attributes

The nature of the different (Master and Device) services is characterized by attributes. All services are defined from the view of the affected layer towards the layer above.

I Initiator of a service (towards the layer above)

R Receiver (responder) of a service (from the layer above)

3.3.5 Figures

For figures that show the structure and services of protocol layers, the following conventions are used:

- an arrow with just a service name represents both a request and the corresponding confirmation, with the request being in the direction of the arrow;
- a request without confirmation, as well as all indications and responses are labelled as such (i.e. service.req, service.ind, service.rsp).

Figure 1 shows the example of a confirmed service.

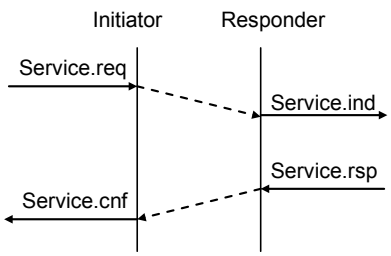

Figure 1 – Example of a confirmed service

3.3.6 Transmission octet order

Figure 2 shows how WORD based data types are transferred from memory to transmission medium and vice versa (i.e. most significant octet transmitted first, see 7.3.3.2 and 7.3.6.1).

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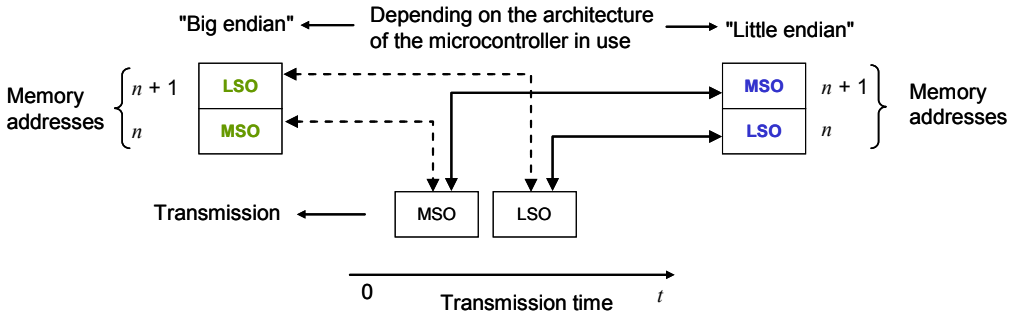


Key

MSO = Most significant octet
LSO = Least significant octet

Figure 2 – Memory storage and transmission order for WORD based data types

3.3.7 Behavioral descriptions

For the behavioral descriptions, the notations of UML 2 (ISO/IEC 19505) are used (e.g. state, sequence, activity, timing diagrams, guard conditions). The layout of the associated state-transition tables is following IEC/TR 62390.

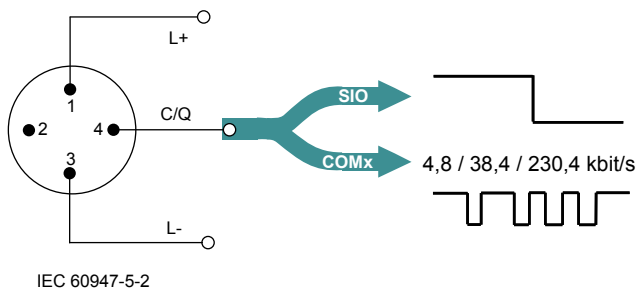
Due to design tool restrictions the following exceptions apply. For state diagrams, a service parameter (in capital letters) is attached to the service name via an underscore character, such as for example in DL_SetMode_INACTIVE. For sequence diagrams, the service primitive is attached via an underscore character instead of a dot, and the service parameter is added in parenthesis, such as for example in DL_Event_ind (OPERATE). Timing constraints are labelled "tm(time in ms)".

Asynchronously received service calls are not modelled in detail within state diagrams.

4 Overview of SDCI (IO-Link™[4])

4.1 Purpose of technology

Figure 3 shows the basic concept of SDCI.



Pin	Signal	Definition	Standard
1	L+	24 V	IEC 61131-2
2	I/Q	Not connected, DI, or DO	IEC 61131-2
3	L-	0 V	IEC 61131-2
4	Q	"Switching signal" DI, DO (SIO)	IEC 61131-2
	C	"Coded switching" (COM1, COM2, COM3)	IEC 61131-9

Figure 3 – SDCI compatibility with IEC 61131-2

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The single-drop digital communication interface technology for small sensors and actuators SDCI (commonly known as IO-Link™) defines a migration path from the existing digital input and digital output interfaces for switching 24 V Devices as defined in IEC 61131-2 towards a point-to-point communication link. Thus, for example, digital I/O modules in existing fieldbus peripherals can be replaced by SDCI Master modules providing both classic DI/DO interfaces and SDCI. Analog transmission technology can be replaced by SDCI combining its robustness, parameterization, and diagnostic features with the saving of digital/analog and analog/digital conversion efforts.

4.2 Positioning within the automation hierarchy

Figure 4 shows the domain of the SDCI technology within the automation hierarchy.

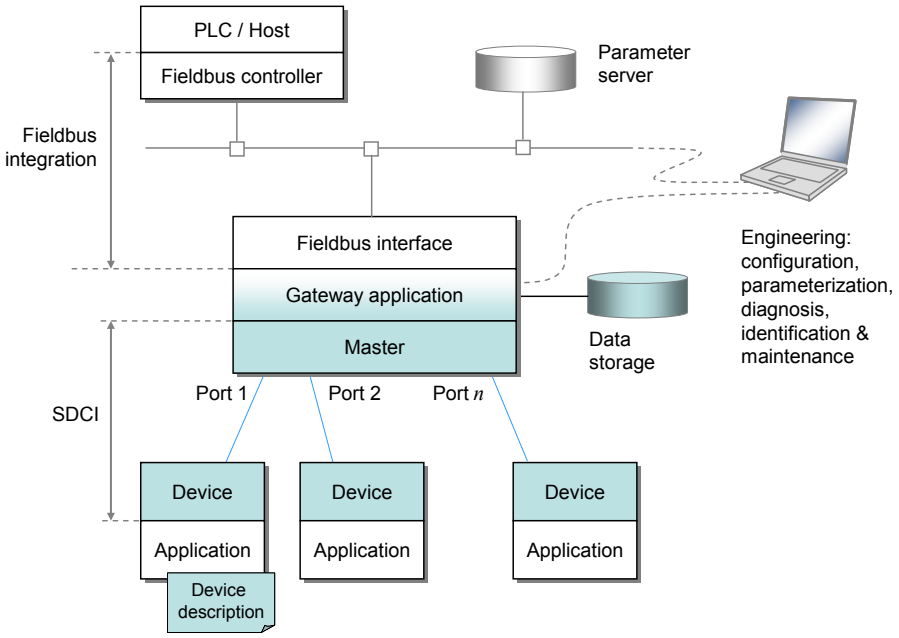

Figure 4 – Domain of the SDCI technology within the automation hierarchy

The SDCI technology defines a generic interface for connecting sensors and actuators to a Master unit, which may be combined with gateway capabilities to become a fieldbus remote I/O node.

Starting point for the design of SDCI is the classic 24 V digital input (DI) defined in IEC 61131-2 and output interface (DO) specified in Table 6. Thus, SDCI offers connectivity of classic 24 V sensors ("switching signals") as a default operational mode. Additional connectivity is provided for actuators when a port has been configured into "single-drop communication mode".

Many sensors and actuators nowadays are already equipped with microcontrollers offering a UART interface that can be extended by addition of a few hardware components and protocol software to support SDCI communication. This second operational mode uses "coded switching" of the 24 V I/O signalling line. Once activated, the SDCI mode supports parameterization, cyclic data exchange, diagnosis reporting, identification & maintenance information, and external parameter storage for Device backup and fast reload of replacement devices. Sensors and actuators with SDCI capability are referred to as "Devices" in this standard. To improve start-up performance these Devices usually provide non-volatile storage for parameters.

NOTE Configuration and parameterization of Devices is supported through an XML-based device description (see [6]), which is not part of this standard.

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4.3 Wiring, connectors and power

The default connection (port class A) comprises 4 pins (see Figure 3). The default wiring for port class A complies with IEC 60947-5-2 and uses only three wires for 24 V, 0 V, and a signal line. The fourth wire may be used as an additional signal line complying with IEC 61131-2.

Five pins connections (port class B) are specified for Devices requiring additional power from an independant 24 V power supply.

NOTE A port class A Device using the fourth wire is not compatible with a port class B Master.

Maximum length of cables is 20 m, shielding is not required.

4.4 Communication features of SDCI

The generic Device model is shown in Figure 5 and explained in the following paragraphs.

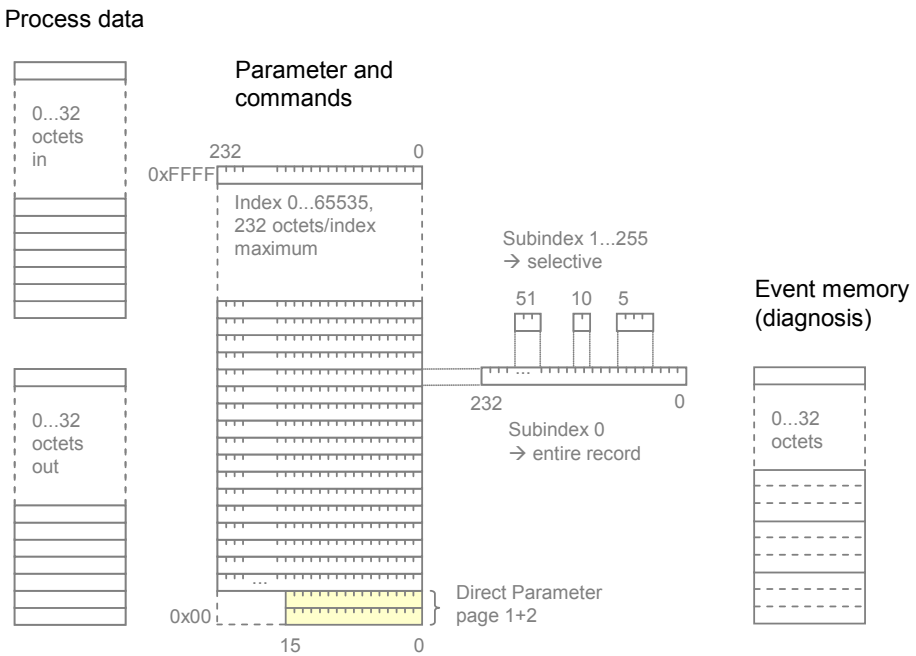

Figure 5 – Generic Device model for SDCI (Master's view)

A Device may receive Process Data (out) to control a discrete or continuous automation process or send Process Data (in) representing its current state or measurement values. The Device usually provides parameters enabling the user to configure its functions to satisfy particular needs. To support this case a large parameter space is defined with access via an Index (0 to 65 535; with a predefined organization) and a Subindex (0 to 255).

The first two index entries 0 and 1 are reserved for the Direct Parameter page 1 and 2 with a maximum of 16 octets each. Parameter page 1 is mainly dedicated to Master commands such as Device startup and fallback, retrieval of Device specific operational and identification information. Parameter page 2 allows for a maximum of 16 octets of Device specific parameters.

The other indices (2 to 65 535) each allow access to one record having a maximum size of 232 octets. Subindex 0 specifies transmission of the complete record addressed by the Index, other subindices specify transfer of selected data items within the record.

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Within a record, individual data items may start on any bit offset, and their length may range from 1 bit to 232 octets, but the total number of data items in the record cannot exceed 255. The organization of data items within a record is specified in the IO Device Description (IODD).

All changes of Device condition that require reporting or intervention are stored within an Event memory before transmission. An Event flag is then set in the cyclic data exchange to indicate the existence of an Event.

Communication between a Master and a Device is point-to-point and is based on the principle of a Master first sending a request message and then a Device sending a response message (see Figure 36). Both messages together are called an M-sequence. Several M-sequence types are defined to support user requirements for data transmission (see Figure 37).

Data of various categories are transmitted through separate communication channels within the data link layer, as shown in Figure 6.

- Operational data such as Device inputs and outputs is transmitted through a process channel using cyclic transfer. Operational data may also be associated with qualifiers such as valid/invalid.
- Configuration and maintenance parameters are transmitted using acyclic transfers. A page channel is provided for direct access to parameter pages 1 and 2, and an ISDU channel is used for accessing additional parameters and commands.
- Device events are transmitted using acyclic transfers through a diagnostic channel. Device events are reported using 3 severity levels, error, warning, and notification.

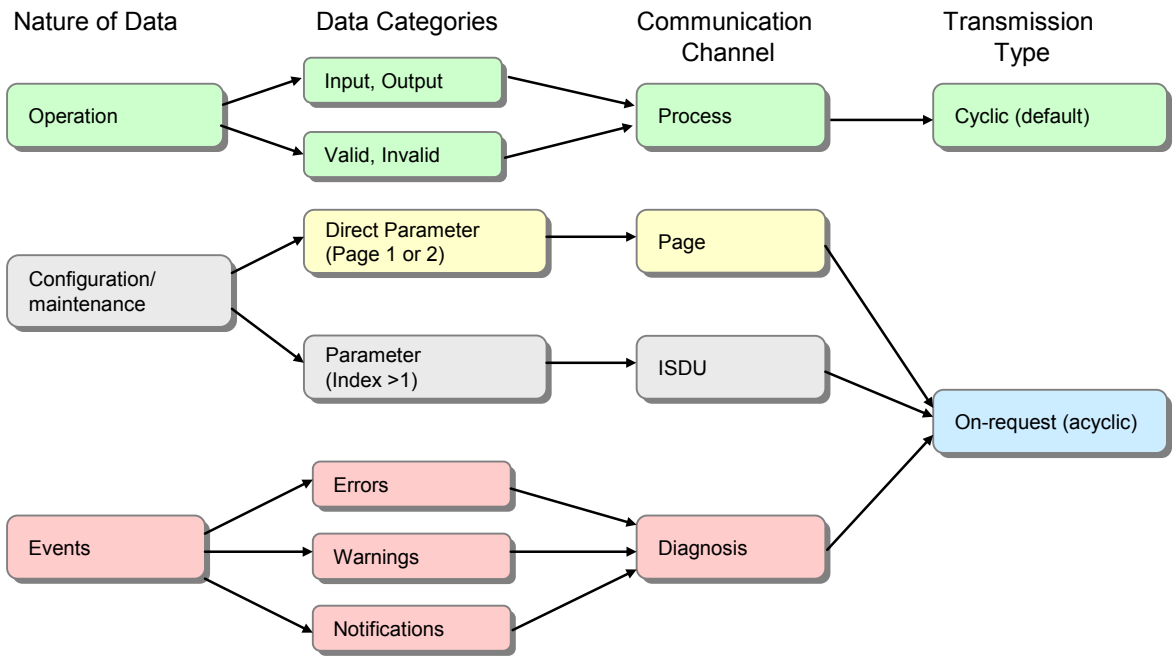

Figure 6 – Relationship between nature of data and transmission types

The first octet of a Master message controls the data transfer direction (read/write) and the type of communication channel.

Figure 7 shows each port of a Master has its own data link layer which interfaces to a common master application layer. Within the application layer, the services of the data link layer are translated into actions on Process Data objects (input/output), On-request Data objects (read/write), and events. Master applications include a Configuration Manager (CM),

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Data Storage mechanism (DS), Diagnosis Unit (DU), On-request Data Exchange (ODE), and a Process Data Exchange (PDE).

System management checks identification of the connected Devices and adjusts ports and Devices to match the chosen configuration and the properties of the connected Devices. It controls the state machines in the application (AL) and data link layers (DL), for example at start-up.

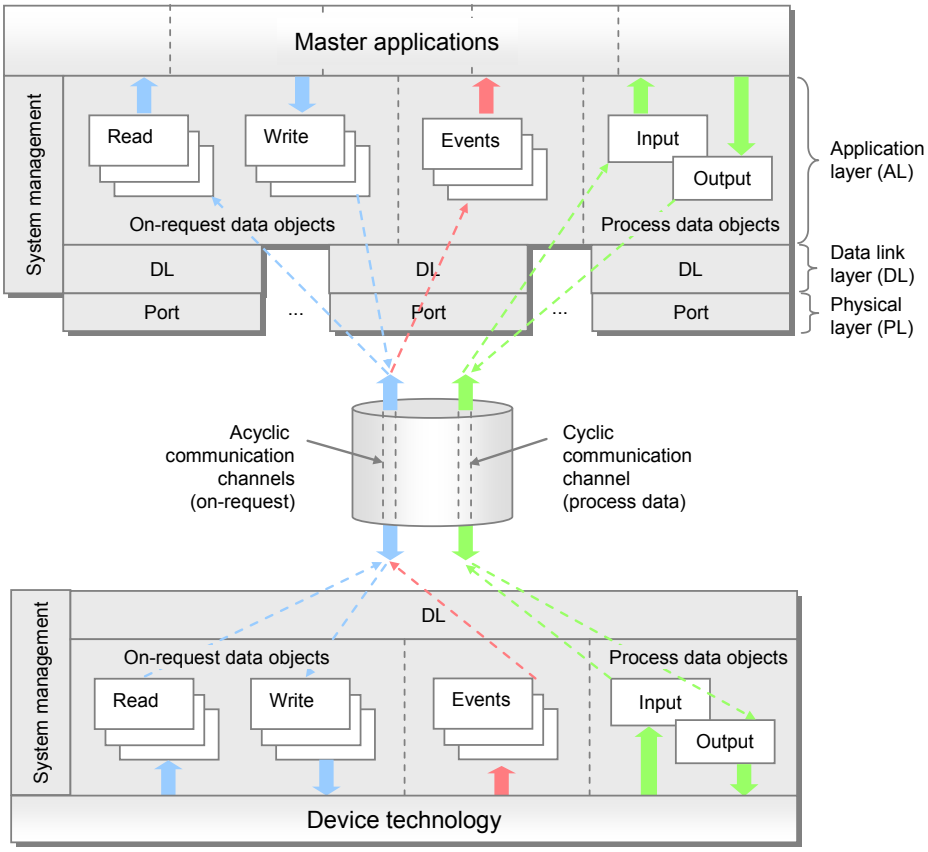

Figure 7 – Object transfer at the application layer level (AL)

4.5 Role of a Master

A Master accommodates 1 to n ports and their associated data link layers. During start-up it changes the ports to the user-selected port modes, which can be INACTIVE, DI, DO, FIXEDMODE, or SCANMODE. If communication is requested, the Master uses a special wake-up current pulse to initiate communication with the Device. The Master then auto-adjusts the transmission rate to COM1, COM2, or COM3 (see Table 8) and checks the "personality" of the connected Device, i.e. its VendorID, DeviceID, and communication properties.

If there is a mismatch between the Device parameters and the stored parameter set within the Master, the parameters in the Device are overwritten (see 11.3) or the stored parameters within the master are updated depending on configuration.

It is also possible to start a device in DI mode, switch to SDCI communication for configuration and parameterization and then use the fallback command (see 11.8.5) to switch back to DI mode for normal operation.

Coordination of the ports is also a task of the Master which the user can configure through the selection of port cycle modes. In "FreeRunning" mode, each port defines its own cycle based on the properties of the connected Device. In "MessageSync" mode, messages sent on the

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connected ports start at the same time or in a defined staggered manner. In "FixedValue" mode, each port uses a user-defined fixed cycle time (see 11.2.2.2).

The Master is responsible for the assembling and disassembling of all data from or to the Devices (see Clause 11).

The Master provides a Data Storage area of at least 2 048 octets per Device for backup of Device data (see 11.3). The Master may combine this Device data together with all other relevant data for its own operation, and make this data available for higher level applications for Master backup purpose or recipe control (see 11.8.3).

4.6 SDCI configuration

Engineering support for a Master is usually provided by a Port and Device Configuration Tool (PDCT). The PDCT configures both port properties and Device properties (see parameters shown in Figure 5). It combines both an interpreter of the I/O Device Description (IODD) and a configurator (see 11.7). The IODD provides all the necessary properties to establish communication and the necessary parameters and their boundaries to establish the desired function of a sensor or actuator. The PDCT also supports the compilation of the Process Data for propagation on the fieldbus and vice versa.

4.7 Mapping to fieldbuses

Integration of a Master within a fieldbus system, i.e. the definition of gateway fuctions for exchanging data with higher level entities on a fieldbus, is out of the scope of this standard.

EXAMPLE These functions include mapping of the Process Data exchange, realization of program-controlled parameterization or a remote parameter server, or the propagation of diagnosis information.

The integration of a PDCT into engineering tools of a particular fieldbus is out of the scope of this standard.

4.8 Standard structure

Figure 8 shows the logical structure of the Master and Device. Clause 5 specifies the Physical Layer (PL) of SDCI, Clause 6 specifies details of the SIO mode. Clause 7 specifies Data Link Layer (DL) services, protocol, wake-up, M-sequences, and the DL layer handlers. Clause 8 specifies the services and the protocol of the Application Layer (AL) and Clause 9 the System Management responsibilities (SM).

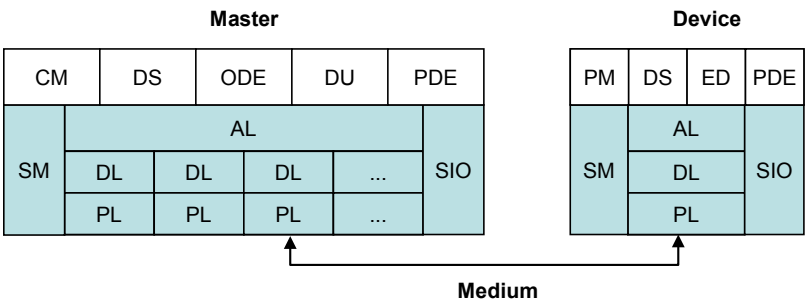

Figure 8 – Logical structure of Master and Device

Clause 10 specifies Device applications and features. These include Process Data Exchange (PDE), Parameter Management (PM), Data Storage (DS), and Event Dispatcher (ED). Technology specific applications are not part of this standard. They may be specified in profiles for particular Device families.

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Clause 11 specifies Master applications and features. These include Process Data Exchange (PDE), On-request Data Exchange (ODE), Configuration Management (CM), Data Storage (DS) and Diagnosis Unit (DU).

Several normative and informative annexes are included. Annex A defines the available M-sequence types. Annex B describes the parameters of the Direct Parameter page and the fixed Device parameters. Annex C lists the error types in case of acyclic transmissions and Annex D the EventCodes (diagnosis information of Devices). Annex E specifies the available basic and composite data types. Annex F defines the structure of Data Storage objects. Annex G deals with conformity and electromagnetic compatibility test requirements and Annex H provides graphs of residual error probabilities, demonstrating the level of SDCI's data integrity. The informative Annex I provides an example of the sequence of acyclic data transmissions. The informative Annex J explains two recommended methods for detecting parameter changes in the context of Data Storage.

5 Physical Layer (PL)

5.1 General

5.1.1 Basics

The 3-wire connection system of SDCI is based on the specifications in IEC 60947-5-2. The three lines are used as follows: (L+) for the 24 V power supply, (L-) for the ground line, and (C/Q) for the switching signal (Q) or SDCI communication (C), as shown in Figure 9.

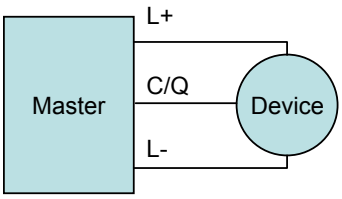

Figure 9 – Three wire connection system

NOTE 1 Binary sensors compliant with IEC 60947-5-2 are compatible with the SDCI 3-wire connection system (including from a power consumption point of view).

Support of the SDCI 3-wire connection system is mandatory for Master. Ports with this characteristic are called port class A.

Port class A uses a four pin connector. The fourth wire may be used as an additional signal line complying with IEC 61131-2. Its support is optional in both Masters and Devices.

Five wire connections (port class B) are specified for Devices requiring additional power from an independant 24 V power supply (see 5.5.1).

NOTE 2 A port class A Device using the fourth wire is not compatible with a port class B Master.

5.1.2 Topology

The SDCI system topology uses point-to-point links between a Master and its Devices as shown in Figure 10. The Master may have multiple ports for the connection of Devices. Only one Device shall be connected to each port.

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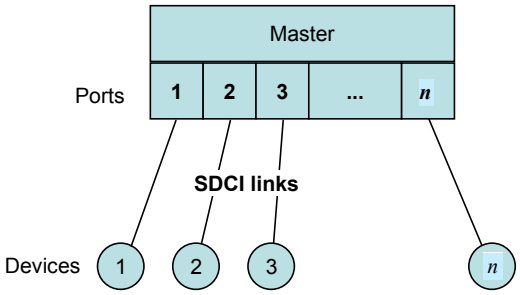

Figure 10 – Topology of SDCI

5.2 Physical layer services

5.2.1 Overview

Figure 11 shows an overview of the Master's physical layer and its service primitives.

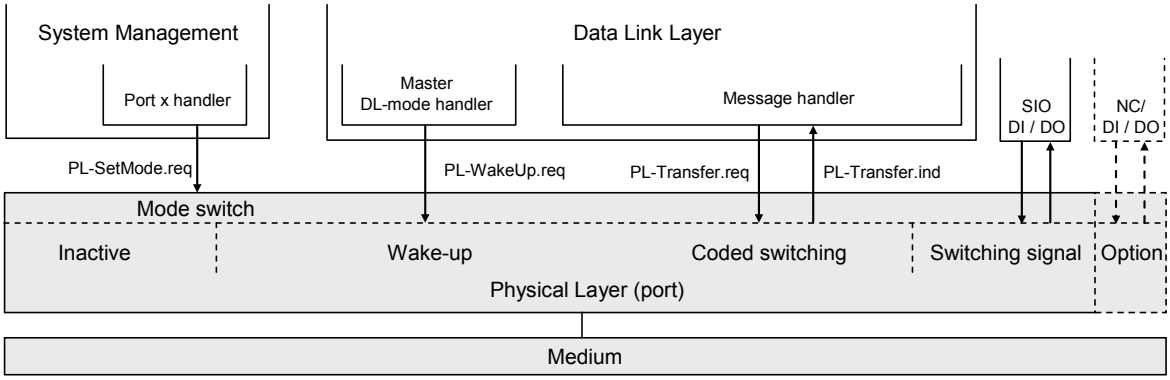

Figure 11 – Physical layer (Master)

The physical layer specifies the operation of the C/Q line in Figure 3 and the associated line driver (transmitter) and receiver of a particular port. The Master operates this line in three main modes (see Figure 11): inactive, "Switching signal" (DI/DO), or "Coded switching" (COMx). The service PL-SetMode.req is responsible for switching into one of these modes.

If the port is in inactive mode, the C/Q line shall be high impedance (floating). In SIO mode, the port can be used as a standard input or output interface according to the definitions of IEC 61131-2 or in Table 6 respectively. The communication layers of SDCI are bypassed as shown in Figure 11; the signals are directly processed within the Master application. In SDCI mode, the service PL_WakeUp.req creates a special signal pattern (current pulse) that can be detected by an SDCI enabled Device connected to this port (see 5.3.3.3).

Figure 12 shows an overview of the Device's physical layer and its service primitives.

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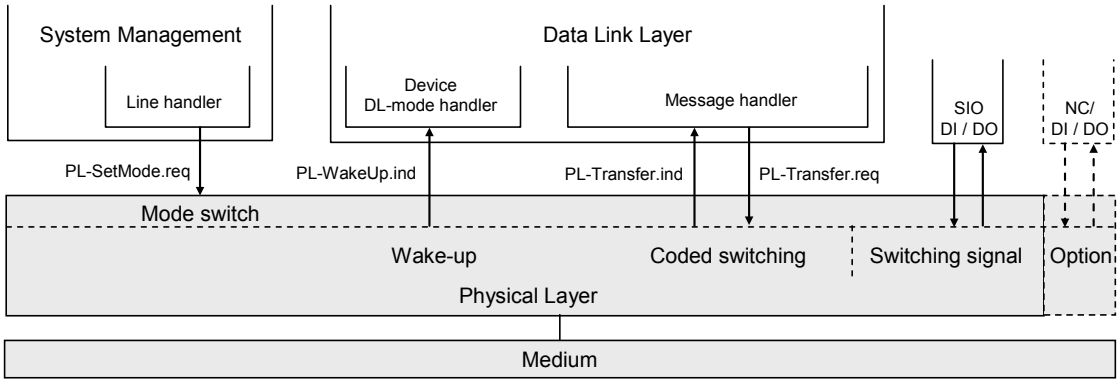

Figure 12 – Physical layer (Device)

The physical layer of a Device according to Figure 12 follows the same principle, except that there is no inactive state. By default at power on or cable reconnection, the Device shall operate in the SIO mode, as a digital input. The Device shall always be able to detect a wake-up current pulse (wake-up request). The service PL_WakeUp.ind reports successful detection of the wake-up request (usually a microcontroller interrupt), which is required for the Device to switch to the SDCI mode.

A special MasterCommand (fallback) sent via SDCI causes the Device to switch back to SIO mode.

Subsequently, the services are specified that are provided by the PL to System Management and to the Data Link Layer (see Figure 83 and Figure 94 for a complete overview of all the services). Table 1 lists the assignments of Master and Device to their roles as initiator or receiver for the individual PL services.

Table 1 – Service assignments of Master and Device

Service name	Master	Device
PL-SetMode	R	R
PL-WakeUp	R	I
PL-Transfer	I / R	R / I
Key (see 3.3.4) I Initiator of service R Receiver (Responder) of service		

5.2.2 PL services

5.2.2.1 PL_SetMode

The PL-SetMode service is used to setup the electrical characteristics and configurations of the Physical Layer. The parameters of the service primitives are listed in Table 2.

Table 2 – PL_SetMode

Parameter name	.req
Argument	M
TargetMode	M

Argument
The service-specific parameters of the service request are transmitted in the argument.

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TargetMode
This parameter indicates the requested operation mode

Permitted values:
INACTIVE (C/Q line in high impedance),
DI (C/Q line in digital input mode),
DO (C/Q line in digital output mode),
COM1 (C/Q line in COM1 mode),
COM2 (C/Q line in COM2 mode),
COM3 (C/Q line in COM3 mode)

5.2.2.2 PL_WakeUp

The PL-WakeUp service initiates or indicates a specific sequence which prepares the Physical Layer to send and receive communication requests (see 5.3.3.3). This unconfirmed service has no parameters. Its success can only be verified by a Master by attempting to communicate with the Device. The service primitives are listed in Table 3.

Table 3 – PL_WakeUp

Parameter name	.req	.ind
<none>		

5.2.2.3 PL_Transfer

The PL-Transfer service is used to exchange the SDCI data between Data Link Layer and Physical Layer. The parameters of the service primitives are listed in Table 4.

Table 4 – PL_Transfer

Parameter name	.req	ind.
Argument		
Data	M	M
Result (+)		S
Result (-)		S
Status		M

Argument
The service-specific parameters of the service request are transmitted in the argument.

Data
This parameter contains the data value which is transferred over the SDCI interface.

Permitted values: 0…255

Result (+):
This selection parameter indicates that the service request has been executed successfully.

Result (-):
This selection parameter indicates that the service request failed.

Status
This parameter contains supplementary information on the transfer status.

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Permitted values:

PARITY_ERROR	(UART detected a parity error),
FRAMING_ERROR	(invalid UART stop bit detected),
OVERRUN	(octet collision within the UART)

5.3 Transmitter/Receiver

5.3.1 Description method

The physical layer is specified by means of electrical and timing requirements. Electrical requirements specify signal levels and currents separately for Master and Device in the form of reference schematics. Timing requirements specify the signal transmission process (specifically the receiver) and a special signal detection function.

5.3.2 Electrical requirements

5.3.2.1 General

The line driver is specified by a reference schematic corresponding to Figure 13. On the Master side, a transmitter comprises a combination of two line drivers and one current sink. On the Device side, in its simplest form, the transmitter takes the form of a p-switching driver. As an option there can be an additional n-switching or non-switching driver (this also allows the option of push-pull output operation).

In operating status ON the descriptive variables are the residual voltage VRQ, the standard driver current IQ, and the peak current $IQPK$. The source is controlled by the On/Off signal. An overload current event is indicated at the “Overload” output (OVD). This feature can be used for the current pulse detection (wake-up).

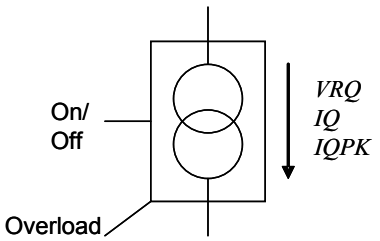

Figure 13 – Line driver reference schematics

The receiver is specified by a reference schematic according to Figure 14. It performs the function of a comparator and is specified by its switching thresholds VTH and a hysteresis $VHYS$ between the switching thresholds. The output indicates the logic level (High or Low) at the receiver input.

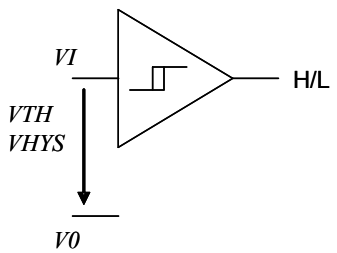

Figure 14 – Receiver reference schematics

Figure 15 shows the reference schematics for the interconnection of Master and Device for the SDCI 3-wire connection system.

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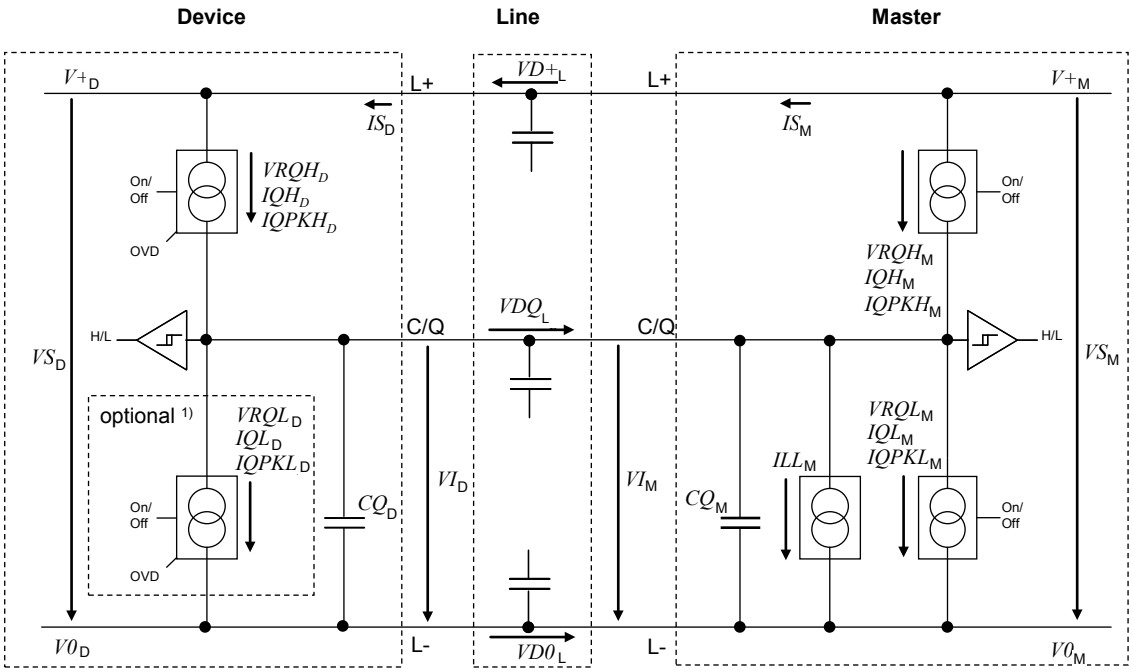

1) Optional:low-side driver (push-pull only)

Figure 15 – Reference schematics for SDCI 3-wire connection system

The subsequent illustrations and parameter tables refer to the voltage level definitions in Figure 16. The parameter indices refer to the Master (M), Device (D) or line (L). The voltage drops on the line $VD+_L$, VDQ_L and $VD0_L$ are implicitely specified in 5.5 through cable parameters.

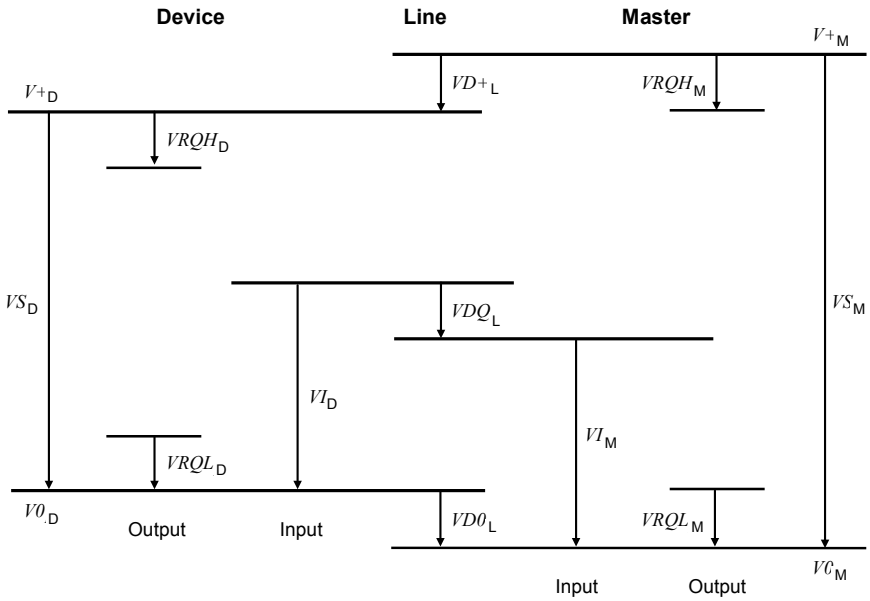

Figure 16 – Voltage level definitions

5.3.2.2 Receiver

The voltage range and switching threshold definitions are the same for Master and Device. The definitions in Table 5 apply.

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Table 5 – Electric characteristics of a receiver

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
$VTHH_{D,M}$	Input threshold 'H'	10,5	n/a	13	V	See NOTE 1
$VTHL_{D,M}$	Input threshold 'L'	8	n/a	11,5	V	See NOTE 1
$VHYS_{D,M}$	Hysteresis between input thresholds 'H' and 'L'	0	n/a	n/a	V	Shall not be negative See NOTE 2
$VIL_{D,M}$	Permissible voltage range 'L'	$V0_{D,M}$ -1,0	n/a	n/a	V	With reference to relevant negative supply voltage
$VIH_{D,M}$	Permissible voltage range 'H'	n/a	n/a	$V+_{D,M}$ + 1,0	V	With reference to relevant positive supply voltage.
NOTE 1 Thresholds are compatible with the definitions of type 1 digital inputs in IEC 61131-2. NOTE 2 Hysteresis voltage $VHYS = VTHH - VTHL$.						

Figure 17 demonstrates the switching thresholds for the detection of Low and High signals.

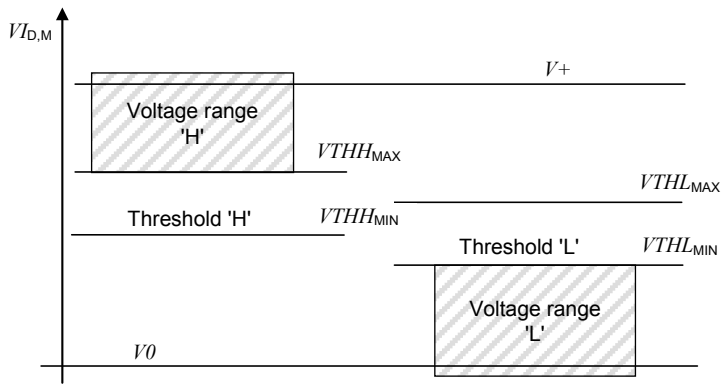

Figure 17 – Switching thresholds

5.3.2.3 Master port

The definitions in Table 6 are valid for the electric characteristics of a Master port.

Table 6 – Electric characteristics of a Master port

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
VS_M	Supply voltage for Devices	20	24	30	V	See Figure 16
IS_M	Supply current for Devices	200	n/a	n/a	mA	External supply required for > 200 mA
$ISIR_M$	Current pulse capability for Devices	400	n/a	n/a	mA	Master supply current capability for a minimum of 50 ms at 18 V after power-on of the port supply

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Property	Designation	Minimum	Typical	Maximum	Unit	Remark
ILL_M	Load or discharge current for 0 V < VI_M < 5 V 5 V < VI_M < 15 V 15 V< VI_M < 30 V	 0 5 5	 n/a n/a n/a	 15 15 15	 mA mA mA	See NOTE 1
$VRQH_M$	Residual voltage 'H'	n/a	n/a	3	V	Voltage drop relating to $V+_M$ at maximum driver current IQH_M
$VRQL_M$	Residual voltage 'L'	n/a	n/a	3	V	Voltage drop relating to $V0_M$ at maximum driver current IQL_M
IQH_M	DC driver current 'H'	100	n/a	n/a	mA	
$IQPKH_M$	Output peak current 'H'	500	n/a	n/a	mA	Absolute value See NOTE 2
IQL_M	DC driver current 'L'	100	n/a	n/a	mA	
$IQPKL_M$	Output peak current 'L'	500	n/a	n/a	mA	Absolute value See NOTE 2
CQ_M	Input capacitance	n/a	n/a	1,0	nF	f=0 MHz to 4 MHz

NOTE 1 Currents are compatible with the definition of type 1 digital inputs in IEC 61131-2. However, for the range 5 V < VI_M < 15 V, the minimum current is 5 mA instead of 2 mA in order to achieve short enough slew rates for pure p-switching Devices.

NOTE 2 Wake-up request current (5.3.3.3).

5.3.2.4 Device

The definitions in Table 7 are valid for the electric characteristics of a Device.

Table 7 – Electric characteristics of a Device

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
VS_D	Supply voltage	18	24	30	V	See Figure 16
ΔVS_D	Ripple	n/a	n/a	1,3	V_{pp}	Peak-to-peak absolute value limits shall not be exceeded. f_{ripple} = DC to 100 kHz
$VRQH_D$	Residual voltage 'H'	n/a	n/a	3	V	Voltage drop compared with $V+_D$ (IEC 60947-5-2)
$VRQL_D$	Residual voltage 'L'	n/a	n/a	3	V	Voltage drop compared with $V0_D$
IQH_D	DC driver current P-switching output ("On" state)	50	n/a	minimum ($IQPKL_M$)	mA	Minimum value due to fallback to digital input in accordance with IEC 61131-2, type 2
IQL_D	DC driver current N-switching output ("On" state)	0	n/a	minimum ($IQPKH_M$)	mA	Only for push-pull output stages
IQQ_D	Quiescent current to VO_D ("Off" state)	0	n/a	15	mA	Pull-down or residual current with deactivated output driver stages

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Property	Designation	Minimum	Typical	Maximum	Unit	Remark
CQ_D	Input capacitance	0	n/a	1,0	nF	Effective capacitance between C/Q and L+ or L- of Device in receive state

The value of 1 nF is applicable for a transmission rate of 230,4 kbit/s. Input capacitance CQ_D may be relaxed to a maximum of 10 nF in the case of push-pull stage design when operating at lower transmission rates, provided that all dynamic parameter requirements in 5.3.3.2 are met.

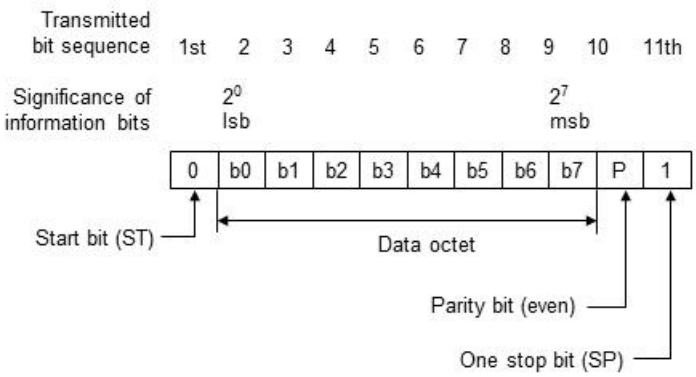
5.3.3 Timing requirements

5.3.3.1 Transmission method

The “Non Return to Zero” (NRZ) modulation is used for the bit-by-bit coding. A logic value “1” corresponds to a voltage difference of 0 V between the C/Q line and L- line. A logic value "0" corresponds to a voltage difference of +24 V between the C/Q line and L- line.

The open-circuit level on the C/Q line is 0 V with reference to L-. A start bit has logic value “0”, i.e. +24 V with reference to L-.

A UART frame is used for the "data octet"-by-"data octet" coding. The format of the SDCI UART frame is a bit string structured as shown in Figure 18.



Key:
lsb least significant bit
msb most significant bit

Figure 18 – Format of an SDCI UART frame

The definition of the UART frame format is based on ISO 1177 and ISO/IEC 2022.

5.3.3.2 Transmission characteristics

The timing characteristics of transmission are demonstrated in the form of an eye diagram with the permissible signal ranges (see Figure 19). These ranges are applicable for receiver in both the Master and the Device.

Regardless of boundary conditions, the transmitter shall generate a voltage characteristic on the receiver's C/Q connection that is within the permissible range of the eye diagram.

The receiver shall detect bits as a valid signal shape within the permissible range of the eye diagram on the C/Q connection. Signal shapes in the “no detection” areas (below $VTHL_{MAX}$ or above $VTHH_{MIN}$ and within t_{ND}) shall not lead to invalid bits.

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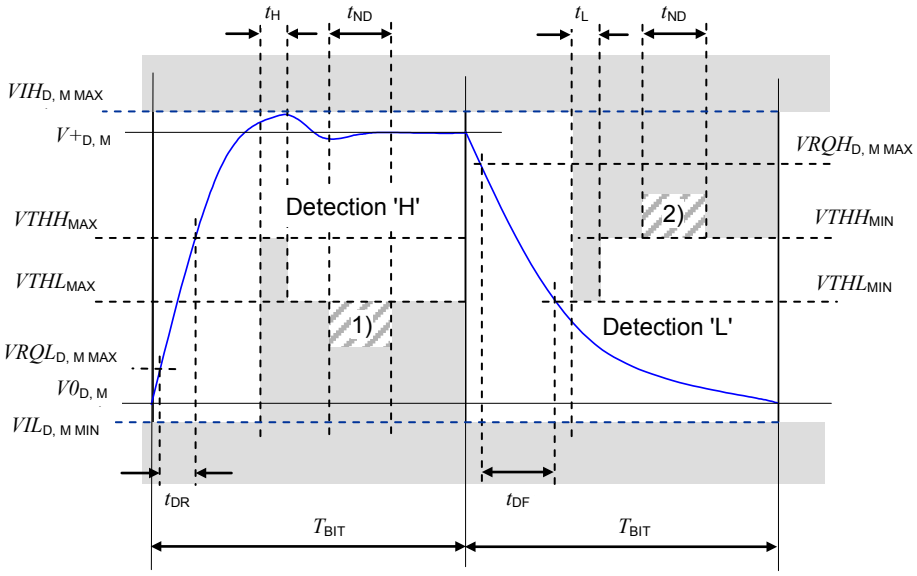

NOTE In the figure, 1) = no detection "L"; and 2) = no detection "H"

Figure 19 – Eye diagram for the 'H' and 'L' detection

In order for a UART frame to be detected correctly, a signal characteristic as demonstrated in Figure 20 is required on the receiver side. The signal delay time between the C/Q signal and the UART input shall be taken into account. Time T_{BIT} always indicates the receiver's bit rate.

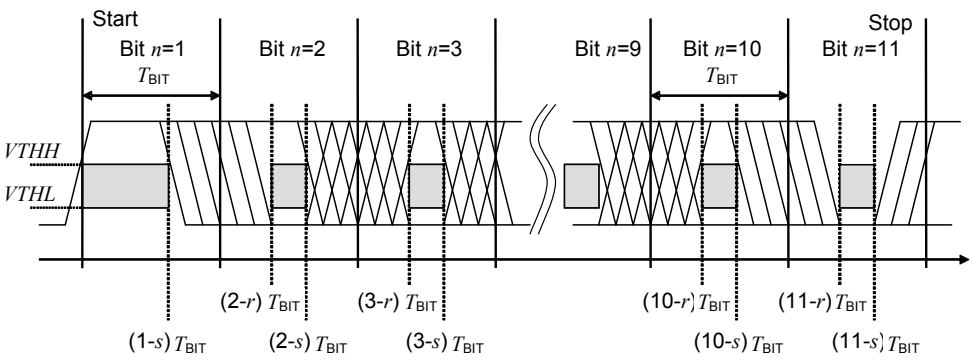

Figure 20 – Eye diagram for the correct detection of a UART frame

For every bit n in the bit sequence (n =1…11) of a UART frame, the time $(n\text{-}r)T_{BIT}$ (see Table 8 for values of r) designates the time at the end of which a correct level shall be reached in the 'H' or 'L' ranges as demonstrated in the eye diagram in Figure 19. The time (n-s) $TBIT$ (see Table 8 for values of s) describes the time, which shall elapse before the level changes. Reference shall always be made to the eye diagram in Figure 19, where signal characteristics within a bit time are concerned.

This representation permits a variable weighting of the influence parameters "transmission rate accuracy", "bit-width distortion", and "slew rate" of the receiver.

Table 8 specifies the dynamic characteristics of the transmission.

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Table 8 – Dynamic characteristics of the transmission

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
f_{DTR}	transmission rate	n/a	4,8 38,4 230,4	n/a	kbit/s	COM1 COM2 COM3
T_{BIT}	Bit time at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s		 208,33 26,04 4,34		 µs µs µs	
Δf_{DTRM}	Master transmission rate accuracy at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s	-0,1 -0,1 -0,1	n/a n/a n/a	+0,1 +0,1 +0,1	% % %	Tolerance of the transmission rate of the Master $\Delta T_{BIT}/T_{BIT}$
r	Start of detection time within a bit with reference to the raising edge of the start bit	0,65	n/a	n/a	-	Calculated in each case from the end of a bit at a UART sampling rate of 8
s	End of detection time within a bit with reference to the raising edge of the start bit	n/a	n/a	0,22	-	Calculated in each case from the end of a bit at a UART sampling rate of 8
T_{DR}	Rise time at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s	0 0 0 0	n/a n/a n/a n/a	0,20 41,7 5,2 869	T_{BIT} µs µs ns	With reference to the bit time unit
t_{DF}	Fall time at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s	0 0 0 0	n/a n/a n/a n/a	0,20 41,7 5,2 869	T_{BIT} µs µs ns	With reference to the bit time unit
t_{ND}	Noise suppression time	n/a	n/a	1/16	T_{BIT}	Permissible duration of a receive signal above/below the detection threshold without detection taking place
t_H	Detection time High	1/16	n/a	n/a	T_{BIT}	Duration of a receive signal above the detection threshold for 'H' level
t_L	Detection time Low	1/16	n/a	n/a	T_{BIT}	Duration of a receive signal below the detection threshold for 'H' level

The parameters 'r' and 's' apply to the respective Master or Device receiver side. This definition allows for a more flexible definition of oscillator accuracy, bit distortion and slewrate on the Device side. The over-all bit-width distortion on the last bit of the UART frame shall provide a correct level in the range of Figure 20.

5.3.3.3 Wake-up current pulse

The wake-up feature is used to request that a Device goes to the COMx mode.

A service call (PL_WakeUp.req) from the DL initiates the wake-up process (see 5.2.2.2).

The wake-up request (WURQ) starts with a current pulse induced by the Master (port) for a time T_{WU}. The wake-up request comprises the following phases (see Figure 21):

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a) Injection of a current IQ_{WU} by the Master depending on the level of the C/Q connection. For an input signal equivalent to logic "1" this is a current source; for an input signal equivalent to logic "0" this is a current sink.

b) Delay time of the Device until it is ready to receive.

The wake-up request pulse can be detected by the Device through a voltage change on the C/Q line or evaluation of the current of the respective driver element within the time T_{WU}. Figure 21 shows examples for Devices with low output power.

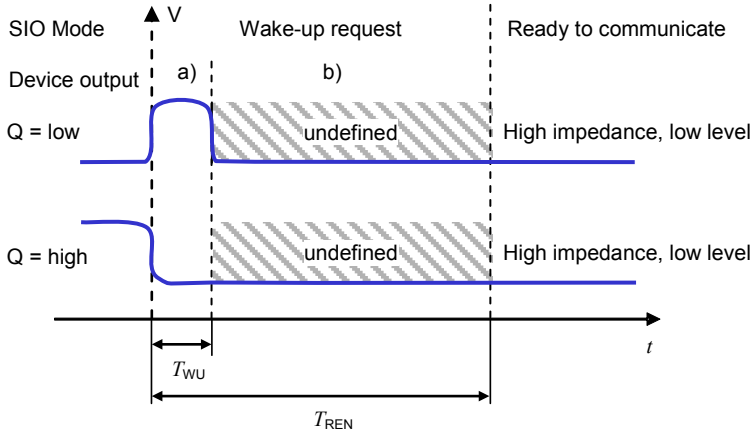

Figure 21 – Wake-up request

Table 9 specifies the current and timing properties associated with the wake-up request. See Table 6 for values of $IQPKL_M$ and $IQPKH_M$.

Table 9 – Wake-up request characteristics

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
IQ_{WU}	Amplitude of Master's wake-up current pulse	$IQPKL_M$ or $IQPKH_M$	n/a	n/a	mA	Current pulse followed by switching status of Device
T_{WU}	Duration of Master's wake-up current pulse	75	n/a	85	µs	Master property
T_{REN}	Receive enable delay	n/a	n/a	500	µs	Device property

5.4 Power supply

5.4.1 Power supply options

The SDCI connection system provides dedicated power lines in addition to the signal line. The communication section of a Device shall always be powered by the Master using the power lines defined in the 3-wire connection system (Power1).

The maximum supply current available from a Master port is specified in Table 6.

The application part of the device may be powered in one of three ways:

- via the power lines of the SDCI 3-wire connection system (class A ports), using Power1;
- via the extra power lines of the SDCI 5-wire connection system (class B ports), using an extra power supply at the Master (Power2);

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- via a local power supply at the Device (design specific).

Port class A allows power consumption of up to 200 mA, as specified in Table 6. Maximum power consumption on port class B depends on the selected connection method. M12 only allows up to an extra 3,5 A.

5.4.2 Power-on requirements

Figure 22 shows how the power-on behavior of a Device is defined by the ramp-up time of the Power1 supply and by the Device internal time to get ready for the wake-up operation.

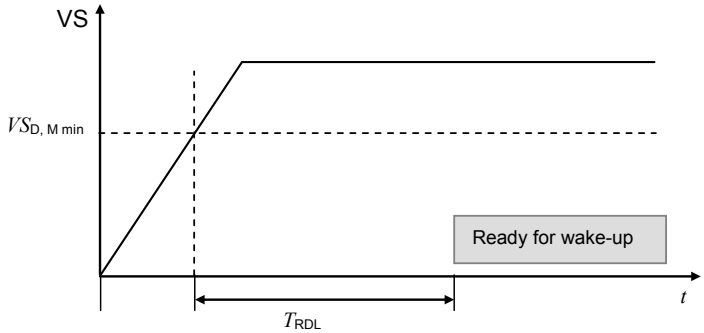

Figure 22 – Power-on timing for Power1

Upon power-on it is mandatory for a Device to reach the wake-up ready state within the time limits specified in Table 10.

Table 10 – Power-on timing

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
T_{RDL}	Wake-up readiness following power-on	n/a	n/a	300	ms	Device ramp-up time until it is ready for wake-up signal detection (See NOTE)
NOTE Equivalent to the time delay before availability in IEC 60947-5-2.						

5.5 Medium

5.5.1 Connectors

The Master and Device pin assignment is based on the specifications in IEC 60947-5-2, with extensions specified in the paragraphs below. Ports class A use M5, M8, and M12 connectors, with a maximum of four pins. Ports class B only use M12 connectors with 5 pins. M12 connectors are mechanically A-coded according to IEC 61076-2-101.

NOTE For legacy or compatibility reasons, direct wiring or different types of connectors can be used instead, provided that they do not violate the electrical characteristics and use signal naming specified in this standard.

Female connectors are assigned to the Master and male connectors to the Device. Table 11 lists the pin assignments and Figure 23 shows the layout and mechanical coding for M12, M8, and M5 connections.

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Table 11 – Pin assignments

Pin	Signal	Designation	Remark
1	L+	Power supply (+)	See Table 7
2	I/Q P24	NC/DI/DO (port class A) P24 (port class B)	Option 1: NC (not connected) Option 2: DI Option 3: DI, then configured DO Option 4: Extra power supply for power Devices (port class B)
3	L-	Power supply (-)	See Table 7
4	C/Q	SIO/SDCI	Standard I/O mode (DI/DO) or SDCI (see Table 6 for electrical characteristics of DO).
5	NC N24	NC (port class A) N24 (port class B)	Option 1: Shall not be connected on the Master side (port class A). Option 2: Reference to the extra power supply (port class B)
NOTE M12 is always a 5 pin version on the Master side (female).			

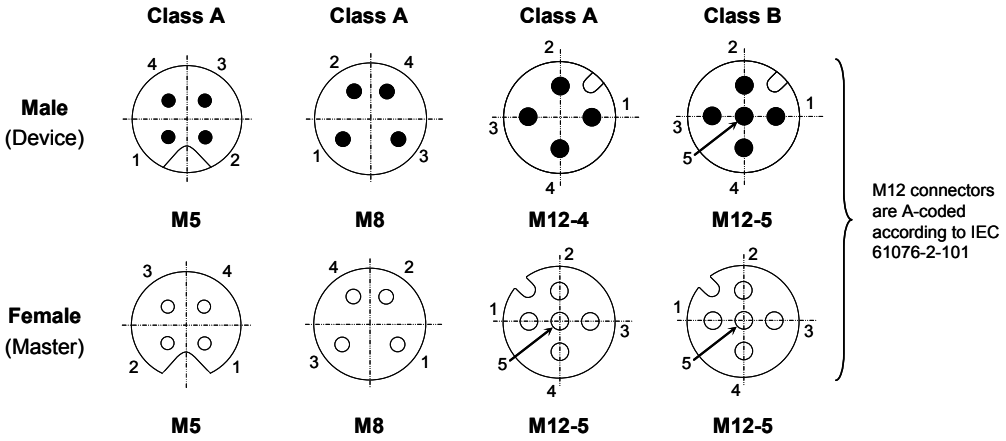

Figure 23 – Pin layout front view

Figure 24 shows the layout of the two port classes A and B. Class B ports shall be marked to distinguish them from Class A ports, because of risks deriving from incompatibilities.

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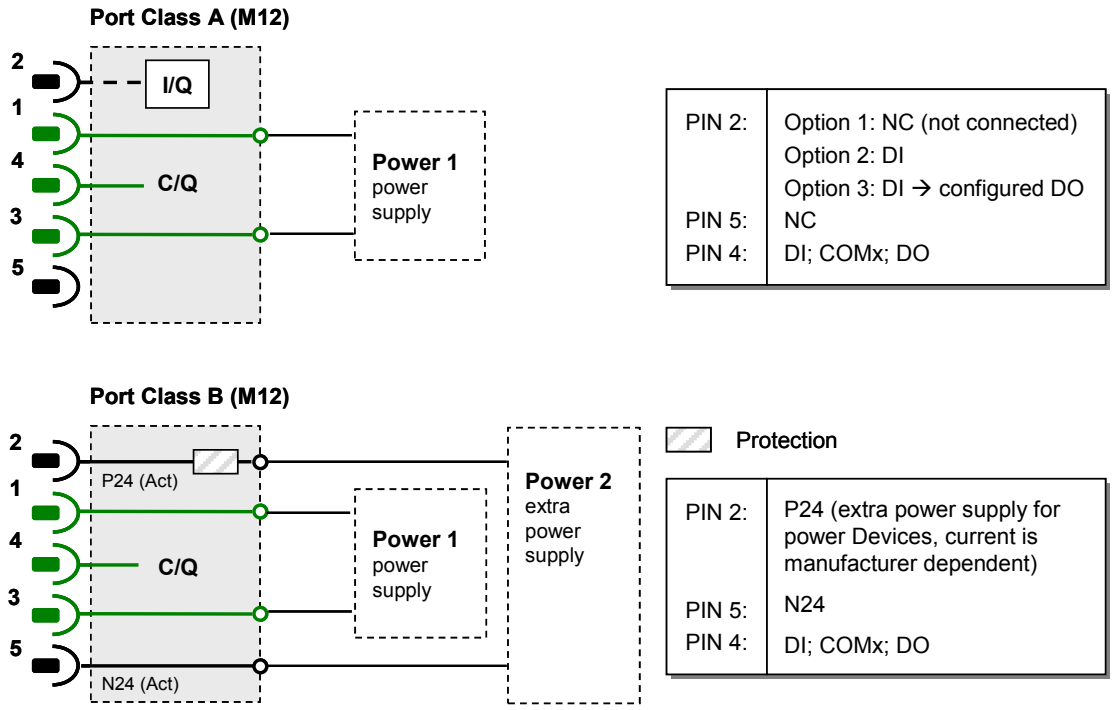

Figure 24 – Class A and B port definitions

5.5.2 Cable

The transmission medium for SDCI communication is a multi-wired cable with 3 or more wires. The definitions in the following paragraphs implicitly cover the static voltage definitions in Table 5 and Figure 16. To ensure functional reliability, the cable properties shall comply with Table 12.

Table 12 – Cable characteristics

Property	Minimum	Typical	Maximum	Unit
Length	0	n/a	20	m
Overall loop resistance RL_{eff}	n/a	n/a	6,0	Ω
Effective line capacitance CL_{eff}	n/a	n/a	3,0	nF (<1 MHz)

The loop resistance RL_{eff} and the effective line capacitance CL_{eff} may be measured as demonstrated in Figure 25.

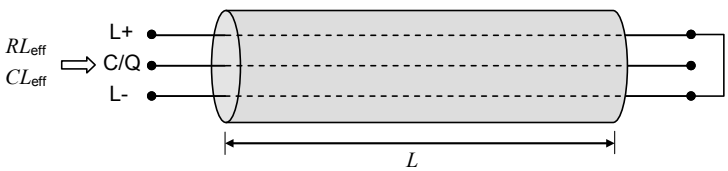

Figure 25 – Reference schematic for effective line capacitance and loop resistance

Table 13 shows the cable conductors and their assigned color codes.

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Table 13 – Cable conductor assignments

Signal	Designation	Color	Remark
L-	Power supply (-)	Blue[a]	SDCI 3-wire connection system
C/Q	Communication signal	Black[a]	SDCI 3-wire connection system
L+	Power supply (+)	Brown[a]	SDCI 3-wire connection system
I/Q	DI or DO	White[a]	Optional
P24	Extra power supply (+)	Any other	Optional
N24	Extra power supply (-)	Any other	Optional
[a] Corresponding to IEC 60947-5-2			

6 Standard Input and Output (SIO)

Figure 83 and Figure 94 demonstrate how the SIO mode allows a Device to bypass the SDCI communication layers and to map the DI or DO signal directly into the data exchange message of the higher level fieldbus or system. Changing between the SDCI and SIO mode is defined by the user configuration or implicitly by the services of the Master applications. The system management takes care of the corresponding initialization or deactivation of the SDCI communication layers and the physical layer (mode switch). The characteristics of the interfaces for the DI and DO signals are derived from the caracteristics specified in IEC 61131-2 for type 1.

7 Data link layer (DL)

7.1 General

The data link layers of SDCI are concerned with the delivery of messages between a Master and a Device across the physical link. It uses several M-sequence ("message sequence") types for different data categories.

A set of DL-services is available to the application layer (AL) for the exchange of Process Data (PD) and On-request Data (OD). Another set of DL-services is available to system management (SM) for the retrieval of Device identification parameters and the setting of state machines within the DL. The DL uses PL-Services for controlling the physical layer (PL) and for exchanging UART frames. The DL takes care of the error detection of messages (whether internal or reported from the PL) and the appropriate remedial measures (e.g. retry).

The data link layers are structured due to the nature of the data categories into Process Data handlers and On-request Data handlers which are in turn using a message handler to deal with the requested transmission of messages. The special modes of Master ports such as wake-up, COMx, and SIO (disable communication) require a dedicated DL-mode handler within the Master DL. The special wake-up signal modulation requires signal detection on the Device side and thus a DL-mode handler within the Device DL. Each handler comprises its own state machine.

The data link layer is subdivided in a DL-A section with its own internal services and a DL-B section with the external services.

The DL uses additional internal administrative calls between the handlers which are defined in the "internal items" section of the associated state-transition tables.

Figure 26 shows an overview of the structure and the services of the Master's data link layer.

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