

Australian/New Zealand Standard™

**Low-voltage switchgear and
controlgear—Controller-device
interfaces (CDIs)**

Part 2: Actuator sensor interface (AS-i)



Standards Australia



AS/NZS 62026.2:2001

This Joint Australian/New Zealand Standard was prepared by Joint Technical Committee EL-006, Industrial Switchgear and Controlgear. It was approved on behalf of the Council of Standards Australia on 21 March 2001 and on behalf of the Council of Standards New Zealand on 4 May 2001. It was published on 28 May 2001.

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Australian/New Zealand Standard™

Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)

Part 2: Actuator sensor interface (AS-i)

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PREFACE

This Standard was prepared by the Joint Standards Australia/Standards New Zealand Committee EL-006, Industrial Switchgear and Controlgear.

The objective of this Standard is to define the requirements for interfaces between a slave, a master and electromechanical structures, normal service conditions for slaves, electromechanical devices and masters, constructional and performance requirements and tests to verify conformance to requirements.

This Standard is Part 2 of a series which, when complete, will consist of the following:

AS/NZS

62026 Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)

62026.1 Part 1: General rules

62026.2 Part 2: Actuator sensor interface (AS-i) (This Standard)

62026.3 Part 3: DeviceNet

62026.5 Part 5: Smart distributed system (SDS)

62026.6 Part 6: Seriplex (Serial multiplexed control Bus)

This Standard is identical with and has been reproduced from IEC 62026-2:2000, *Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)—Part 2: Actuator sensor interface (AS-i)*.

This Standard covers interfaces between low-voltage switchgear and controlgear switching elements and controllers (e.g. programmable controllers, personal computers, etc.).

The provisions of the general rules in AS/NZS 62026.1 are applicable to this Joint Australian/New Zealand Standard, where specifically called for. General rules clauses and subclauses thus applicable, as well as tables, figures and annexes, are identified by reference to Part 1 of the IEC Standard from which this Standard is reproduced, for example subclause 7.2.4.1 of IEC 62026-1.

Where inputs and outputs (I/O) are described in this Standard, their meaning is regarding the master, the meaning regarding the application is the opposite.

Clauses 1 to 8 contain the general requirements. Clause 9 contains the test specifications. Specific requirements for the various profiles of actuators, sensors, masters, etc. are given in the relevant annexes.

A reference to an International Standard identified in the Normative References Clause by ~~striketthrough (example)~~ is replaced by a reference to the Australian or Australian/New Zealand Standard(s) listed immediately thereafter and identified by shading (example). Where the struck-through referenced document and the referenced Australian or Australian/New Zealand Standard are identical, this is indicated in parenthesis after the title of the latter.

As this Standard is reproduced from an International Standard, the following applies:

- (a) Its number does not appear on each page of text and its identity is shown only on the cover and title page.
- (b) In the source text 'this standard' should read 'this Australian/New Zealand Standard'.
- (c) A full point should be substituted for a comma when referring to a decimal marker.

The term 'normative' has been used in this Standard to define the application of the annex to which it applies. A 'normative' annex is an integral part of a Standard.

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Australian/New Zealand Standard**Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)****Part 2: Actuator sensor interface (AS-i)**

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1 Scope

This International Standard applies to interfaces between low-voltage switchgear and controlgear switching elements, and controllers (e.g. programmable controllers, personal computers, etc.).

This standard specifies a bit-oriented interface-system between a single control circuit device and switching elements, connected by a nonshielded, untwisted two-wire cable, carrying data and power, and establishes a system for the interchangeability of components with such interfaces.

The object of this standard is to define, for such interfaces:

- requirements for interfaces between a slave, a master and electromechanical structures;
- normal service conditions for slaves, electromechanical devices and masters;
- constructional and performance requirements;
- tests to verify conformance to requirements.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

References to International Standards that are struck through in this Clause are replaced by references to equivalent Australian or Australian/New Zealand Standards that are listed immediately thereafter and identified by shading. Any Australian or Australian/New Zealand Standard that is identical to the International Standard it replaces is appropriately identified.

CISPR 11:1997, *Industrial, scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement*

IEC 60364-4-41:1992, *Electrical installations of buildings – Part 4: Protection for safety – Chapter 41: Protection against electric shock*

~~IEC 60947-1:1999, *Low-voltage switchgear and controlgear – Part 1: General rules*~~

AS/NZS 3947.1, *Low-voltage switchgear and controlgear, Part 1: General rules*

~~IEC 60947-5-2:1997, *Low-voltage switchgear and controlgear – Part 5-2: Control circuit devices and switching elements – Proximity switches*~~

AS/NZS 3947.5.2, *Low-voltage switchgear and controlgear, Part 5.2: Control circuit devices and switching elements—Proximity switches* (identical to IEC 60947-5-2:1997 including Amd.1:1999)

~~IEC 60998-2-3:1991, *Connecting devices for low-voltage circuits for household and similar purposes – Part 2-3: Particular requirements for connecting devices as separate entities with insulation piercing clamping units*~~

AS/NZS 60998.2.3, *Connecting devices for low-voltage circuits for household and similar purposes, Part 2.3: Particular requirements for connecting devices as separate entities with insulation piercing clamping units*

IEC 61000-4-2:1995, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*. Basic EMC publication

~~IEC 61000-4-3:1995, *Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques – Radiated, radio-frequency, electromagnetic field immunity test*~~

AS/NZS 61000.4.3, *Electromagnetic compatibility (EMC), Part 4.3: Testing and measurement techniques—Radiated, radio-frequency, electromagnetic field immunity test*

IEC 61000-4-4:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 4: Electrical fast transient/burst immunity test*. Basic EMC publication

IEC 61000-6-2:1999, *Electromagnetic compatibility (EMC) – Part 6-2: Generic standards – Immunity for industrial environments*

IEC 61131-2:1992, *Programmable controllers – Part 2: Equipment requirements and tests*

~~IEC 62026-1:2000, *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 1: General rules*~~

AS/NZS 62026.1, *Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs) , Part 1: General rules* (identical to IEC 62026-1:2000)

3 Definitions, symbols and abbreviations

Alphabetical index of definitions

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3.1 Definitions

For the purpose of this International Standard, clause 3 of IEC 62026-1 applies with the following additions.

3.1.1

active slave

slave connected to the AS-i line and capable of communicating properly

3.1.2

Actuator Sensor interface (AS-i)

set of interfaces and serial communication method for the connection of low-voltage switchgear, controlgear and other simple devices with a controller

3.1.3

address

numerical parameter between 0 and 31 which specifies a node of an AS-i network

NOTE Address 0 is reserved for slaves which have not had an address assigned.

3.1.4

address assignment

replacement of the existing address of the AS-i slave with a new address

3.1.5

AS-i cycle

set of up to 33 transactions

NOTE A transaction may, in case of a detected fault, include one master request or slave response retransmission.

3.1.6**AS-i input**

physical (external) or logical (internal) slave input port (see figure 1)

3.1.7**AS-i line**

two-wire cable utilized by AS-i slaves and the AS-i master for transferring information and power

3.1.8**AS-i master**

unit on the AS-i line that manages the communication between the slaves and the controller

3.1.9**AS-i network**

network composed of AS-i master, slaves, power supply and line

3.1.10**AS-i output**

physical (external) or logical (internal) slave output port (see figure 1)

3.1.11**AS-i power supply**

combined d.c. supply and decoupling circuit needed for an AS-i network

3.1.12**AS-i slave**

physical and logical means to connect the application devices (actuator, sensor or other components) to the AS-i line

NOTE A slave may be a stand alone device or part of another device.

3.1.13**bit time (effective) (T_{bit})**

duration of the transmission of one bit

3.1.14**decoupling circuit**

part of the AS-i power supply for decoupling the d.c. source and for conditioning the physical data transmission within the AS-i network

3.1.15**field devices**

items connected to the AS-i slave, for example actuators, sensors, push-buttons, indicator lights, etc.

NOTE "Intelligent" field devices also include integrated AS-i circuitry.

3.1.16**I/O configuration (I/O code)**

set of four bits which defines the direction of data flow at the four I/O ports of a slave

3.1.17**identification code (ID code)**

set of four bits which defines the type of slave profile for a given I/O configuration

3.1.18**master pause**

time between the last bit of a master request and the first bit of the slave response to the master

3.1.19**master request**

data or parameter or function sent from the master to a single slave. The content of this master request is either data (to be moved to the output ports of the slave), parameters or a command

3.1.20**non-volatile stored data**

data that remains unchanged following power interruption

3.1.21**operation address**

address of the AS-i slave other than the zero address

3.1.22**output current limit I_{Lim}**

output current of the power supply not to be exceeded under all environmental and load conditions

3.1.23**send pause**

period after receipt of the slave response during which no subsequent transmission occurs

3.1.24**slave pause**

minimum time between the last bit of a slave response and the start of the first bit of the next master request

3.1.25**slave response**

message from the slave to the master after a master request has been received and processed without error. The content of this response is either data or the result of a command

3.1.26**transaction**

combination of a master request, master pause, slave response and send pause (see figure 5)

3.1.27**volatile stored data**

data that may change following power interruption

3.1.28**zero address**

special address reserved for the online assignment of a new address to an AS-i slave

3.2 Symbols and abbreviations

APF	AS-i power failure
APM	Alternate pulse modulation
APO	AS-i power-ON
AS-i	Actuator sensor interface
T_{bit}	Bit period
TS	Transaction status
U_b	Power supply voltage
U_{send}	Peak value of the voltage pulses
$u(t)$	Pulse waveform

4 Classification

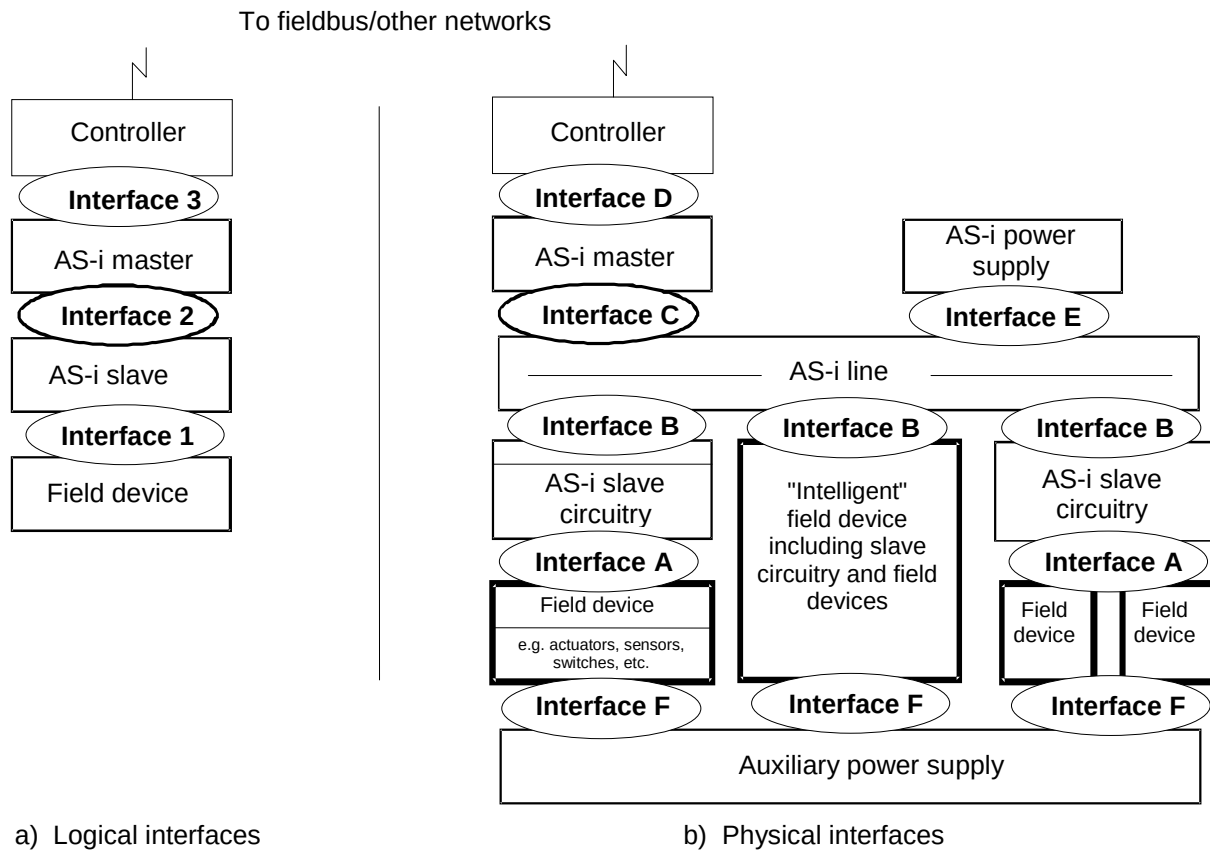
4.1 Overview

AS-i will usually be applied at the lowest level in a multi-level automation hierarchy. AS-i concentrates on the typical requirements to connect binary elements with a controller.

AS-i can be used as an interface physically integrated into field devices, for example actuators, sensors, or other devices and elements themselves, allowing the design of "intelligent" binary actuators, sensors, or other devices and elements. Alternatively, AS-i may be used in separate modules, each providing an interface for up to four conventional actuators and/or sensors or other devices and elements.

The AS-i structure contains two different types of interface, three logical and six physical, as shown in figure 1.

Logically, the AS-i system is a master-slave communication system composed of a single master and up to 31 slaves. The master sends data and parameters to each specific slave. The slave passes the data to the output ports or processes the requested procedure (e.g. reset_slave) and returns the input data or the result of the successfully processed procedure to the master.



IEC 1145/2000

Figure 1 – AS-i components and interfaces

The AS-i concept is independent of the specific field devices. It defines the mechanisms and all the components for the communication with a controller and it offers electromechanical structures for a standardized "interconnection system" for installation of actuators, sensors, or other devices and elements.

Normally, more than one standard field device may be connected via the physical interface A to the slave.

"Intelligent field devices" contain the slave circuitry, the physical interface A and the field device itself.

The annexes define profiles for common types of field devices, that will often be used in AS-i systems.

4.2 Components and interfaces

As shown in figure 1, the AS-i system deals with components, and logical and physical interfaces.

4.2.1 Components

AS-i slave

Includes the circuitry which determines the logical and functional behaviour of the unit, and which can be accessed by the master via the AS-i line for data exchange, parameterization and monitoring. It responds to a specific request from the master and it ensures that a malfunction of the attached actuator, sensor, other device or of the slave itself shall not disturb the communication between the master and the other slaves in the network.

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AS-i master	Includes the circuitry which determines the logical and functional behaviour of the unit which organizes and monitors the network, and schedules the exchange of data, parameters and commands with the AS-i slave via the AS-i line. The AS-i master sends master requests to an AS-i slave and receives slave responses from it.
AS-i power supply	Provides power to the AS-i network and includes the decoupling circuitry.
AS-i line	Provides the signalling and d.c. power connections between the AS-i devices.

4.2.2 Logical interfaces

Interface 1	The slave interface which connects the AS-i slave with the actuators, sensors, or other devices and elements. It is characterized by several ports which define the input, output or bi-directional input/output behaviour, the parameterization behaviour of the AS-i slave and the timing of the signals.
Interface 2	Provides all logical definitions required for data exchange between the AS-i master and slaves. It comprises the signalling of encoded information and the network management.
Interface 3	Provides all functions used by the controller (host) to access the AS-i master for sending and receiving data to and from slaves, sending commands to a slave, to set or to get flags and values for several lists in the master. This interface allows the controller to manage the AS-i master's behaviour and thus the behaviour of the AS-i system. Typical functions include "set_something" in the master or "get_some_information" from the master. This interface is conceptual in nature and its definition is outside the scope of this standard. The concrete representation of the interface depends on the implementation. To a large extent, it depends on the features of the specific controller system.

4.2.3 Physical interfaces

Interface A	Defines the physical connection between the field device and the AS-i slave circuitry including physical interface, signal levels and power requirements, if any.
Interface B	Defines the physical connection of the AS-i slave circuitry to the AS-i line including physical interface (mechanical/electrical), signal characteristics and power requirements.
Interface C	Defines the physical connection of the AS-i master circuitry to the AS-i line including physical interface (mechanical/electrical), signal characteristics and power requirements.
Interface D	The definition of the physical interface is outside the scope of this standard and shall be provided by the manufacturer.
Interface E	Defines the physical connection of the AS-i power supply including the signal decoupling circuit to the AS-i line.
Interface F	Defines the physical interface between the field device and an external auxiliary power supply, if any.

5 Characteristics

5.1 AS-i components

The AS-i components are described in the relevant annexes.

5.2 AS-i transmission system

5.2.1 General

The AS-i transmission system provides the communication between the AS-i slaves and the AS-i master, i.e. it represents interface 2 between a master and the slaves (see figure 1).

The AS-i system is a digital, serial, multidrop data communication with actuators and sensors including simultaneous power supply. The following specifies the transmission of data between the master and a specific slave.

5.2.2 Signal characteristics

The characteristics of the transmitted signal and the modulation are defined in this subclause.

The bit time (T_{bit}) shall be 6 μs . Thus the bit rate shall be 166 $\frac{2}{3}$ kbit/s. The maximum deviation from the nominal bit time shall not exceed $\pm 0,2 \%$.

The transmission coding and encoding principle shall be as shown in figure 2. Each master request or slave response shall include a start and an end bit. The idle state shall be represented by a "1". The Master request or slave response are encoded in Manchester II format with alternate pulse modulation (APM). The duration of each bit shall be 6 μs .

A "0" shall be encoded by a period of 3 μs high level followed by a period of 3 μs low level. A "1" shall be encoded by a period of 3 μs low level followed by a period of 3 μs high level. The transmitter shall be implemented as a current sink. The amplitude of the modulation current shall be between 55 mA and 68 mA. Together with the decoupling inductances of the decoupling circuit in the power supply, this current leads to a negative voltage pulse at each rising edge and a positive voltage pulse at each falling edge. The waveform of the pulses shall be ideally:

$$u(t) \approx \pm U_{\text{send}} \times \sin^2 \left(\frac{2\pi}{6 \mu\text{s}} t \right)$$

$$U_{\text{send}} = \text{Const} \approx 2 \text{ V (see figure 2)}$$

NOTE In a real AS-i system, the falling edge of the pulses is flattened due to the behaviour of the decoupling circuit and the physical properties of the AS-i line.

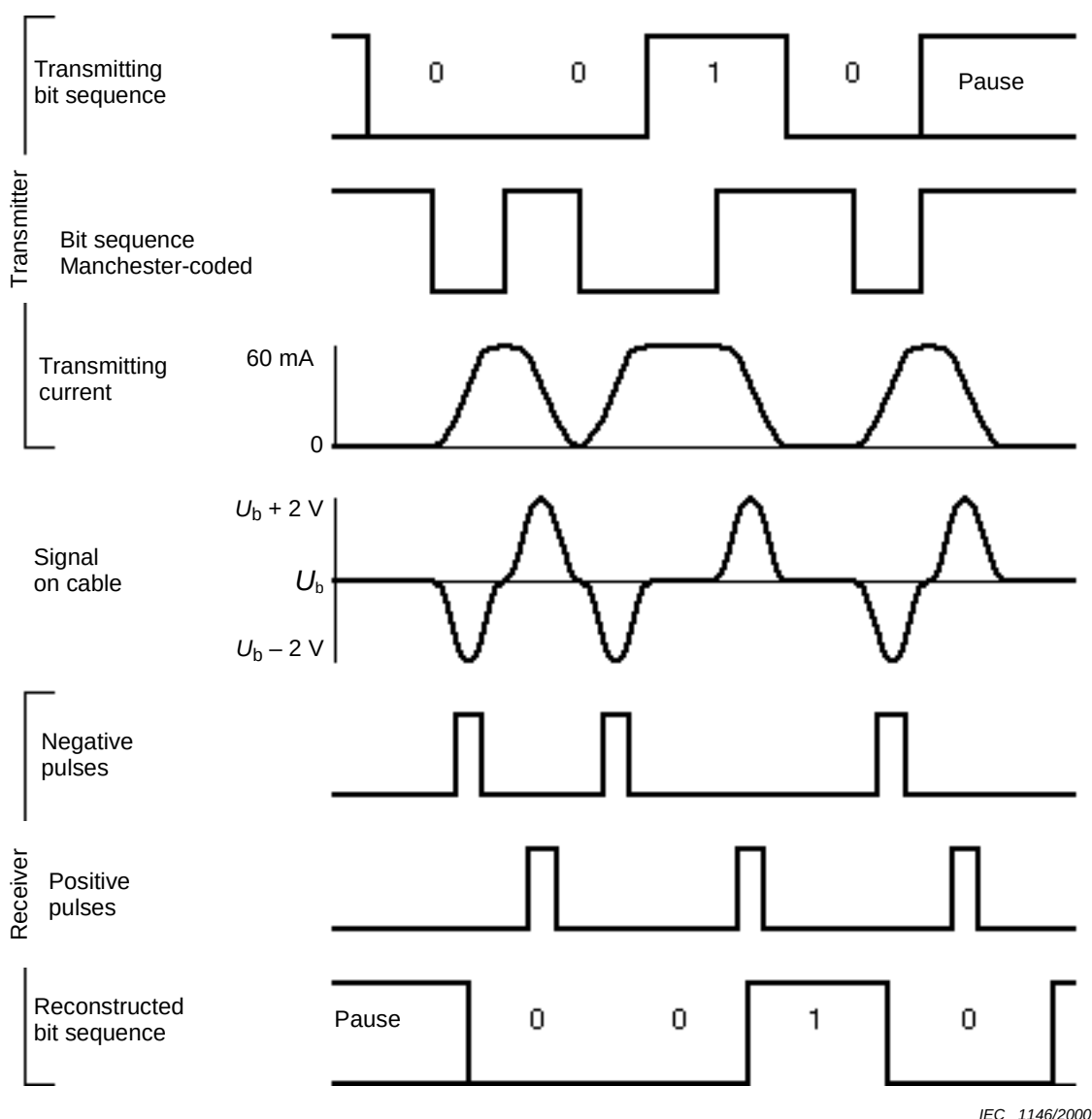


Figure 2 – Transmission coding and encoding principle

5.2.3 Power and data distribution

The simultaneous transmission of data and power on the AS-i line requires technical provisions for decoupling data and power.

The AS-i power supply shall provide the d.c. power requirements of all devices on the AS-i line. Furthermore, it shall perform the main conditioning of the physical data transmission within the system. This comprises the transmission signal forming and adaptation to the cable wave guide magnitude as well as ensuring the symmetry of the AS-i line. The adaptation is provided by a decoupling circuit.

NOTE Power distribution and data distribution are not interdependent but are combined in the AS-i line to reduce cabling requirements.

The galvanic isolation of the AS-i line from the equipment ground shall be according to figure 3. Externally connected components shall meet the PELV requirements of IEC 60364-4-41.

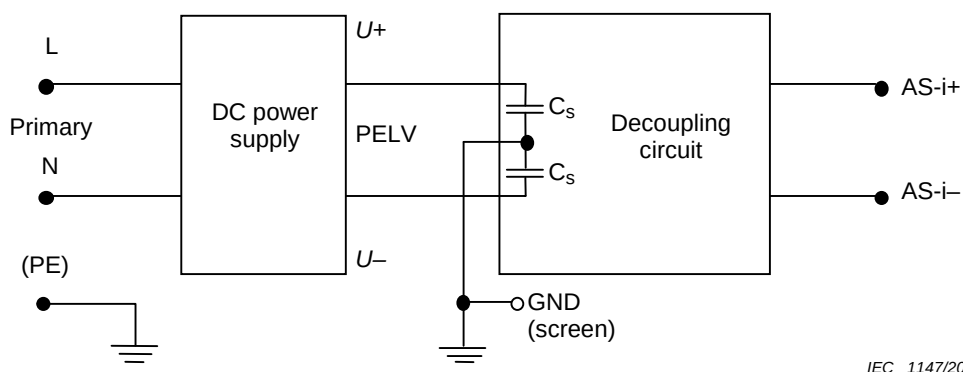


Figure 3 – AS-i power supply incorporating the decoupling circuit

5.3 AS-i topology

The AS-i system is a master-slave communication system composed of a single master and up to 31 slaves. Each slave shall have a unique address in the range 1 to 31. This address is called the operation address. The operation address shall be non-volatile.

The zero address is used during the change of a slave address. Normally, the zero address is non-volatile for factory new slaves.

A single transaction shall be composed of a master request and a slave response. If a slave responds to a master request, it shall start its response within a period of 2,5 to 5,5 bit times after the end of a master request. The master shall be able to accept the start of a slave response within a period of 2,5 to 10 bit times after the end of its request to allow for propagation delay on the line and the possible use of repeaters.

A slave shall not respond if it detects an erroneous master request. The slave shall not give any negative response. The master shall interpret the absence of a slave response as a negative response.

5.4 Data transmission

A data exchange shall be realized by the processing of transactions (see figure 4). A transaction shall start with a master request (issued by the master to transfer data or a command to the slave). The master shall expect a slave response (issued by the slave to transfer data or a command result to the master) within a certain time. If the master does not receive a valid response from the slave within this time, it may retransmit the master request once. After receiving a valid response and after the send pause has elapsed, the master shall start the next transaction.

The AS-i master shall provide means for sending one master request by the master to a single slave and receiving a slave response from the slave. At a given time, the master shall process one, and only one, master request or slave response. After a transaction has been finished, the next transfer can be processed by the master. In case of failure, no more than one retransmission shall be processed in the same cycle.

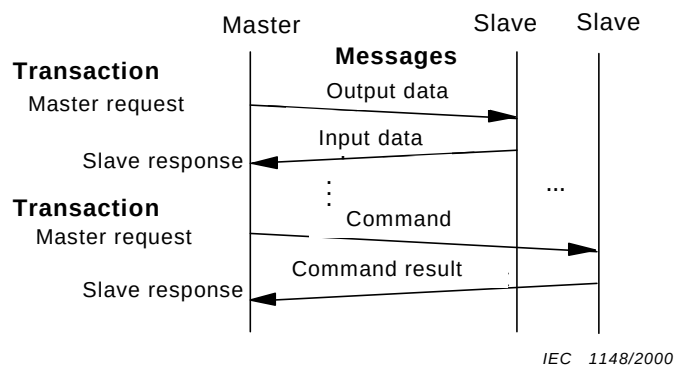


Figure 4 – Transactions

All times specified in this subclause are related to the signals on the AS-i line at the master terminals.

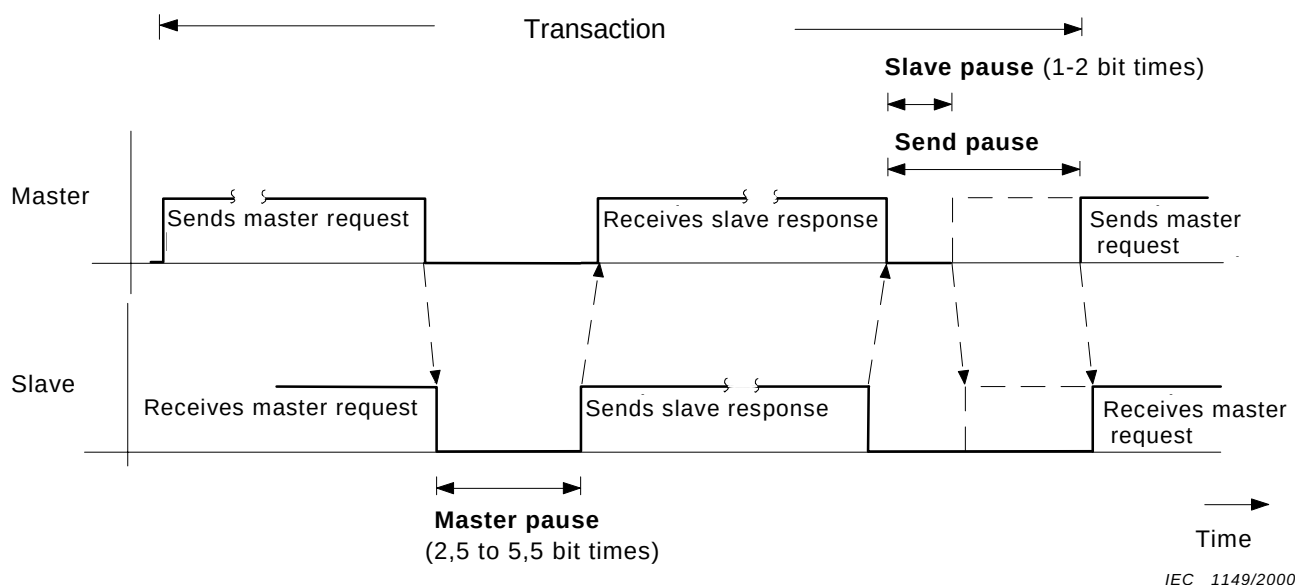


Figure 5 – Transaction cycle

A transaction shall be split into two actions (master request and slave response) and two time intervals (master pause and send pause) according to figure 5.

Master request	Sending a master request from the master to a single slave and expecting a response from the slave.
Master pause	During this time, the slave processes the requested function and produces the response data.
Slave response	Transmission of the slave data or the command result to the master.
Slave pause	After receipt of the slave response, there shall be a minimum period during which no subsequent transmission shall occur. This pause shall be 1 to 2 bit times.
Send pause	After receipt of the slave response, there shall be a minimum period during which no subsequent transmission shall occur. During normal operation with more than 30 transactions per AS-i cycle, the time of this pause shall be one slave pause. If there are 30 or less transactions per AS-i cycle, the send pause may be prolonged to a maximum of 500 μ s. In this case, the AS-i cycle time shall not be longer than 5 ms.

Slave response time-out If no response is received from the slave within a defined time (the slave response time-out) the master shall either end the transaction or repeat the transmission. This time shall be a maximum of 10 bit times. This time shall be determined by the master pause, signal propagation on the line and the repeaters. The time-out timer shall start at the end of the transmission of the master request. Within the slave response time-out, the master expects the beginning of a response frame from the slave. After this time, the transmission function determines the absence of a slave response.

During the send pause, the master shall not transmit any signal. It shall sense the AS-i line to allow the detection of an end bit error.

Subsequent data shall be transmitted only if the AS-i line was idle for at least the duration of a slave pause, after the beginning of the send pause. Every disturbance of this idle state shall cause a restart of the send pause.

A transaction shall be considered successfully processed if:

- **after** the minimum master pause and
- **before** the time of the slave response time-out + 7 T_{bit} has elapsed,
- a **valid** slave response has been received.

After Master Power-On (MPO), the master shall process a send pause.

5.5 AS-i transactions

5.5.1 AS-i transaction types

Four AS-i transaction types are defined in table 1 for data exchange, parameterization, network management and diagnostics. All master requests and slave responses have the same structure and the same length of 14 bits (master request) and 7 bits (slave response).

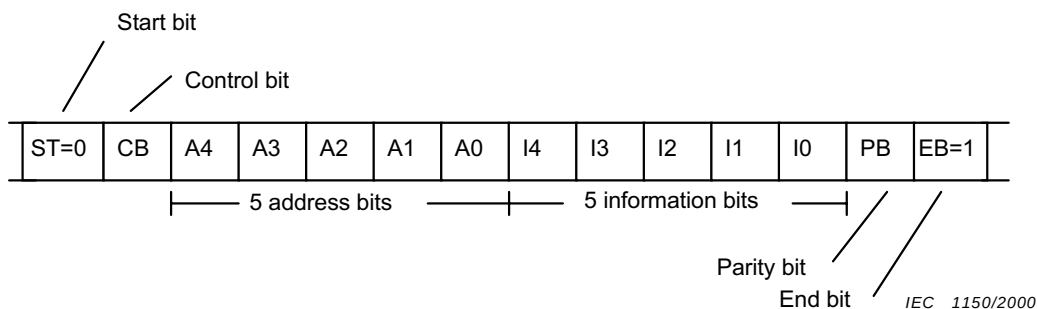
Table 1 – AS-i transaction types

Data_exchange	Delivery and/or receipt of the bit pattern to/from the data output/input ports of the slave
Write_parameter	Delivery of the bit pattern to the parameter ports of the slave
Address_assignment	Assignment of a non-volatile address (1...31) to a slave to replace a zero address
Commands	Miscellaneous functions: - reset_slave - delete_address - read_I/O_configuration - read_identification_code - read_status - read_reset_status - reserve_R1

The master may be able to issue all or only some of the requests (according to a specific master profile), whereas any slave shall be able to respond to all master requests defined (with the possible exception of the address_assignment request).

5.5.2 Structure of the master request

The master request shall be composed as follows:



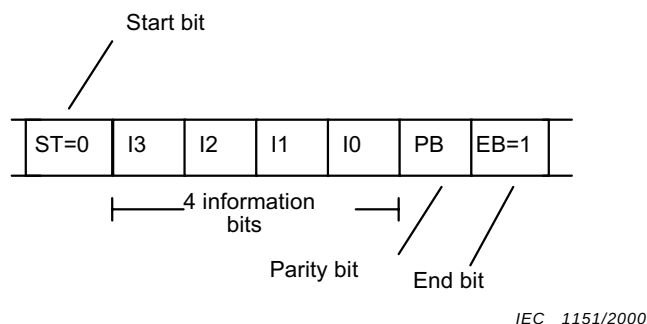
The meaning of each bit shall be as shown in table 2.

Table 2 – Master request

Bit string	Semantic	Comments
ST	Start bit	Identifies the beginning of the master request, always 0
CB	Control bit	Identifies the data/parameter transmission in the information cell 0 = data/parameter transmission/address assignment 1 = command transmission
A4..A0	Address (5 bits)	To address the listed slaves 0x00 = zero address 0x01...0x1F = slave 1 through 31
I4..I0	Information	These five bits contain the information to be transferred to the slave for every request type.
PB	Parity bit	For verification of master requests by the slave The master request has even parity. 0 = even count of 1-symbols in (CB, A4...A0, I4...I0) 1 = odd count of 1-symbols in (CB, A4...A0, I4...I0)
EB	End bit	Marks the end of the master request

5.5.3 Structure of the slave response

The slave response shall be composed as follows:



The meaning of each bit shall be as shown in table 3.

Table 3 – Slave response

Bit string	Semantic	Comments
ST	Start bit	Marks the slave response beginning
I3...I0	Information	Information of the slave response
PB	Parity bit	For verification of master requests by the slave The master request has even parity. 0 = even count of 1-symbols in (I3...I0) 1 = odd count of 1-symbols in (I3...I0)
EB	End bit	Marks the end of the slave response

5.5.4 Individual AS-i transactions

5.5.4.1 General

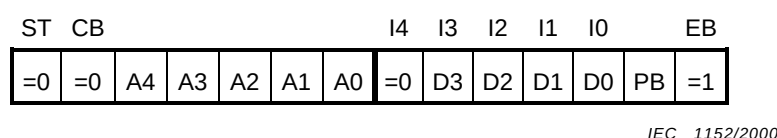
This subclause describes the different transactions. The detailed functions of a slave after receiving a master request are defined in conjunction with the slave specification (slave reactions, see 8.2.1).

All other codes (bit patterns of transactions not defined in this standard) are reserved and shall not be used by any implementation.

5.5.4.2 Data_exchange

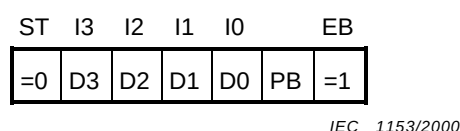
The data_exchange request shall be used by the master to transfer four bits of data (I3...I0) to the data output register of the slave and to get four bits of data from the slave input register.

The data_exchange request shall have the following structure:



The bits A4...A0 shall contain an operation address (1...31).

The slave response shall have the following structure:



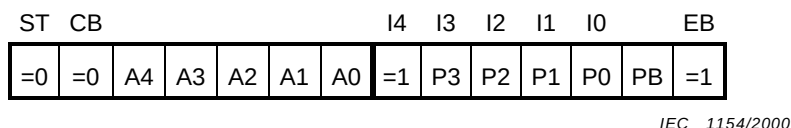
If the slave is not activated, no response shall be generated.

If the I/O configuration of the slave is 0x0F, no response shall be generated.

5.5.4.3 Write_parameter

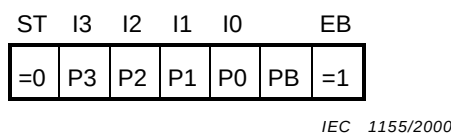
The write_parameter request shall be used by the master to transfer the four parameter bits (I3...I0) to the parameter output register of the slave and to get four parameter bits from the slave parameter ports.

The write_parameter request shall have the following structure:



The bits A4...A0 shall contain an operation address (1...31).

The slave response shall have the following structure:

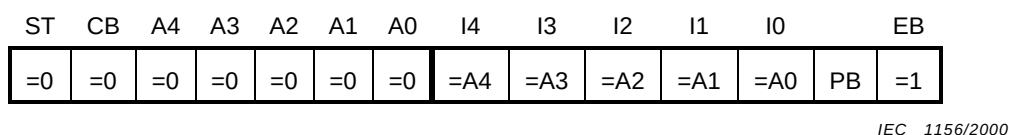


The write_parameter request may affect the behaviour.

5.5.4.4 Address_assignment

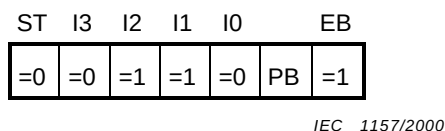
The address_assignment request shall be used by the master to force the slave to store the given address (I4...I0) in a non-volatile form and to use this address when responding to the master requests.

The address_assignment request shall have the following structure:



The bits A4...A0 shall contain the zero address (0x00).

The slave response shall have the following structure:



After a successful address_assignment, a slave shall respond with the new address.

5.5.4.5 Reset_AS-i_slave

The reset_AS-i_slave request shall be used by the master to reset a specific slave.

This command shall be encoded in the information part of the master request by 0x1C. The reset_AS-i_slave command shall have the following structure:

ST	CB						I4	I3	I2	I1	I0		EB
=0	=0	A4	A3	A2	A1	A0	=1	=1	=1	=0	=0	PB	=1

IEC 1158/2000

The slave response shall have the following structure:

ST	I3	I2	I1	I0		EB
=0	=0	=1	=1	=0	PB	=1

IEC 1159/2000

The reset_AS-i_slave request affects the state diagram of the slave.

5.5.4.6 Delete_address (temporary)

The delete_address request shall be used by the master to delete the operation address of a specific slave.

This command shall be encoded in the information part of the master request as 0x00. The delete_address command shall have the following structure:

ST	CB						I4	I3	I2	I1	I0		EB
=0	=1	A4	A3	A2	A1	A0	=0	=0	=0	=0	=0	PB	=1

IEC 1160/2000

The slave response shall have the following structure:

ST	I3	I2	I1	I0		EB
=0	=0	=0	=0	=0	PB	=1

IEC 1161/2000

After a successful delete_address, a slave shall respond with the zero address which is stored in a volatile form.

The delete_address request does not affect the state diagram of the slave.

A delete_address request to a slave with a zero address shall generate a slave response, but shall have no other effect.

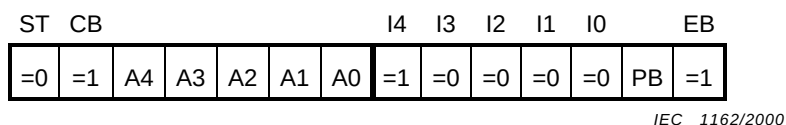
A delete_address request shall not be issued by the master if the slave is in the process of storing its address into the non-volatile memory (processing the address_assignment request).

NOTE This is to prevent an undefined result of the storage process.

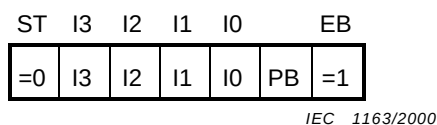
5.5.4.7 Read_I/O_configuration

The read_I/O_configuration request shall be used by the master to read the I/O configuration of a specific slave.

This command shall be encoded in the information part of the master request as 0x10. The read_I/O_configuration request shall have the following structure:



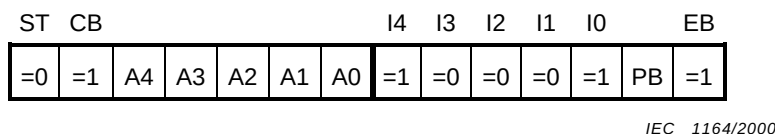
The slave response shall have the following structure:



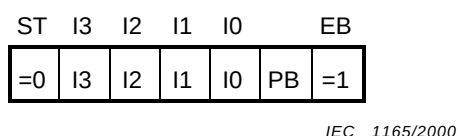
5.5.4.8 Read_identification_code

The command read_identification_code request shall be used by the master to read the identification code of a specific slave.

This command shall be encoded in the information part of the master request as 0x11. The read_identification_code request shall have the following structure:



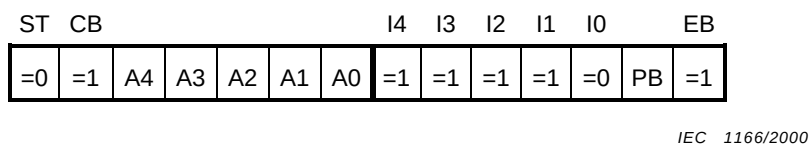
The slave response shall have the following structure:



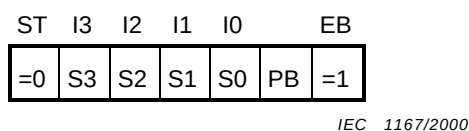
5.5.4.9 Read_status

The read_status request shall be used by the master to read the status of a specific slave.

This command shall be encoded in the information part of the master request as 0x1E. The read_status request shall have the following structure:



The slave response shall have the following structure:



The actual values of S0 to S3 of the status bits shall not be affected by the request.

The slave shall provide four bits for status values. These four bits are independent of each other and shall have the following semantics:

- S0: 0 – address (non-volatile)
 1 – address (volatile)
- S1: 0 – no parity bit error detected
 1 – parity bit error detected
- S2: 0 – no end bit error detected
 1 – end bit error detected
- S3: 0 – no error_reading in non-volatile memory
 1 – error_reading in non-volatile memory

The information given in the status register may be used for diagnostic purposes or for the master to determine what action can be taken to recover from a fault condition.

5.5.4.10 Read_reset_status

The read_reset_status request shall be used by the master to read the status and to reset the status bits of a specific slave.

This command shall be encoded in the information part of the master request as 0x1F. The read_reset_status request shall have the following structure:

ST	CB							I4	I3	I2	I1	I0		EB
=0	=1	A4	A3	A2	A1	A0		=1	=1	=1	=1	=1	PB	=1

IEC 1168/2000

The slave response shall have the following structure:

ST	I3	I2	I1	I0		EB
=0	S3	S2	S1	S0	PB	=1

IEC 1169/2000

After transmitting the slave response, the values of S1 to S3 of the status bits shall be 0.

The semantics of the status bits shall be the same as defined for read_status.

5.5.4.11 Reserve_R1

NOTE The reserve_R1 request is under further consideration.

This command shall be encoded in the information part of the master request as 0x12. The reserve_R1 request shall have the following structure:

ST	CB							I4	I3	I2	I1	I0		EB
=0	=1	A4	A3	A2	A1	A0		=1	=0	=0	=1	=0	PB	=1

IEC 1170/2000

The slave response shall have the following structure:

ST	I3	I2	I1	I0		EB
=0					PB	=1

IEC 1171/2000

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