

Australian/New Zealand Standard™

**Low-voltage switchgear and
controlgear—Controller-device
interfaces (CDIs)**

**Part 6: Seriplex (Serial multiplexed
control bus)**

AS/NZS 62026.6:2002

This Joint Australian/New Zealand Standard was prepared by Joint Technical Committee EL-006, Industrial Switchgear and Controlgear. It was approved on behalf of the Council of Standards Australia on 24 September 2002 and on behalf of the Council of Standards New Zealand on 17 September 2002. It was published on 1 November 2002.

The following are represented on Committee EL-006:

Australasian Railway Association
Australian Chamber of Commerce and Industry
Australian Electrical and Electronic Manufacturers Association
Bureau of Steel Manufacturers of Australia
Electrical Contractors Association of New Zealand
Electricity Supply Association of Australia
Independent Electrical Switchboard Manufacturers Association
Institution of Engineers Australia
Ministry of Economic Development (New Zealand)
National Electrical and Communications Association
Testing Interests (Australia)
WorkCover New South Wales

Keeping Standards up-to-date

Standards are living documents which reflect progress in science, technology and systems. To maintain their currency, all Standards are periodically reviewed, and new editions are published. Between editions, amendments may be issued. Standards may also be withdrawn. It is important that readers assure themselves they are using a current Standard, which should include any amendments which may have been published since the Standard was purchased.

Detailed information about joint Australian/New Zealand Standards can be found by visiting the Standards Australia web site at www.standards.com.au or Standards New Zealand web site at www.standards.co.nz and looking up the relevant Standard in the on-line catalogue.

Alternatively, both organizations publish an annual printed Catalogue with full details of all current Standards. For more frequent listings or notification of revisions, amendments and withdrawals, Standards Australia and Standards New Zealand offer a number of update options. For information about these services, users should contact their respective national Standards organization.

We also welcome suggestions for improvement in our Standards, and especially encourage readers to notify us immediately of any apparent inaccuracies or ambiguities. Please address your comments to the Chief Executive of either Standards Australia International or Standards New Zealand at the address shown on the back cover.

This Standard was issued in draft form for comment as DR 02344.

Australian/New Zealand Standard™

Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)

Part 6: Seriplex (Serial multiplexed control bus)

First published as AS/NZS 62026.6:2002.

COPYRIGHT

© Standards Australia/Standards New Zealand

All rights are reserved. No part of this work may be reproduced or copied in any form or by any means, electronic or mechanical, including photocopying, without the written permission of the publisher.

Jointly published by Standards Australia International Ltd, GPO Box 5420, Sydney, NSW, 2001
and Standards New Zealand, Private Bag 2439, Wellington 6020

ISBN 0 7337 4882 1

PREFACE

This Standard was prepared by the Joint Standards Australia/Standards New Zealand Committee EL-006, Industrial Switchgear and Controlgear.

The objective of this Standard is to define the requirements for interface systems between single or multiple controllers and control circuit devices or switching elements and establishes requirements for the interchangeability of components of such interfaces.

This Standard is Part 6 of a series which, when complete, will consist of the following:

AS/NZS

- 62026 Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)
- 62026.1 Part 1: General rules
- 62026.2 Part 2: Actuator sensor interface (AS-i)
- 62026.3 Part 3: DeviceNet
- 62026.5 Part 5: Smart distributed system (SDS)
- 62026.6 Part 6: Seriplex (Serial Multiplexed Control Bus) (This Standard)

This Standard is identical with and has been reproduced from IEC 62026-6:2001, *Low-voltage switchgear and controlgear—Controller-device interfaces (CDIs)—Part 6: Seriplex (Serial Multiplexed Control Bus)*.

The provisions of the general rules in AS/NZS 62026.1 are applicable to this Joint Australian/New Zealand Standard, where specifically called for. General rules clauses and subclauses thus applicable, as well as tables, figures and annexes, are identified by reference to Part 1 of the IEC Standard from which this Standard is reproduced, for example subclause 7.2.4.1 of IEC 62026-1.

Seriplex (Serial Multiplexed Control Bus) is a controller-device interface which provides a deterministic means of exchanging simple data among control and sensing devices. All devices are connected together by a single shielded four or six conductor cable.

Any device which fully conforms to this part of AS/NZS 62026 will be able to perform at least elementary data exchange with other compliant devices through the Seriplex controller-device interface.

As this Standard is reproduced from an International Standard, the following applies:

- (a) Its number does not appear on each page of text and its identity is shown only on the cover and title page.
- (b) In the source text ‘this standard’ should read ‘this Australian/New Zealand Standard’.
- (c) A full point should be substituted for a comma when referring to a decimal marker.

CONTENTS

	<i>Page</i>
1 Scope	1
2 Normative references.....	1
3 Definitions, symbols and abbreviations	2
3.1 Definitions	2
3.2 Symbols and abbreviations	8
4 Classification	8
4.1 General	8
4.2 Frame period, t_f	9
4.3 Signal update time, t_u	10
4.4 Input response time, t_{ir}	10
4.5 Output response time, t_{or}	11
4.6 System response time, t_{sr}	13
5 Characteristics.....	14
5.1 System overview	14
5.2 Frequency, cable length and node count.....	18
5.3 Data transmission.....	19
5.4 General data transmission features	21
5.5 Signal timing.....	26
5.6 Data definitions	28
5.7 Signal addressing conventions	33
5.8 Operational characteristics	34
5.9 Fault responses.....	39
5.10 Device programming.....	43
6 Product information	44
7 Normal service, mounting and transport conditions	44
7.1 General	44
7.2 Ambient air temperature	44
7.3 Humidity	44
7.4 Conditions during transport and storage	44
7.5 Mounting	44
7.6 Shock	44
7.7 Vibration.....	45
8 Constructional and performance requirements	45
8.1 Seriplex power supply.....	45
8.2 Power distribution.....	45
8.3 Isolation.....	46
8.4 Data line characteristics	46
8.5 Clock line characteristics	48
8.6 Seriplex cable topology.....	50
8.7 Cable specifications.....	51
8.8 Electromagnetic compatibility	53

	<i>Page</i>
9 Tests	55
9.1 Supply polarity.....	55
9.2 Power supply.....	55
9.3 Clock source.....	56
9.4 I/O device	66
9.5 Seriplex cable.....	76
Figure 1 – Seriplex controller-device interface system diagram.....	15
Figure 2 – Peer-to-peer timing diagram.....	16
Figure 3 – Master/slave timing diagram.....	17
Figure 4 – Example of address multiplexing.....	17
Figure 5 – Peer-to-peer transmission format.....	19
Figure 6 – Master/slave mode data transmission format.....	21
Figure 7 – Sync period diagram	23
Figure 8 – Data signal timing diagram.....	27
Figure 9 – Check byte formation	33
Figure 10 – Bus Fault Detection pulse	36
Figure 11 – Digital debounce	38
Figure 12 – Data line diagram.....	47
Figure 13 – Hysteresis	48
Figure 14 – Clock line diagram	49
Figure 15 – Preferred Seriplex topologies	50
Figure 16 – Other controller-device interface topologies	50
Figure 17 – Four-conductor Seriplex cable.....	52
Figure 18 – Six-conductor Seriplex cable.....	53
Figure 19 – Circuit for verification of clock source power consumption.....	56
Figure 20 – Connections for clock signal tests	57
Figure 21 – Clock signal waveform	57
Figure 22 – Test circuit for clock signal.....	59
Figure 23 – Waveform of clock pulse	60
Figure 24 – Transient current.....	60
Figure 25 – Test circuit for CDI data signal	61
Figure 26 – Waveform for CDI data signal.....	61
Figure 27 – Data line waveforms.....	63
Figure 28 – Connections for verification of data line requirements	64
Figure 29 – Waveforms for verification of data line requirements	64
Figure 30 – Connections for verification of I/O device requirements	66
Figure 31 – Connections for verification of I/O device data line capacitance	67
Figure 32 – Connections for measurement of I/O device data line capacitance	67
Figure 33 – Measurement of I/O device data line capacitance.....	68

	<i>Page</i>
Figure 34 – Connections for measurement of I/O device voltage drop	69
Figure 35 – Connections for measurement of output device lower voltage threshold	69
Figure 36 – Connections for measurement of output device upper voltage threshold.....	70
Figure 37 – Connections for measurement of input device lower voltage threshold	71
Figure 38 – Connections for measurement of input device upper voltage threshold.....	72
Table 1 – Maximum available clock frequency for valid networks (single power supply)	18
Table 2 – Maximum available clock frequency for valid networks (multiple power supplies)...	19
Table 3 – Sync period parameters	23
Table 4 – Symbols and parameters	27
Table 5 – CDR signal address assignments	30
Table 6 – Address codes	32
Table 7 – Channel codes	32
Table 8 – I/O direction codes	33
Table 9 – Seriplex power supply requirements	45
Table 10 – Data line characteristics	47
Table 11 – Clock line characteristics.....	49
Table 12 – Wire size and characteristics.....	51
Table 13 – General Seriplex cable characteristics.....	51
Table 14 – Seriplex cable specifications	52

STANDARDS AUSTRALIA/STANDARDS NEW ZEALAND

Australian/New Zealand Standard**Low-voltage switchgear and controlgear—Controller-device interfaces
(CDIs)****Part 6: Seriplex (Serial multiplexed control bus)**

Any IEC table, figure or passage of text that is struck-through is not part of this Standard. Any Australian/New Zealand table, figure or passage of text that is added (and identified by shading) is part of this Standard.

1 Scope

This part of IEC 62026 specifies an interface system between single or multiple controllers, and control circuit devices or switching elements. The interface system uses two twisted conductor pairs within one cable – one of these pairs provides a communication medium and the other pair provides power to the devices. It also establishes requirements for the interchangeability of components with such interfaces.

This standard specifies the physical and operating characteristics of the Seriplex controller-device interface, including:

- requirements for interfaces between controllers and switching elements;
- normal service conditions for devices;
- constructional and performance requirements;
- tests to verify conformance to requirements.

These particular requirements apply in addition to the general requirements of IEC 62026-1.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 62026. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 62026 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

References to International Standards that are struck through in this Clause are replaced by references to equivalent Australian or Australian/New Zealand Standards that are listed immediately thereafter and identified by shading. Any Australian or Australian/New Zealand Standard that is identical to the International Standard it replaces is appropriately identified.

IEC 60068-2-6:1995, *Environmental testing – Part 2: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-27:1987, *Basic environmental test procedures – Part 2: Tests – Test Ea and guidance: Shock*

IEC 60664-1:1992, *Insulation coordination for equipment within low voltage systems – Part 1: Principles, requirements, and tests*

~~IEC 60947-1:1999, Low-voltage switchgear and controlgear – Part 1: General rules~~

AS/NZS 3947.1, Low-voltage switchgear and controlgear, Part 1: General rules (identical with IEC 60947-1:1999 including its Amendment 1:2000)

IEC 61000-4-2:1995, Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 2: Electrostatic discharge immunity test. Basic EMC Publication

~~IEC 61000-4-3:1995, Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 3: Radiated, radio-frequency, electromagnetic field immunity test~~

AS/NZS 61000.4.3, Electromagnetic compatibility (EMC), Part 4.3: Testing and measurement techniques—Radiated, radio-frequency, electromagnetic field immunity test (identical with IEC 61000-4-3:1995 including its Amendment 1:1998)

IEC 61000-4-4:1995, Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 4: Electrical fast transient/burst immunity test. Basic EMC Publication

~~IEC 61000-4-5:1995, Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 5: Surge immunity test~~

AS/NZS 61000.4.5, Electromagnetic compatibility (EMC), Part 4.5: Testing and measurement techniques—Surge immunity test (Identical with IEC 61000-4-5)

~~IEC 61000-4-6:1996, Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 6: Immunity to conducted disturbances induced by radio-frequency fields~~

AS/NZS 61000.4.6, Electromagnetic compatibility (EMC), Part 4.6: Testing and measurement techniques—Immunity to conducted disturbances induced by radio-frequency fields (identical with IEC 61000-4-6:1996)

~~IEC 62026-1:2000, Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 1: General rules~~

AS/NZS 62026.1, Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs), Part 1: General rules (identical with IEC 62026-1:2000)

~~CISPR 11:1997, Industrial, scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement~~

AS/NZS 2064, Limits and methods of measurement of electromagnetic disturbance characteristics of industrial, scientific and medical (ISM) radiofrequency equipment

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purpose of this part of IEC 62026, clause 3 of IEC 62026-1, together with the following additions, apply.

3.1.1

address multiplexing

means of extending the data capacity of a Seriplex controller-device interface by assigning signals to one of 16 multiplex channels and broadcasting the multiplex channel number at the start of each data frame

3.1.2**address sharing**

practice of assigning two or more signals to the same address

NOTE In the peer-to-peer mode, all addresses used are typically shared by one input signal and one output signal.

3.1.3**analogue input device**

device which converts an external analogue signal to a numeric signal to be transmitted to the controller-device interface as input data

3.1.4**analogue output device**

device which converts a Seriplex numeric output signal to an external analogue signal

3.1.5**Bus Fault Detect (BFD) pulse**

negative-going (logic high-to-low-to-high) pulse on the data line during the sync period, produced by the clock source, and used by the clock source and I/O devices to evaluate the condition of the Seriplex controller-device interface

3.1.6**bus halt**

intentional condition in which generation of the Seriplex clock signal is suspended, so that no data signals are transmitted through the controller-device interface, and all output devices assume their default states

NOTE A bus halt is essentially the same as a clock loss condition; bus halt is usually used to indicate that the condition is normal and intentionally induced by the clock source.

3.1.7**clock**

Seriplex signal which is used to synchronize data exchange among connected devices

3.1.8**clock loss**

condition in which the Seriplex clock signal is not operating due to a fault condition, so that no data signals are transmitted through the controller-device interface, and all output devices assume their default states

3.1.9, t_{clock} **clock loss detection period**

time without a transition of the Seriplex clock signal (low-to-high or high-to-low) after which a device detects a clock loss condition

NOTE Typically, output devices will assume their default states after the clock loss detection period has elapsed.

3.1.10**clock module**

dedicated device which performs clock source functions for a Seriplex CDI operating in peer-to-peer mode

3.1.11**clock pulse**

sequence of logic level transitions on the Seriplex clock line, beginning with a positive (logic low-to-high) transition and including a negative (high-to-low) transition

3.1.12**clock rate**

repetition frequency of the Seriplex clock signal during the data-transmission portion of a data frame

NOTE This rate is the reciprocal of the clock period.

3.1.13**clock source**

Seriplex device which generates the clock signal, provides the current source for the data line, and transmits the Bus Fault Detect pulse

NOTE Usually the clock source is incorporated within an interface to a controller, but for peer-to-peer mode operation this may be a clock module instead.

3.1.14**control software**

software which monitors Seriplex input signals and controls Seriplex output signals

NOTE This software might be C or Basic or other code within a computer, ladder logic within a PLC, or embedded firmware within a dedicated control device. Typically this software performs controller-device interface start/stop functions and interface card initialization as well as signal monitoring and control.

3.1.15**daisy-chain**

method of connecting Seriplex devices by cable segments connected end-to-end

3.1.16**data echo**

feature of Seriplex devices whereby the device receives a signal then retransmits that signal to the controller-device interface

NOTE This feature may be used to indicate to a data-transmission device that a data signal has been properly received by another device.

3.1.17**data frame**

sequence of clock pulses on the clock line, bounded at its beginning and end by a sync period

3.1.18**data line capacitance**

capacitance of the data line to all the other conductors

3.1.19**data pass-through**

interface feature used in master/slave mode, which takes controller-device interface input signals and retransmits them as controller-device interface output signals at the same signal addresses, without the intervention of control software

NOTE This feature mimics peer-to-peer mode operation in that input devices may directly control output devices at the same address without control programming.

3.1.20**default state**

state of Seriplex I/O device output signals under initial power-up, clock loss, and bus fault conditions

NOTE Usually this state is the "off" or inactive state, and corresponds to an output signal value of 0.

3.1.21**digital debounce**

optional feature of Seriplex devices whereby multiple identical values of a particular discrete controller-device interface output signal are detected in successive data frames in order to cause the Seriplex device to change the logic state of its external output signals

3.1.22**discrete signal**

data signal consisting of exactly one bit of information

NOTE Such a signal may assume one of only two states or values—logic high or low, 0 or 1. Both Seriplex input and output data signals and a device's external input and output signals may be discrete signals.

3.1.23**drop**

relatively short length of Seriplex cable which is connected to a longer "trunk" cable

NOTE Typically branch lines are 16 m or less, while trunk lines may be hundreds or thousands of metres long.

3.1.24**excess time constant
bleedover**

effect which occurs when the data line cannot recharge to a high logic state within one-half clock period after being released from a logic low state

NOTE This effect may result in signals with an intended value of 0 being incorrectly interpreted as having a value of 1.

3.1.25**frame length**

number of signal addresses transmitted within a single Seriplex data frame

3.1.26**frame period, t_f**

time consumed by one data frame, that is, the elapsed time between the end of successive sync periods during normal operation

3.1.27**host interface**

electronic hardware device which allows control software running on a controller to monitor and control I/O devices through a Seriplex controller-device interface by some means such as a backplane interface or controller-device interface gateway

NOTE A host interface typically also provides Seriplex clock source functions.

3.1.28**input propagation delay**

elapsed time between an external input signal event and that signal's availability within a Seriplex input device for transmission to the controller-device interface

3.1.29**input response time, t_{ir}**

a) in **peer-to-peer mode**, elapsed time between an external input signal event and that signal's appearance on the controller-device interface communications medium

b) in **master/slave mode**, the elapsed time between an external input signal event and that signal's availability to a master's internal logic processor

3.1.30**input signal**

signal received by a Seriplex device other than a controller, and reported to the Seriplex controller-device interface

3.1.31**I/O module**

device that converts between Seriplex signals and external signals from control circuit devices

3.1.32**master**

Seriplex device which executes control logic, incorporates the clock source function, has exclusive access to input data, and is the only device which transmits output data

3.1.33**master/slave mode**

mode 2

operating mode comprising a master and one or more slaves

NOTE In this mode, two clock pulses are transmitted per address – one for input data and the other for output data.

3.1.34**multiplex channel number**

integer between 0 and 15 which serves as an extension of the signal address of devices which support address multiplexing

NOTE Each multiplexed signal is assigned to a single multiplex channel, and is transmitted through the Seriplex controller-device interface during data frames in which the multiplex channel number broadcast by the clock source at the beginning of the data frame matches its assigned channel number.

3.1.35**node**

logically active connection to the controller-device interface

NOTE 1 Typical nodes consist of a clock source or I/O devices.

NOTE 2 Passive connections such as T-junctions are not nodes.

3.1.36**numeric signal**

group of consecutive input or output data bits which together represent a single number or quantity

NOTE The allowable range of a numeric signal value is determined by the number of bits assigned to that signal, typically 8, 12, or 16, and usually assigned a starting signal address which is a multiple of 16 (0, 16, 32, ..., 240).

3.1.37**output propagation delay, t_{op}**

time between a change in the logic state of an output signal within a Seriplex device and the corresponding change in state of its external output signal

3.1.38**output response time, t_{or}**

a) in **peer-to-peer mode**, time between a signal's appearance on the controller-device interface and the corresponding change in state of an external output signal

b) in **master/slave mode**, elapsed time between a signal's assertion by the controller's internal logic processor (usually into an interface card's memory) and the corresponding change in state of an external output signal

3.1.39**output signal**

signal which is received through the controller-device interface by a device other than a controller

3.1.40**peer-to-peer mode**

mode 1

operating mode in which one device can control signals to any other device directly, without the intervention of a controller

NOTE In this mode, one clock pulse is transmitted per address, and input and output data are sampled at the same time.

3.1.41**Seriplex device**

control or sensing apparatus which is electrically connected to the controller-device interface, including both clock sources and I/O devices

NOTE The term "device" refers collectively to the controller-device interface communications circuitry, to any other circuitry within the device, to any mechanical and/or electromechanical actuators which interface with the device circuitry and to the device's physical housing and electrical connectors.

3.1.42**Seriplex power supply**

device which produces the d.c. voltage applied to the controller-device interface circuitry of Seriplex devices

NOTE Typically this power source is electrically isolated from any power sources used to activate control devices or sensors.

3.1.43**signal address**

address

integer between 0 and 255 which identifies a single bit of Seriplex input or output data

3.1.44**signal update time, t_u**

time between successive transmissions of a particular signal through the Seriplex controller-device interface

NOTE For non-multiplexed signals, the signal update time is equal to the frame period. For multiplexed signals, the signal update time is equal to the frame period multiplied by the number of multiplex channels scanned by the clock source.

3.1.45**slave**

Seriplex device that does not generate the controller-device interface clock signal

3.1.46**sync period, t_{sync}**

pause in the Seriplex clock signal at the end of each data frame, causing all I/O devices to reset their address counters, and therefore synchronizing data transmission among devices

3.1.47**system response time, t_{sr}**

elapsed time between an external input signal event and a resulting change in state of an external output signal

NOTE It includes input response time, output response time, controller processing time and I/O device propagation delays.

3.1.48 word

group of 16 bits of Seriplex input or output data assigned to consecutive signal addresses, with the starting address being an integer multiple of 16 (0, 16, 32, ..., 240)

3.2 Symbols and abbreviations

BFD	Bus Fault Detect
CDR	Complementary Data Retransmission
EUT	Equipment Under Test
N_{ch}	Number of multiplex channels scanned by the clock source
t_{bd}	BFD pulse delay
t_{bfd}	BFD pulse duration
t_{br}	BFD pulse recovery time
t_{ch}	Data line charge time
t_{clock}	Clock period
t_{closs}	Clock loss detection period
t_{dis}	Data line discharge time
t_{eof}	End of frame delay
t_f	Frame period
t_{hip}	Host interface input propagation delay
t_{hold}	Hold time after data sampling
t_{hop}	Host interface output propagation delay
t_{hr}	Controller response time
t_{ip}	Input device propagation delay
t_{ir}	Input response time
t_{op}	Output device propagation delay
t_{or}	Output response time
t_{poff}	Data off propagation delay
t_{pon}	Data on propagation delay
t_{setup}	Set-up time before data sampling
t_{sr}	System response time
t_u	Signal update time
V_h	High level of the square wave data signal
V_l	Low level of the square wave data signal

4 Classification

4.1 General

Seriplex is usually applied at the lowest level in a multi-level automation hierarchy. Seriplex concentrates on the typical requirements to connect binary elements to a controller.

Seriplex can be used as an interface physically integrated into field devices, e.g. actuators, sensors, or other devices, allowing design of "intelligent" binary actuators, sensors or other devices and elements. Alternatively, Seriplex may be used in separate modules, each providing interfaces for conventional actuators, sensors or other devices and elements.

The Seriplex concept is independent of the specific field devices.

Connected devices may include:

- sensors (photoelectric switches, proximity sensors, and pushbuttons);
- actuators (valves and contactors);
- universal input/output modules;
- controllers (PLCs and personal computers);
- clock modules.

Cable topology may be of any type. Recommended topologies are daisy chain or trunk and drop, since their performance is the most predictable and easily characterized. Each drop length in a trunk and drop or loop system should be limited to less than 10 m.

The Seriplex cable consists of four or six individually insulated conductors surrounded by a foil shield, and housed within a single overall insulating jacket. The conductors of the four-core cable correspond to the power, common, clock, and data lines. In the six-core cable the two additional conductors (I/O+ and I/O–) are located outside the shield but within the outer jacket.

Both master/slave and peer-to-peer configurations are possible in Seriplex systems.

Clock rates may be up to 200 kHz.

Seriplex signal update time depends on the length of the data frame (from 16 to 256 addresses), the clock rate (10 kHz to 200 kHz), and the number of multiplex channels scanned (1 to 16).

4.2 Frame period, t_f

A frame period is defined as the elapsed time between the end of successive sync periods while a Seriplex bus system is operating normally. Within a given system, the frame period is fixed and is determined by the designated frame length, clock rate, and sync period (t_{sync}).

For clock rates up to 100 kHz, assuming the sync period is eight clock periods in duration, the frame period can be calculated as

$$t_f = [(mode \times frame\ length) + 8] / \text{clock rate}$$

where

mode = 1 for peer-to-peer operation;

mode = 2 for master/slave operation.

For clock rates above 100 kHz, the sync period is normally 16 clock periods in duration, so the frame period is calculated as

$$t_f = [(mode \times frame\ length) + 16] / \text{clock rate}$$

As the formula indicates, the frame period can be reduced either by shortening the frame length or by increasing the clock rate.

4.3 Signal update time, t_u

Signal update time is defined as the elapsed time between successive transmissions of a particular signal through the Seriplex CDI. The longest signal update time for any signal within a given system also defines the time required to update all the CDI data within that system. For non-multiplexed signals, the signal update time equals the frame period:

$$t_u = t_f$$

For multiplexed signals when no priority channels are designated, the signal update time equals the frame period times the number of multiplex channels scanned by the clock source (N_{ch}):

$$t_u = t_f \times N_{ch}$$

If a multiplexed priority channel is designated, the calculations are modified as follows.

For a priority channel:

$$t_u = t_f \times 2$$

For non-priority channels:

$$t_u = t_f \times 2 \times (N_{ch} - 1)$$

4.4 Input response time, t_{ir}

In peer-to-peer mode, input response time is defined as the elapsed time between an external input signal event and that signal's appearance on the Seriplex CDI. Since the timing of the input event need not be synchronized with the operation of the Seriplex CDI, the maximum input response time for a given signal is primarily determined by the signal update time. The propagation delay (t_{ip}) of the input device also affects the input response time, although this factor is usually negligible compared to the signal update time:

$$t_{ir} = t_u + t_{ip}$$

This formula is true for both multiplexed and non-multiplexed signals.

In master/slave mode, input response time is defined as the elapsed time between an external input signal event and that signal's availability to a controller's internal logic processor. In the case of a typical backplane interface, this would be the time from the input event until new input data is posted in the interface's dual-port memory for use by application software. Master/slave input response time is determined by the propagation delay (t_{ip}) of the input device, the signal update time (t_u), the propagation delay (t_{hip}) of the host interface, and whether input data is posted immediately when received or withheld until completion of bus fault detection (BFD) checks.

The input response time formula for immediately posted data is

$$t_{ir} = t_{ip} + t_u + t_{hip}$$

Since input propagation delay can usually be disregarded, and the propagation delay for typical CPU interface cards is approximately 32 clock periods in master/slave mode, the complete calculation for input response time is usually performed as follows:

$$t_{ir} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32] / \text{clock rate}$$

NOTE 1 For clock rates >100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the interface manufacturer.

NOTE 2 For non-multiplexed signals, $N_{ch} = 1$.

If data posting is withheld until BFD checks are completed, an extra delay (t_{eof}) from the time the signal is reported on the Seriplex bus until the end of the following sync period is introduced. This end-of-frame delay is determined by the frame length and the signal's address (input_addr):

$$t_{eof} = [(2 \times \text{frame length} + 8) - (2 \times \text{input_addr})] / \text{clock rate}$$

Therefore the complete input response time formula becomes:

$$t_{ir} = t_{ip} + t_u + t_{hip} + t_{eof}$$

Under the assumptions given above, this would be calculated as

$$t_{ir} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32 + (2 \times \text{frame length} + 8) - (2 \times \text{input_addr})] / \text{clock rate}$$

which can be simplified to

$$t_{ir} = [(2 \times \text{frame length} + 8) \times (N_{ch} + 1) + 32 - (2 \times \text{input_addr})] / \text{clock rate}$$

NOTE 3 For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the interface manufacturer.

NOTE 4 For non-multiplexed signals, $N_{ch} = 1$.

If digital debounce is used, input response time can still be calculated by the same formula. In this case, the selected number of data samples (2 or 3) should be substituted for the number of multiplex channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously for the same signal.

4.5 Output response time, t_{or}

In peer-to-peer mode, output response time is defined as the elapsed time between a signal's appearance on the Seriplex CDI and the corresponding change in state of an output device's external output signal.

Since Seriplex output devices hold output data until a valid BFD check is made before passing the data on to the physical outputs, the primary component of peer-to-peer output response time is the end-of-frame delay (t_{eof}) from the time the signal is reported on the Seriplex CDI until the end of the following sync period. The propagation delay (t_{op}) of the output device also affects the output response time, although this factor is usually negligible compared to the end-of-frame delay:

$$t_{or} = t_{eof} + t_{op}$$

where

$$t_{eof} = (\text{frame length} + 8 - \text{output_addr})/\text{clock rate}$$

NOTE 1 For clock rates >100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the interface manufacturer.

NOTE 2 This formula applies to both multiplexed and non-multiplexed signals.

If digital debounce is used, output response time becomes:

$$t_{or} = t_{eof} + t_{op} + (\text{deb_lgth} \times t_u)$$

where deb_lgth is the selected debounce length for the signal; the number of identical data samples (2 or 3) required before the corresponding output changes state.

Digital debounce and address multiplexing shall not be used simultaneously for the same signal.

In master/slave mode, output response time is defined as the elapsed time between a signal's assertion by the controller's internal logic processor (usually into a backplane interface's dual-port memory) and the corresponding change in state of an external output signal.

Since the writing of output data into a backplane interface's dual-port memory is not synchronized with the operation of the Seriplex CDI, the maximum output response time for a given signal is primarily determined by the signal update time. There is also an end of frame delay (t_{eof}) as described for peer-to-peer output response time. Finally, the propagation delays of both the host interface (t_{hop}) and the output device itself (t_{op}) contribute to the total output response time.

The complete output response time formula is

$$t_{or} = t_u + t_{hop} + t_{eof} + t_{op}$$

Since output propagation delay can usually be disregarded, and the host propagation delay for typical CPU interface cards is approximately 32 clock periods in master/slave mode, the complete calculation for output response time is usually performed as follows:

$$t_{or} = [(2 \times \text{frame length} + 8) \times N_{ch} + 32 + (2 \times \text{frame length} + 8) - (2 \times \text{output_addr})]/\text{clock rate}$$

which can be simplified to

$$t_{or} = [(2 \times \text{frame length} + 8) \times (N_{ch} + 1) + 32 - (2 \times \text{output_addr})]/\text{clock rate}$$

NOTE 3 For clock rates > 100 kHz, the factor of 8 in the above formula can change to 16 or to some other value specified by the interface manufacturer.

NOTE 4 For non-multiplexed signals, $N_{ch} = 1$.

If digital debounce is used, output response time can be calculated using the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously on the same signal.

4.6 System response time, t_{sr}

Seriplex CDI system response time is defined as the elapsed time between an external input signal event and a resulting change in state of an external output signal.

For the Seriplex CDI peer-to-peer mode, system response time is simply the sum of input response time and output response time:

$$t_{sr} = t_{ir} + t_{or}$$

This formula can be expanded to

$$t_{sr} = t_{ip} + t_u + t_{eof} + t_{op}$$

Disregarding input and output propagation delays as before, this formula is typically calculated using the formula:

$$t_{sr} = [(frame\ length + 8) \times N_{ch} + (frame\ length + 8) - output_addr] / clock\ rate$$

which can be simplified to

$$t_{sr} = [(frame\ length + 8) \times (N_{ch} + 1) - output_addr] / clock\ rate$$

NOTE 1 For clock rates > 100 kHz, the factor of 8 in the above formula changes to 16 or to some other value specified by the clock source manufacturer.

NOTE 2 For non-multiplexed systems, $N_{ch} = 1$.

If digital debounce is used, system response time can still be calculated by the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously on the same signal.

For Seriplex master/slave mode systems, system response time factors include controller processing time t_{hr} as well as input response time t_{ir} and output response time t_{or} :

$$t_{sr} = t_{ir} + t_{hr} + t_{or}$$

Disregarding input and output propagation delays, this formula is calculated as:

$$t_{sr} = [2 \times (2 \times frame\ length + 8) \times (N_{ch} + 1) + 64 - (2 \times input_addr) - (2 \times output_addr)] / clock\ rate + t_{hr}$$

If digital debounce is used, system response time can still be calculated by the same formula. In this case, the debounce length (deb_lgth) of 2 or 3 data samples should be substituted for the number of multiplexed channels (N_{ch}).

Digital debounce and address multiplexing shall not be used simultaneously on the same signal.

Controller processing time is outside the scope of this standard, and is dependent on a wide variety of factors including processor type and speed, control program type and size, and data polling methods.

5 Characteristics

5.1 System overview

A Seriplex system consists of the following elements, as shown in figure 1:

- controller-device interface cable;
- clock source;
- input and output (I/O) devices;
- Seriplex power supply(ies);
- control power supply(ies);
- controller (optional).

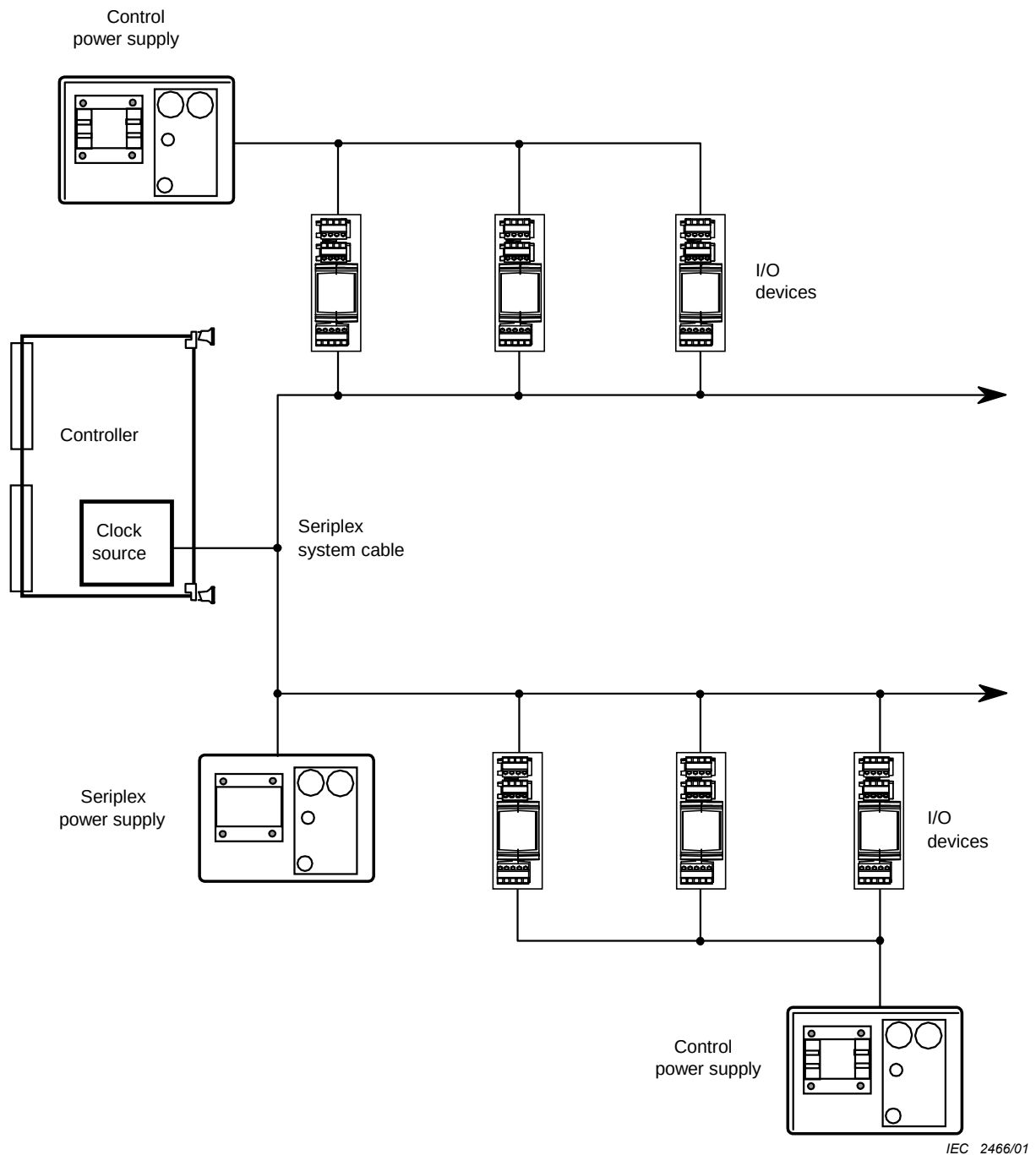


Figure 1 – Seriplex controller-device interface system diagram

The controller-device interface cable conducts Seriplex power and signals among the various system elements. It consists of four insulated conductors, surrounded by a shield and an outer insulating jacket. Two of the wires conduct Seriplex power, while the other two conduct a clock and a data signal which are used to transmit data among system devices. A six-core cable can be used in which the two additional conductors (I/O+ and I/O-) are located outside the shield but within the outer jacket.

The clock source generates the controller-device interface clock signal which is used to synchronize data transfer among system devices. It also provides a current source for the data signal, so that this signal assumes a normally-high logic state. The clock source periodically transmits a Bus Fault Detect (BFD) pulse which is used by input and output devices to validate the operational status of the controller-device interface; the clock source also makes use of this pulse to monitor and report fault conditions. The clock source may either be a “passive” device providing controller-device interface arbitration, or it may be a master or controller providing centralized control and reporting of all controller-device interface data.

I/O devices carry out the physical activities of a control system. They may be simple devices such as switches and lamps, or complex such as operator interface terminals and motion controllers. Input devices sense external conditions and report them to the controller-device interface, while output devices perform some action based on controller-device interface data.

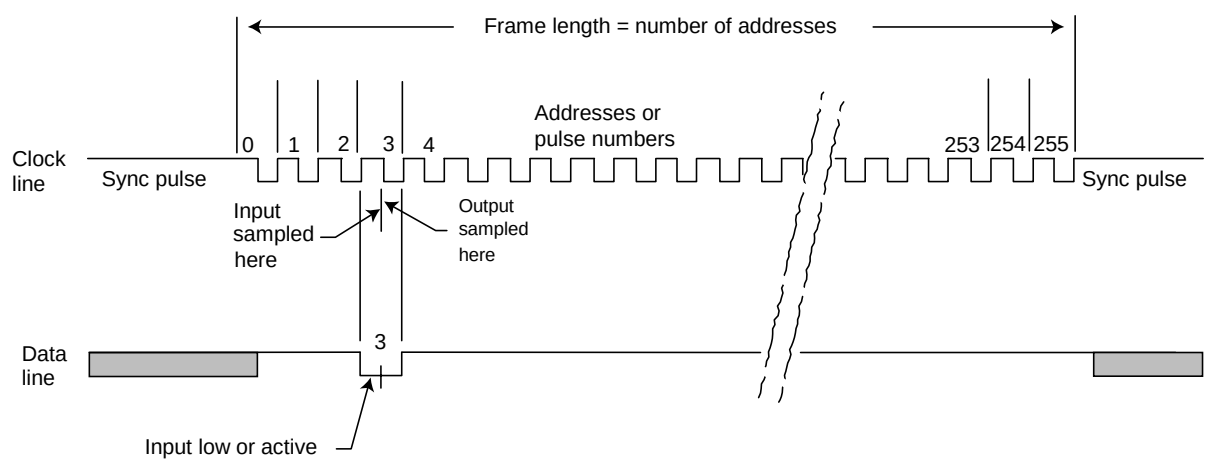
The Seriplex power supply provides power for the controller-device interface itself; that is, for the controller-device interface circuitry within each device. The Seriplex power supply provides a 24 V d.c. source for the controller-device interface. Multiple Seriplex power supplies may be used within a single system.

NOTE 1 In general, the Seriplex power supply does not provide power to monitoring and control devices, so that an I/O fault would not cause a controller-device interface supply failure and in turn halt the operation of the controller-device interface.

NOTE 2 Control power supplies provide power for I/O circuitry such as sensors and actuators. Although this type of power supply may also connect directly to Seriplex I/O devices, in general such supplies are electrically isolated from the Seriplex power supply. This is so that control faults such as a short-circuit load do not affect the operation of the controller-device interface itself, although they may trip circuit breakers or otherwise remove power from the control devices.

NOTE 3 A controller typically consists of a combination of hardware and software, such as a personal computer or programmable controller, and provides centralized reporting and control of data. A controller usually operates a controller-device interface in the master/slave mode, meaning that all input data is reported exclusively to the controller, and that the controller has exclusive control over the states of all output signals.

Controller-device interface data is transmitted through the clock and data signals. Each data transmission frame is defined by a series of pulses on the clock line, bounded by a sync period during which the clock line remains inactive for a defined period of time. Each device on the controller-device interface counts the clock pulses, and the state of the data line during a particular clock period defines the value of a corresponding data signal bit (see figure 2).



IEC 2467/01

Figure 2 – Peer-to-peer timing diagram

Each discrete I/O device on the controller-device interface is assigned an address. In the peer-to-peer mode, this signal address corresponds directly to the sequence of the clock pulses. For example, input device 17 asserts its signal value on the data line during clock pulse 17. Correspondingly, output device 17 monitors the data line during clock pulse 17 to determine whether it should be on or off until the next time its signal is presented to the controller-device interface. In this way, input devices directly control output devices without intervention by a host controller such as a computer or programmable logic controller (PLC).

Devices may be assigned multiple signal addresses in order to form a multi-bit signal value. For example, 16 consecutive bits could be assigned to an analogue input device such as a flow meter; these bits would then represent a 16-bit binary number which could be read and used by another device.

In the master/slave mode, there are two clock pulses per signal address instead of one as in the peer-to-peer mode (see figure 3). During the first clock pulse for each address, input data is transmitted from a device to a controller such as a computer or PLC. During the second clock pulse, the controller transmits output data to devices. This logically separates input signals from output signals at the same address, and allows the host controller to make all control decisions and to have exclusive control over the state of all output signals.

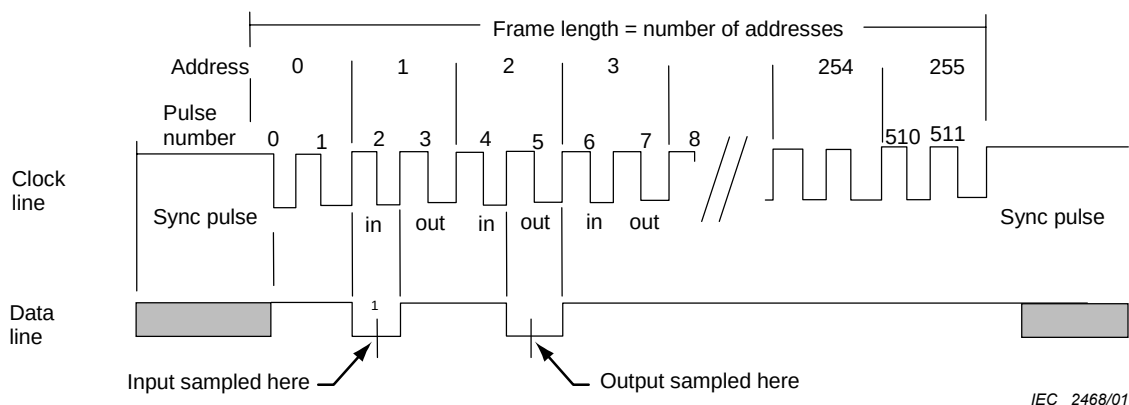


Figure 3 – Master/slave timing diagram

The maximum number of signal bits which may be transmitted within a single data frame is 255 in peer-to-peer mode and 510 in master/slave mode (address 0 is not used). However, the peer-to-peer mode still supports 510 I/O devices because each signal acts as both an input and an output signal. Signal capacity may be increased by address multiplexing in which multiplexed devices are assigned the same signal addresses. This is accomplished by using output signals 1 through 4 as a binary number which indicates a "multiplex channel" between 0 and 15 (see figure 4). A single multiplex channel is scanned in each data frame. Remote I/O devices may be assigned to an individual multiplex channel. These devices monitor the multiplex channel indication to determine whether to assert or receive their signals within a particular data frame.

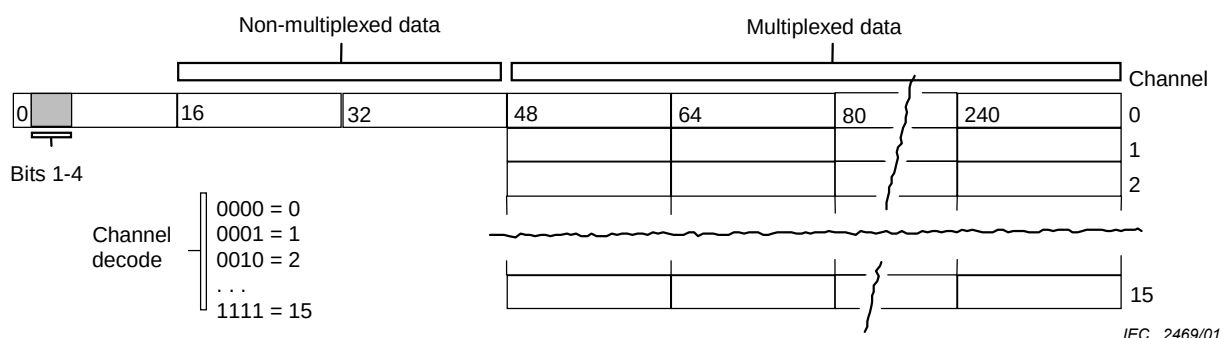


Figure 4 – Example of address multiplexing

Seriplex signal update time depends on the length of the data frame (from 16 to 256 addresses), the clock rate (10 kHz to 200 kHz), and the number of multiplex channels scanned (1 to 16).

The Seriplex clock and data signal amplitude is 12 V d.c. nominal. The data signal is low-true, meaning that a low logic level corresponds to a value of 1, with high corresponding to 0. In its "resting" state, the data line is pulled high by the clock source. Any device asserts its input signals by either pulling the data line low during the proper clock pulse to indicate a 1, or by leaving the data line high to indicate a 0. With this method, "wire-OR" logic may be used; that is, multiple devices may be assigned to a given input signal and any of them may assert a 1 to override the 0s asserted by the other devices. Similarly, multiple output devices may be assigned to the same address, and will respond to the same output signal value. In this way the I/O capacity of the controller-device interface may increase to more than 510 devices per data frame.

5.2 Frequency, cable length and node count

The relationship between clock rate, node count, and cable length is governed by two limiting factors; voltage drop through the cable, and cable transmission effects. The two primary transmission effects are propagation delay and bulk capacitance of both the cable and the connected devices.

Table 1 and table 2 both show the maximum allowable operating frequency for a given bus node count and cable length, under different conditions. In both cases the following assumptions are made:

- cable type = 1622P16;
- I/O device capacitance = 75 pF;
- I/O device current consumption = 17 mA;
- ambient temperature = 25 °C.

Table 1 assumes that the clock source and a single bus power supply are located at the same end of the bus cable, and that all nodes are connected directly to the trunk cable (drop length = 0) and distributed evenly along the length of the cable. In this case the voltage drop in the cable is the primary limiting factor.

Table 1 – Maximum available clock frequency for valid networks (single power supply)

Cable length M	Number of nodes							
	5	10	20	50	100	200	500	1 000
25	150 kHz	125 kHz	75 kHz	50 kHz	20 kHz	—	—	—
50	125 kHz	100 kHz	64 kHz	—	—	—	—	—
100	75 kHz	64 kHz	32 kHz	—	—	—	—	—
200	64 kHz	32 kHz	—	—	—	—	—	—
500	25 kHz	—	—	—	—	—	—	—
1 000	—	—	—	—	—	—	—	—
2 000	—	—	—	—	—	—	—	—
3 000	—	—	—	—	—	—	—	—

Table 2 assumes that the clock source is at one end of the bus cable, that all nodes are connected directly to the trunk cable (drop length = 0) and that multiple power supplies are distributed throughout the bus as necessary to ensure that the cable voltage drop is limited to that caused by the 30 mA data line current. In this case, cable transmission effects limit the operating frequency.