



Designation: F 1153 – 92 (Reapproved 1997)

AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements¹

This standard is issued under the fixed designation F 1153; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers procedures for measurement of metal-oxide-silicon (MOS) structures for flatband capacitance, flatband voltage, average carrier concentration within a depletion length of the semiconductor-oxide interface, displacement of flatband voltage after application of voltage stress at elevated temperatures, mobile ionic charge contamination, and total fixed charge density. Also covered is a procedure for detecting the presence of P-N junctions in the subsurface region of bulk or epitaxial silicon.

1.2 The procedure is applicable to *n*-type and *p*-type bulk silicon with carrier concentration from 5×10^{14} to 5×10^{16} carriers per cm^3 , inclusive, and *N/N*⁺ and *P/P*⁺ epitaxial silicon with the same range of carrier concentration.

1.3 The procedure is applicable for test specimens with oxide thicknesses of 50 to 300 nm.

1.4 The procedure can give an indication of the level of defects within the MOS structure. These defects include interface trapped charge, fixed oxide charge, trapped oxide charge, and permanent inversion layers.

1.5 The precision of the procedure can be affected by inhomogeneities in the oxide or in the semiconductor parallel to the semiconductor-oxide interface.

1.6 The procedure is applicable for measurement of mobile ionic charge concentrations of $1 \times 10^{10} \text{ cm}^{-2}$ or greater. Alternative techniques, such as the triangular voltage sweep method² (1), may be required where mobile ionic charge concentrations less than $1 \times 10^{10} \text{ cm}^{-2}$ must be measured.

1.7 The procedure is applicable for measurement of total fixed charge density of $5 \times 10^{10} \text{ cm}^{-2}$ or greater. Alternative techniques, such as the conductance method (2), may be required where the interface trapped-charge density component of total fixed charge of less than $5 \times 10^{10} \text{ cm}^{-2}$ must be measured.

1.8 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appro-*

priate safety and health practices and determine the applicability of regulatory limitations prior to use.

2. Referenced Documents

2.1 ASTM Standards:

F 388 Method for Measurement of Oxide Thickness on Silicon Wafers and Metallization Thickness by Multiple Beam Interference (Tolansky Method)³

F 576 Test Method for Measurement of Insulator Thickness and Refractive Index on Silicon Substrates by Ellipsometry⁴

F 723 Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon⁴

3. Terminology

3.1 Definitions of Terms Specific to This Standard:

3.2 *accumulation condition*—the region of the C-V curve for which a 5 V increment toward a more negative voltage for *p*-type material (Fig. 1), or toward a more positive voltage for *n*-type material (Fig. 2), results in less than a 1 % change in the maximum capacitance, C_{max} .

3.3 *equilibrium capacitance*—that capacitance reached after an MOS specimen at a fixed bias is illuminated and then allowed to stabilize in darkness.

3.4 *flatband condition, in microelectronics*—the point at which an external applied voltage causes there to be no internal potential difference across an MOS structure. Under practical conditions, metal-semiconductor work-function differences and charges in the oxide require the application of an external voltage to produce the flatband condition.

3.5 *flatband voltage, V_{fb}* —the applied voltage necessary to produce the flatband condition.

3.6 *flatband capacitance, C_{fb}* —the capacitance of an MOS structure at the flatband voltage.

3.7 *inversion condition*—for the purposes of this test method and for measurements on surfaces that do not exhibit a permanent inversion layer, the region of the Capacitance-Voltage, (C-V) curve for which a 5 V increment toward a more positive voltage for *p*-type material (Fig. 1), or toward a more negative voltage for *n*-type material (Fig. 2), results in less than

¹ This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved May 15, 1992. Published July 1992. Originally published as F 1153 – 88. Last previous edition F 1153 – 88.

² Boldface numbers in parentheses refer to the list of references at the end of this test method.

³ Discontinued; see 1992 Annual Book of ASTM Standards, Vol 10.05.

⁴ Annual Book of ASTM Standards, Vol 10.05.

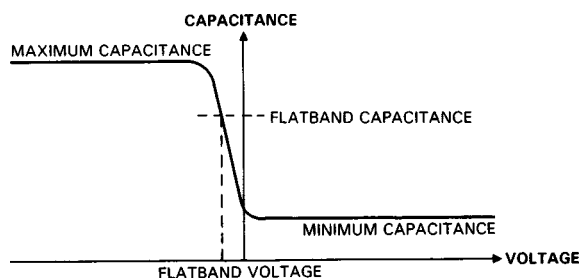


FIG. 1 Typical Capacitance-Voltage Plot of MOS Device Fabricated with p -Type Silicon

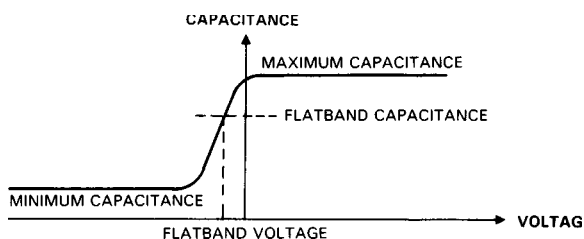


FIG. 2 Typical Capacitance-Voltage Plot of MOS Device Fabricated with n -Type Silicon

1 % change in the equilibrium minimum capacitance, C_{min} .

3.8 *permanent inversion layer*—for the purposes of this test method, the region of the C-V curve that exhibits a definite minimum "dip," as shown in Fig. 3. The permanent inversion layer is an anomalous condition caused by interface charge or surface conditions and prevents proper determination of C_{min} .

3.9 *total fixed charge density*, N_{tf} —the sum of the nonmobile charge densities: oxide fixed charge density, oxide trapped charge density, and interface trapped charge density (3).

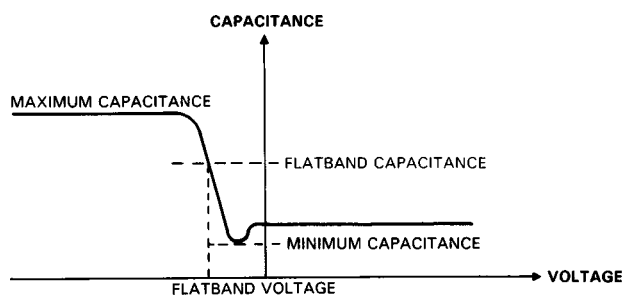
4. Summary of Test Method

4.1 A specimen MOS structure consisting of a metal field plate on the oxidized silicon substrate is fabricated.

4.2 The small-signal, high-frequency capacitance of the specimen is measured as a function of a ramped voltage applied between the field plate and the silicon substrate.

4.3 The surface carrier concentration, flatband capacitance, and flatband voltage, are computed from the capacitance and voltage data.

4.4 A voltage stress is applied to the sample at elevated temperature and the shift in V_{fb} is measured after cooling. This shift is interpreted as a measure of the concentration of mobile ionic charges in the oxide.



NOTE 1—Specimen exhibits permanent inversion layer.

FIG. 3 Capacitance-Voltage Plot of MOS Device Fabricated with p -Type Silicon

4.5 Total fixed-charge density is calculated from the flatband voltage.

4.6 The presence of subsurface P-N junctions is detected by photosensitivity. The specimen is biased into accumulation, and the capacitance measured and recorded. The specimen is then illuminated and the capacitance remeasured. An increase in capacitance due to illumination is interpreted as an indication of the presence of a P-N junction.

NOTE 1—Light will generate charge in the P-N junction and alter the capacitance of the junction which is in series with the MOS device. For the purposes of this test method, the subsurface region is defined as the region extending from the true surface to a depth at which no light penetrates. For the visible spectrum, maximum penetration depth is not well defined, as it depends on the intensity and spectral distribution of the light source and the carrier concentration of the silicon.

5. Significance and Use

5.1 Net carrier concentration present near the silicon-oxide interface may constitute an important acceptance requirement. Where there is not significant doping compensation by impurities of the opposite conductivity type, the material resistivity may be determined from this carrier concentration using Practice F 723.

5.2 Flatband voltage is an important parameter in the manufacture of MOS devices. Its value is dependent on the work function difference between the silicon and the metal field plate, interface trapped charge, and fixed or trapped charge distributed within the oxide. It can be an indicator of anomalies in these values (4).

5.3 Instability of the flatband voltage of an MOS structure subjected to voltage stress at elevated temperatures is a measure of the mobile ionic charge concentration within the oxide. Most device applications require that mobile ionic charge be minimized.

5.4 This test method may be employed for qualification of furnaces or other semiconductor device-processing equipment where such qualification depends on the determination of contamination resulting from high mobile ionic charge concentration.

5.5 The presence of unwanted subsurface P-N junctions may have deleterious effects on device operation.

6. Interferences

6.1 If the apparatus is not well shielded from electromagnetic interference caused by radio frequency (r-f) fields, their presence may affect the measurements since the impedance of the MOS structure is high and since the test signal used is in the mV range.

6.2 The presence of any light during the measurements will adversely affect the results as the capacitance of the MOS device in the inversion condition is light sensitive.

6.3 The measurement may be affected if the relative humidity of the environment is permitted to exceed 60 %. The use of dry N_2 gas flowing into the sample chamber is recommended to control excess humidity.

6.4 The presence of a permanent surface inversion layer condition can affect the measurement.

NOTE 2—A permanent surface inversion layer condition makes it difficult to determine the value for C_{min} to be used in the calculations. If

an incorrect $C_{\min}$ were chosen, all shift values would still be correct, but doping and fixed charge computations would be wrong.

6.5 Stray capacitance and inductance caused by excessive lengths of connecting cable and by improper zeroing of the capacitance measuring instrument can cause significant errors in the capacitance measurement. Typical cable lengths should be kept below 1 m.

6.6 Alternating Current, (a-c) test signals greater than 25 mV rms can lead to errors in the measured capacitance.

6.7 Series resistance between the MOS capacitor and the capacitance measuring instrument can cause significant errors in the measured capacitance. Sources of series resistance can be in the sample itself, in the back contact, or in the test cables.

6.8 A leaky oxide which draws significant current can cause errors in the measured capacitance.

6.9 Inability of an inversion layer to form in an MOS sample will preclude measurement by this test method.

6.10 Very long minority-carrier lifetime in an MOS sample may cause errors in the measurement of $C_{\min}$ if the inversion layer has not had sufficient time to form.

NOTE 3—A maximum lifetime cannot be specified readily. However, an error will occur if the lamp in 11.9 is not illuminated for sufficient duration, or is not of sufficient intensity to generate charge to form the inversion layer.

6.11 Prolonged negative-bias temperature stressing can result in a shift in flatband voltage larger than the shift due to mobile ionic charge alone.

6.12 Hysteresis in the capacitance-voltage characteristics of an MOS sample can cause significant error in the determination of mobile ionic charge concentration.

7. Apparatus

7.1 *Facilities*, for growing gate quality oxides and for depositing and defining metal field plates on the oxide.

7.2 *Electrical Apparatus*:

7.2.1 *Ramping d-c Voltage Supply*, covering the range ± 100 V and capable of sweeping between any two preset voltages within that range. Sweeping rate shall be variable between 0.1 and 1 V/s. Ripple shall be 0.5 % of the d-c output, or less. The supply shall be capable of supplying a fixed preset voltage with an accuracy of ± 10 mV.

7.2.2 *Capacitance Meter*, with full scale ranges of 1 pF to 1000 pF, or greater, in decade, or smaller, steps. The measurement frequency shall be in the range 0.9 to 1.1 MHz inclusive. The accuracy shall be 0.5 % of full scale or better for each range and the reproducibility shall be 0.25 % of full scale or better. The instrument shall be capable of sustaining an external d-c bias of ± 100 V or greater and shall be capable of compensating for an external probe fixture with stray capacitance of up to 5 pF. The a-c measuring signal shall be 0.025 V rms or less. The meter shall have an analog voltage output proportional to the capacitance measurement; output impedance shall be 100 Ω , or less.

NOTE 4—C-V measurements of MOS capacitors built from thin oxides on high resistivity substrates exhibit high series resistance effects which may require concurrent conductance measurements and subsequent computations to determine the true MOS capacitance. This test method is limited to capacitance-only measurements, but includes a test in 12.1 to check for the presence of series resistance effects.

7.2.3 *Digital Voltmeter (DVM)*, with sensitivity 1 μ V or better, accuracy of 0.5 % of full scale or better, a reproducibility of 0.25 % of full scale or better, an input impedance of 10 M Ω or greater, and a common mode rejection 100 dB or greater at 60 Hz.

7.2.4 *X-Y Recorder*, with a minimum slewing speed of 20 cm/s, an accuracy of 0.5 % of full scale or better, a linearity of 0.5 % of full scale or better, and an input impedance of 1 M Ω or greater. X-axis and y-axis sensitivities shall be 5 mV/cm or greater.

7.2.5 *Stress Bias d-c Power Supply*, capable of supplying 0 to ± 100 V (open circuit) with ripple 1 % of the d-c output or less, to be used for voltage stressing.

7.3 *Standard Capacitors*, of accuracy 0.25 % or better at the measurement frequency. At least one capacitor shall be used for each capacitance meter range used. At least one capacitor shall be in the range 1 to 10 pF inclusive and one shall be in the range 10 to 100 pF inclusive.

7.4 *Probe Fixture*:

7.4.1 *Probe*, to contact the top field plate; probe force shall not exceed 1.75 N; probe tip shall have a nominal radius of curvature of 5 μ m; probe and holder should be designed such that the stray capacitance is less than 1 pF.

7.4.2 *Vacuum Chuck*, to hold the specimen wafer and contact the back surface; capable of reaching a temperature of 300°C, and maintaining set temperature to within $\pm 10^\circ$ C over the specimen area.

7.4.3 *Light Tight Metal Box*, to enclose the specimen during the measurement. Equipped with incandescent lamp, 7 to 20 W.

7.4.4 *Dry N₂ Gas Flow*, to control the humidity in the sample chamber.

7.5 *Equipment*, to measure the temperature of the vacuum chuck of 7.4.2 with an accuracy of $\pm 2^\circ$ C.

7.6 *Toolmaker's Microscope, Shadowgraph or Planimeter*, capable of measuring the field plate diameter to an accuracy of 0.5 % or better or the field plate area to an accuracy of 1 % or better.

7.7 *Shielded Cables*, for making electrical connections between the probe fixture, ramping voltage supply, capacitance meter, and digital voltmeter.

7.8 *Precision Voltage Source*, capable of providing output voltages from -100 to $+100$ V. The accuracy of this source shall be 0.1 % or better.

7.9 *A d-c Current Detector*, capable of measuring currents in the range from 100 nA to 1 mA, inclusive, with an accuracy of ± 1 %.

NOTE 5—This test method indicates the use of basic analog instrumentation to perform the various test procedures. This does not preclude the implementation of this test method by computerized or otherwise automated instrumentation provided that such instrumentation is of equivalent accuracy and that the algorithms used therewith conform to the procedures of this test method.

8. Sampling

8.1 A specimen wafer sampling plan shall be agreed upon by all parties to the test. This sampling plan shall address the number of wafers per lot to be tested and the number of test points per wafer.