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Standard Terminology of Silicon Technology¹

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1. Scope

1.1 This terminology covers terms and definition used in relation to semiconductor grade silicon crystal and wafers.

1.2 This terminology covers terms describing attributes of silicon wafers as specified in SEMI Specifications M1 and SEMI Format M18. These attributes include electrical, structural, chemical, and mechanical characteristics of polished and epitaxial wafers as well as surface defects and contamination.

1.3 This terminology is applicable for use in connection with research, development, process control, procurement, and inspection of silicon material.

1.4 Originally the terms and definitions included in this standard were extracted from other ASTM Standards relating to silicon technology. The original source standards for such terms are identified by their designations immediately following the definition. All such standards are found in this volume of the *Annual Book of ASTM Standards*. More recently, new or revised terms and definitions have been balloted directly for inclusion in this standard; these terms have no designation following the definition.

1.5 Almost all of the terms listed are nouns; in other cases, the part of speech is given explicitly immediately following the term.

2. Referenced Documents

2.1 SEMI Standards:²

M1 Specifications for Polished Monocrystalline Silicon Wafers

M18 Format for Silicon Wafer Specification Form for Order Entry

3. Terminology

3.1 Terms and Their Definitions:

acceptor—an impurity in a semiconductor that accepts electrons excited from the valence band, leading to hole conduction.

accumulation condition—the region of the C–V curve for which a 5-V increment toward a more negative voltage for

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² Available from Semiconductor Equipment and Materials International, 805 E. Middlefield Rd., Mountain View, CA 94043.

p-type material, or toward a more positive voltage for *n*-type material, results in less than a 1 % change in the maximum capacitance, $C_{\max}$. **F 1153**

anisotropic, *adj.*—exhibiting different physical properties in different directions.

DISCUSSION—In semiconductor technology, the different directions are defined by the crystallographic planes.

anisotropic etch—a selective etch that exhibits an accelerated etch rate along specific crystallographic planes.

DISCUSSION—Anisotropic etches are used to determine crystal orientation, to facilitate dielectric component isolation, and to fabricate micromechanical structures.

area contamination—on a semiconductor wafer, matter, unintentionally added to the surface of the wafer, of extent greater than a single localized light scatterer.

DISCUSSION—Area contamination may be foreign matter on the wafer surface resulting from chuck marks, finger or glove prints, stains, wax or solvent residues, etc.

area defect—*not preferred*, see **extended light scatterer**.

azimuth—in *ellipsometry*, the angle between the major axis of the ellipse and the plane of incidence.

autodoping—of an epitaxial layer, incorporation of dopant originating from the substrate into epitaxial layer. Also called **self-doping**.

backside—Not preferred, use **back surface**.

back surface—of a semiconductor wafer, the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated. **F 523, F 533, F 534**

bevel angle, α —the smaller of the angles between the wafer surface and the section plane. **F 950**

bipolar—semiconductor device fabrication technology that produces transistors that use both holes and electrons as charge carriers.

birefringence—a double-refraction phenomenon in which an unpolarized beam of light is divided into two beams with different directions and relative velocities.

block structure—See **cell structure**. **F 154**

bow—of a semiconductor wafer, the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer. **F 534**

buried layer—a diffused region in a substrate that is, or is

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intended to be, covered with an epitaxial layer.

carrier—in *semiconductor materials*, an entity capable of carrying electric charge through a solid, for example, valence holes and conduction electrons in semiconductors. Also called **charge carrier**.

carrier density, n (electrons); p (holes)—the number of majority carriers per unit volume in an extrinsic semiconductor, usually given in number/cm³ although the SI unit is number/m³. **F 723**

cell structure—malformations attributable to crystal inhomogeneities and that have their origins in the crystal growth process. Also known as **block structure**. **F 154**

chemical vapor deposition—in *semiconductor technology*, a process in which a controlled chemical reaction produces a thin surface film.

DISCUSSION—Epitaxial growth is an example of a special case of chemical vapor deposition (CVD).

chem-mechanical polish—in *semiconductor technology*, a process for the removal of surface material from the wafer that utilizes chemical and mechanical actions to achieve a mirror-like surface for subsequent processing.

chip—in *semiconductor wafers*, region where material has been unintentionally removed from the surface or edge of the wafer.

chuck mark—any physical mark on either surface of a wafer caused by robotic end effector, a chuck, or wand.

cleavage plane—a crystallographically preferred fracture plane.

coherence—a measure of the ability a source of electromagnetic radiation has to interfere.

compensation—reduction in number of free carriers resulting from the presence of impurities other than the majority dopant density impurity. **F 723**

concentration—relative amount of a minority constituent of a mixture to the majority constituent (for example parts per million, parts per billion, or percent) by either volume or weight. **F 723**

conductivity (electrical)—a measure of the ease with which charge carriers flow in a material; the reciprocal of resistivity.

DISCUSSION—In a semiconductor, the conductivity is proportional to the product of free carrier density, electron charge, and carrier mobility. Most variant of all crystal properties, conductivity can range over 13 orders of magnitude. Conductivity can be locally modified by temperature, carrier injection, irradiation, or magnetic field. Symbol is σ and units are ($\Omega \cdot \text{cm}$)⁻¹.

conductivity type—of a *semiconductor crystal or wafer*, a property that identifies the majority charge carrier in the semiconductor. See also **n -type, p -type**.

contamination—on a *semiconductor wafer*, see **area contamination** or **particulate contamination**.

crack—on *semiconductor wafers*, cleavage or fracture that extends to the surface of a wafer and which may or may not pass through the entire thickness of the wafer. **F 154**

cratering—a surface texture of irregular closed ridges with smooth central regions. **F 523**

crests—structures with parallel major axes, attributed to

substrate defects either above or below the surface plane of silicon substrates after epitaxial deposition (see also **fish-tails**). **F 154**

crow's-foot—on *semiconductor wafers*, intersecting cracks in a pattern resembling a "crow's foot" Y on {111} surfaces and a cross "+" on {100} surfaces. **F 154, F 523**

crystal—a solid composed of atoms, ions or molecules arranged in a pattern that is periodic in three dimensions. **F 47**

crystal defect—departure from the regular arrangement of atoms in the ideal crystal lattice.

crystal indices—See **Miller indices**.

crystal originated particle (COP)—a surface depression that is formed during soft alkaline chemical treatment of silicon wafer surfaces that contain crystal defects at or close to the wafer surface and that scatters light similarly to a very small particle, also called **surface micro defect (SMD)**.

DISCUSSION—Soft alkaline chemical treatment may consist of cleaning with a 5:1:1 H₂O-NH₄OH-H₂O₂(SC-1) solution, chem-mechanical polishing, etc.

crystallographic notation—a symbolism based on Miller indices used to label planes and directions in a crystal as follows:

plane	(111)	direction	[111]
family of planes	{111}	family of directions	<111>

damage—a defect of the crystal lattice of a single crystal silicon specimen in the form of irreversible deformation that results from mechanical surface treatments such as sawing, lapping, grinding, sandblasting, and shot peening at room temperature without subsequent heat treatments. **F 950³**

damage depth, T_z —the maximum thickness of the damage region as revealed by preferential etch that removes silicon in the region of the deformation. **F 950³**

deep level impurity—a chemical element that when introduced into a semiconductor has an energy level (or levels) that lies in the mid-range of the forbidden energy gap, between those of the dopant impurity species. **F 723**

depletion layer—a region in which the mobile carrier charge density is not sufficient to neutralize the net fixed charge density of donors and acceptors. Also known as **barrier layer, blocking layer, or space-charge layer**.

depletion width—the width of the region in a semiconductor near a metal-semiconductor contact in which the charge-carrier density is insufficient to neutralize the fixed-charge density of donors and acceptors. **F 108**

diameter—of a *semiconductor wafer*, the linear dimension across the surface of a circular wafer that contains the wafer center and excludes flats or other peripheral fiducial geometries. **F 613³**

diffused layer—a region of opposite conductivity type formed near the surface of a semiconductor crystal as a result of the introduction of impurities into the silicon crystal by means of solid state diffusion. **F 110**

dimple—a shallow depression in a wafer surface, with a concave, spheroidal shape and gently sloping sides.

³ These citations indicate definitions that have been edited or otherwise differ from the definition in the source document.

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DISCUSSION—Dimples are macroscopic features that are visible to the unaided eye under proper lighting conditions.

dirt—on semiconductor wafers, surface contaminant that cannot be removed by pre-inspection solvent cleaning. **F 154**

dislocation—a line imperfection in a crystal that either forms the boundary between slipped and nonslipped areas of a crystal or that is characterized by a closure failure of Burger's circuit. **F 47³**

donor—an impurity or imperfection in a semiconductor that donates electrons to the conduction band, leading to electron conduction.

dopant density—in an uncompensated extrinsic semiconductor, the number of dopant impurity atoms per unit volume, usually given in atoms/cm³ although the SI unit is atoms/m³. Symbols: N_D for donor impurities and N_A for acceptor impurities. **F 723**

doping—addition of impurities to a semiconductor to control the electrical resistivity.

edge effect—localized structure about the edge of a specimen. **F 154**

edge profile—on edge contoured wafers (whose edges have been shaped chemically or mechanically), a description of the contour of the boundary of the wafer that joins the front and back surfaces.

effective electrical contact radius, (cm)—of a spreading resistance probe assembly, an empirical quantity defined by

$$a = np/4R_s$$

where:

n = number of current-carrying probes across which the potential drop is determined,

p = resistivity of a homogeneous semiconductor specimen, $\Omega \cdot \text{cm}$, and

R_s = measured spreading resistance, Ω .

F 525, F 672

ellipticity—in optics, of elliptically polarized light, the angle x given by the inverse tangent of the ratio of the minor to the major axis of the ellipse described by the electric vector of the light. **F 576**

epitaxial layer—in semiconductor technology, a layer of a single crystal semiconducting material grown on a host substrate which determines its orientation.

equilibrium capacitance—that capacitance reached after an MOS specimen at a fixed bias is illuminated and then allowed to stabilize in darkness. **F 1153**

etch, n —a solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material either selectively or nonselectively. See also **anisotropic etch, preferential etch**.

etch pit—a pit, resulting from preferential etching, localized on the surface of a wafer at a crystal defect or stressed region.

extended light scatterer (XLS)—a feature larger than the spatial resolution of the inspection equipment, on or in a wafer surface, resulting in increased light scattering intensity relative to that of the surrounding wafer surface.

DISCUSSION—Origins of XLSs include area contamination and unresolved clusters of localized light scatterers, such as particles or COPs.

When observed by the unaided eye, an XLS can usually be seen under high intensity illumination. Some automated inspection instruments have sensors for reporting XLSs. XLSs can be observed as increased haze under dark field conditions. Under bright field conditions, an XLS can be observed as a decrease in the intensity of the specularly reflected beam, sometimes called a **light channel defect**.

fast axis—in optics, of a doubly refracting crystal, that direction in which the velocity of light is a maximum. **F 576**

fishtails—structures, attributed to substrate defects, either above or below the surface plane after epitaxial deposition, which have their "tails" aligned in a particular crystallographic direction (see also **crescents**). **F 154**

fixed quality area (FQA)—central area of a wafer surface, defined by a nominal edge exclusion, X , over which the specified values of a perimeter apply.

DISCUSSION—The boundary of the FQA is at all points the distance X away from the periphery of a wafer of nominal dimensions.

flake chip—See **peripheral chip**. **F 154³**

flat—on a semiconductor wafer, a portion of the periphery of a circular wafer that has been removed to a chord. See also **primary orientation flat, secondary flat**.

flatband condition—in microelectronics, the point at which an external applied voltage causes there to be no internal potential difference across an MOS structure. **F 1153**

flatband voltage, V_{fb} —the applied voltage necessary to produce the flatband condition. **F 1153**

flatband capacitance, C_{fb} —the capacitance of an MOS structure at the flatband voltage. **F 1153**

flatness—for wafer surfaces, the deviation of the front surface, expressed in TIR or maximum FPD, relative to a specified reference plane when the back surface of the wafer is ideally flat, as when pulled down by a vacuum onto an ideally clean flat chuck.

focal plane deviation (FPD)—on a wafer surface, the distance parallel to the optical axis from a point on the wafer surface to the focal plane of the optical system.

four-point probe—an electrical probe arrangement for determining the resistivity of a material in which separate pairs of contacts are used (1) for passing current through the specimen and (2) measuring the potential drop caused by the current.

front side—Not preferred, use **front surface**.

front surface—of a semiconductor wafer, the exposed surface upon which active semiconductor devices have been or will be fabricated. **F 523, F 533, F 534**

gettering—the process that immobilizes impurities at locations away from the region of the specimen to be investigated. **F 416**

goniometer—an instrument to measure angles.

DISCUSSION—A goniometer is frequently used with X-ray diffraction equipment to measure crystal axis angles or for optical angle measurement.

grain boundary—the surface that may be closed over which a crystal is in contact with other crystals in a solid body. **F 47**

groove—in a semiconductor wafer, a shallow scratch with rounded edges, that is usually the remnant of a scratch.