

Engineering diagram drawing practice

Part 4: Recommendations for logic diagrams

Committees responsible for this British Standard

The preparation of this British Standard was entrusted by the General Mechanical Engineering Standards Policy Committee (GME/-) to Technical Committee GME/4 upon which the following bodies were represented:

- Amalgamated Union of Engineering Workers (Technical and Supervisory Section)
- British Engine Group of SMMT
- British Paper and Board Industry Federation
- British Railways Board
- British Standards Society
- Drawing Office Material Manufacturers' and Dealers' Association
- Electricity Supply Industry in England and Wales
- Electronic Engineering Association
- Engineering Equipment and Materials Users' Association
- Gauge and Tool Makers' Association
- Institution of Electrical Engineers
- Institution of Engineering Designers
- Institution of Mechanical Engineers
- Society of British Aerospace Companies Limited
- Telecommunication Engineering and Manufacturing Association
- United Kingdom Atomic Energy Authority

The following bodies were also represented in the drafting of the standard, through subcommittees and panels:

- British Coal Corporation
- British Shipbuilders
- British Telecommunications plc
- GAMBICA (BEAMA Ltd.)
- Independent Broadcasting Authority

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Foreword

This part of BS 5070 has been prepared under the direction of the General Mechanical Engineering Standards Policy Committee. It introduces logic diagrams to form a fourth part of BS 5070. The 1974 edition of BS 5070, which was withdrawn with the completion of its revision into three parts in 1988, set out recommendations for drawing practice to be followed in preparing engineering diagrams in all fields of engineering with a view to securing uniformity between one drawing office and another in the same industry. It also aimed to increase uniformity between one field of engineering and another in the basic principles involved and in the designations for different types of diagram.

Attention is drawn to BS 5070 being a companion standard to BS 308; the latter covers engineering drawing practice used in a wide range of engineering disciplines. Commonly, as a diagram can be called a “drawing” and a drawing can be called a “diagram”, it is useful to summarize the difference in the scopes of these standards. BS 308 covers what are commonly accepted to be drawings that define shape, size and form. BS 5070 covers the drawing of diagrams that are normally associated with flow of one sort or another and which relate components (usually indicated by symbols) functionally one to another by the use of lines, but do not depict their shape, size or form; neither do they in general indicate physical connections or locations.

From experience with the 1974 edition it was decided that for the first revision, whilst bearing in mind the long term aim of uniformity of conventions, there was a need for more comprehensive treatment of the varying requirements of differing industries and for more careful attention to their presentation. BS 5070 is therefore now revised in parts by which the practice and conventions of several disciplines and industries are collected into three groups. Part 1 covers general principles common to all subsequent parts, which in turn deal particularly with electrotechnology; control, flow and systems; and logic.

BS 5070 gives recommendations for the drawing of engineering diagrams using the symbols given in relevant British Standards. It does not itself originate symbols. The diagrams in this standard contain symbols as they appear in the particular standards current at the time this publication was prepared. However, although every effort has been made to ensure that correct and current symbols have been used, it has to be recognized that the particular symbols standards are themselves subject to periodic review. It is therefore stressed that the relevant symbols standards, and not this standard, have to be consulted to obtain definitive symbols.

The recommendations of this standard have been established having regard to the requirements of microfilming. Diagrams prepared in accordance with this standard should be suitable for microfilming and reduced-size reproduction techniques.

During the course of the first revision particular attention has been paid to developments in computer aided machine draughting and it has been established that such machines are currently capable of complying with this standard. Any minor exceptions due to the limitations of a particular system would not be expected to prejudice the understanding of a diagram otherwise claimed to comply with this standard.

It is recognized that though this standard is published in a number of parts, there may be instances when certain recommendations and descriptions are repeated. This has been kept to a minimum and it is hoped that all the needs of any specialized engineering discipline are contained in the part of BS 5070 that deals with those specific needs.

This part of BS 5070 deals with logic diagram drawing and follows the recommendations being formulated internationally through the International Electrotechnical Commission (IEC).

Part 1 deals with general principles of diagram drawing and is the base document. Part 2 deals with all forms of diagrams in electrical, electronics and telecommunications engineering. Part 3 deals with a variety of non-electrical diagrams including those concerned with control and flow; transfer of materials (both solids and fluids, i.e. liquids, vapours and gases); and energy transfer (hydraulic, pneumatic and mechanical).

Compliance with a British Standard does not of itself confer immunity from legal obligations.

Notes on the presentation of this standard

NOTE 1 The figures illustrating the text in this standard are independent and each is selected solely for its simplicity and clarity to illustrate only the text to which it relates. They are not the only possible examples and they are not intended as design examples or to be fully working diagrams, but otherwise are drawn according to the basic recommendations of this standard.

NOTE 2 Numerical values of components given in the figures throughout are arbitrarily chosen to assist in illustrating the point under consideration; they are typical and are not given as recommendations.

NOTE 3 In the illustrations to this standard, a convention is adopted of using capital letters for notes that would appear as part of the drawing and lower case letters are used for notes explaining the point under consideration in relation to the text.

Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, pages 1 to 40, an inside back cover and a back cover.

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Introduction

A symbol for a binary logic element may represent either a concept, i.e. a theoretical or an ideal item, or a real hardware item. In programmable equipment the symbols are used to represent programme elements in modules. Binary logic is concerned with variables, each of which may take up one of two states. These states may be described by terms such as ON and OFF, YES and NO, TRUE and FALSE or more usually as the logic 1-state and the logic 0-state.

The symbols for logic functions in BS 3939-12 represent the relationship between the inputs and outputs in terms of logic states. They may therefore be used in diagrams representing abstract logic designs and no difficulties of interpretation should arise. At this stage no knowledge is needed as to what type of device (e.g. electric, fluidic) will eventually be used to implement the design.

As soon as hardware items are selected to carry out the desired logic functions it becomes necessary to decide on the physical quantities that will be used to represent the logic states. With electrical devices it is usual to select electrical potential as the physical quantity and to assign values to represent the logic states. However, for other possibilities see 6.3. Absolute figures are not normally used and the values are merely identified as more positive or less positive. These two values are known as logic levels.

This part of BS 5070 uses the symbols 0 and 1 to identify the two logic states of a binary variable. These states are referred to as the 0-state and the 1-state. A binary variable may be related to any physical quantity for which two distinct ranges can be defined. In this standard, these distinct ranges are referred to as logic levels and are denoted H and L. H is used to denote the logic level with the more positive algebraic value, and L is used to denote the logic level with the less positive algebraic value. In cases where the logic levels are equated with other qualities of physical quantity (e.g. positive or negative pulses, presence or absence of a pulse) H and L may be used to represent these qualities or may be replaced by more suitable designations.

1 Scope

This part of BS 5070 gives recommendations for the practice to be followed in preparing logic diagrams and the application of binary logic symbols for such diagrams. It should be read in conjunction with Part 1 and Part 2. Analogue and hybrid techniques have not been considered.

This part is applicable to those forms of integrated circuit design in which the basic logic circuit elements are predefined cells which are laid out and interconnected in a manner similar to packages on a printed circuit board. These integrated circuits are known as uncommitted logic arrays, gate arrays, or standard cell arrays.

NOTE 1 The logic circuit diagrams will not contain internal pin numbers, but in all other respects should have the characteristics of the diagrams shown as examples in this standard.

NOTE 2 The symbols and descriptions have been prepared with a view to electrical applications but they are equally applicable to other, non-electrical systems such as pneumatic, hydraulic or mechanical.

NOTE 3 The titles of the publications referred to in this standard are listed on the inside back cover.

2 Definitions

For the purposes of this part of BS 5070 the following definitions apply.

2.1

logic diagram

a diagram that uses symbols for binary logic elements to depict the overall function of a system in terms of logic stages and is not necessarily related to physical implementation

2.2

logic circuit diagram

a diagram that shows the practical implementation of a logic diagram. This diagram will also show components that are not logic stages but are necessary to make the system work

NOTE When the logic diagram is to be implemented in a practical form, a more detailed diagram has to be prepared that shows symbols for the actual gates used (see also clause 7).

2.3

stage

an element or group of elements that act(s) upon one or more incoming signals to develop one or more output signals, the two types of which are:

- a) *logic stage*. A stage that performs a logic function e.g. AND, OR, NEGATION, delay or storage
- b) *non-logic stage*. A stage that performs a non-logic function e.g. amplification, pulse regeneration, adjustment of levels, impedance transformations, etc

2.4

positive logic convention

the representation of the 1-state and the 0-state by the High (H) and Low (L) levels respectively

2.5

negative logic convention

the representation of the 1-state and the 0-state by the Low (L) and High (H) levels respectively

2.6

polarity indicator convention

the designation of the internal state produced by the external level of an input, or producing the external level of an output, by the presence or absence of the polarity indicator symbol

2.7

logic state

one of two possible abstract states that may be taken on by a logic (binary) variable, the two types of which are:

- a) *0-state*. The logic state represented by the binary symbol 0 denoting a false logic condition
- b) *1-state*. The logic state represented by the binary symbol 1 denoting a true logic condition

2.8

internal logic state

the logic state assumed to exist inside an element symbol outline at an input or output

2.9

external logic state

the logic state assumed to exist outside an element symbol outline:

- a) on an input line prior to any external qualifying symbol of that input, or
- b) on an output line beyond any external qualifying symbol at that output

2.10

logic level

any level within one of two non-overlapping ranges of value of a physical quantity used to represent the logic state, the two ranges of which are:

- a) *high (H) level*. A level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states
- b) *low (L) level*. A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states

2.11

negation bar

a line over a signal name that indicates the logic complement of that signal

2.12

signal name

a label, usually a mnemonic¹⁾, that identifies a signal or a signal line

¹⁾ Mnemonic is a term commonly used to describe symbolic abbreviations for signal names of logic systems (see also Appendix A).

3 Symbols

3.1 General

Rules for the use and combination of symbols for binary logic elements are given in BS 3939-12. Symbols representing hardware elements which are contained in one physical package may also be combined providing the interconnections are not accessible to the user and the quoted rules are applied.

Each logic element should be shown by that symbol which correctly depicts the logic function actually performed by that element in the system.

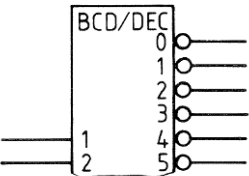
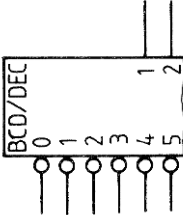
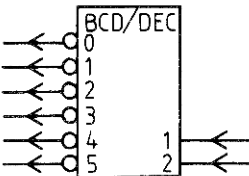
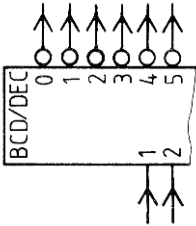
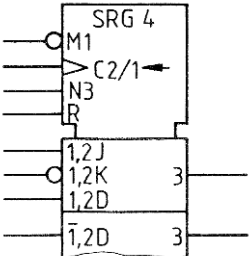
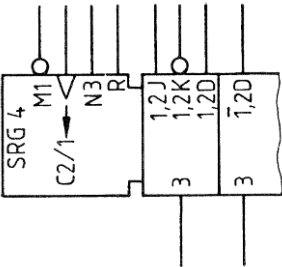
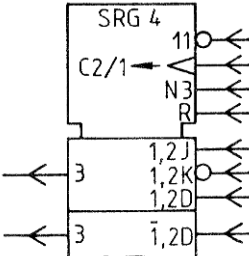
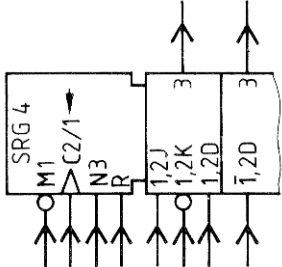
3.2 Orientation

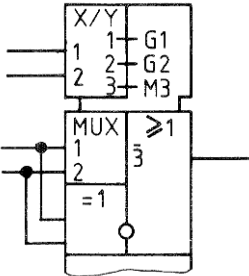
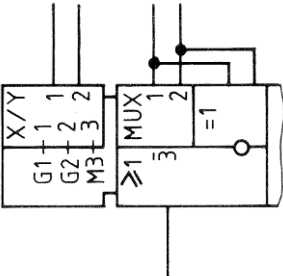
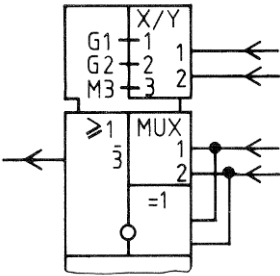
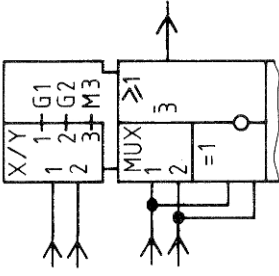
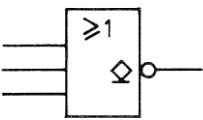
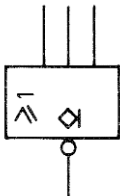
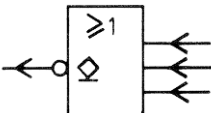
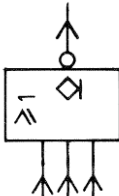
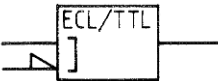
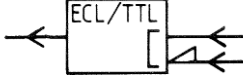
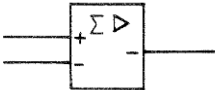
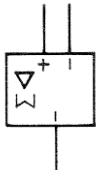
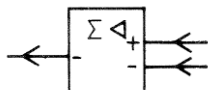
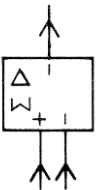
The preferred orientation of symbols is for inputs to be on the left and outputs to be on the right. However, alternative orientations are permissible, as shown in Table 1, providing the following rules are observed.

- The rules for the placement of the qualifying symbol(s) for the device function should be obeyed (see BS 3939-12).
- In general, outputs should appear on the opposite side of the symbol outline from the inputs.
- Sufficient space should be provided to avoid confusion between the qualifying symbol(s) for the function and the input and output labels.
- Strings of characters, forming qualifying symbols or labels, should preferably appear in normal reading order and each input (output) label should be centred with respect to its input (output) line.
- The orientation of qualifying symbols for negation, polarity, grouping dynamic inputs, inhibit and amplification with respect to the connection lines should remain unchanged.
- Where the signal flow is from right to left or from bottom to top, directional arrows should be used on the signal line.

Examples of orientation of symbols are given in Table 1.

Table 1 — Orientation of symbols

Left to right	Top to bottom	Right to left	Bottom to top
			
			

Left to right	Top to bottom	Right to left	Bottom to top
			
			
			
			

3.3 Complex logic units

Symbols for complex logic units should be developed in accordance with the rules given in BS 3939-12. If this is not possible owing to the complexity of the function, then the symbol used can be a simple rectangle containing a description of the function or a reference to the appropriate documentation. Uniform labels should be used for inputs and outputs where possible.

If a symbol for a complex function has to be repeated on a diagram each repetition may be shown as a simple rectangle with appropriate references.

3.4 Representation of unused elements

Any elements of a multiple package which are not used, e.g. inputs or outputs or complete elements within a multiple package, may be shown. When shown it is important to identify the unused elements and the corresponding pin numbers.

4 Signal names and characteristics

4.1 General

The labelling of lines will greatly enhance the understanding of a diagram and facilitate the maintenance of a logic system, provided that the signals are named intelligently and that the allocation is based on carefully named system functions.

In general, the characters comprising the total signal identification provide two types of information:

- a) the signal name which gives a functional description;
- b) information which relates the logic state of a function with its logic level (used only on diagrams employing the polarity indicator).

To ensure correct interpretation different signal lines should have different signal names, e.g. if a signal is gated with another, is delayed, chopped or stored. On the contrary, a signal should not change its name as a result of being inverted, amplified or level shifted.

Serial numbers should be used to avoid confusion with similar signal names, e.g. ALARM-1, ALARM-2, GR-1, STOP-1, STOP-2 (or STOP-1 -N, STOP-2-N).

The space on a diagram or in a data file usually limits the allowable length of signal names. Therefore every effort should be made to use mnemonic and standard abbreviations. The mnemonics and abbreviations should be explained on the diagram or in the associated documentation.

Signal names should be composed from standard character sets, excluding lower case letters. In addition, a single character space may be used where necessary, although the use of a dot as a separator often proves advantageous over a space.

NOTE Design automation may place certain constraints on the use of characters.

There is no restriction as to the use of a language for the formation of signal names. The signal names used in this standard may therefore not necessarily be translated literally when using another language.

4.2 Binary signals

The signal name is a mnemonic for a statement which can be either true or false. For example, the name ALARM is associated with the statement ALARM IS PRESENT.

True and complement signals of the same function are often required. The preferred method to denote the complement of a signal is to use a negation bar over the signal name, thus: ALARM. If only an in-line notation can be used the preferred presentation is ALARM-N.

The convention for the relationship between the true and false states of a statement represented by a signal name, and the corresponding logic states of the signal to which that name is assigned, is as follows.

True corresponds to the logic 1-state;

False corresponds to the logic 0-state.

For example, the signal name ALARM implies that if ALARM is true, the signal is in its 1-state. Conversely, ALARM implies that if ALARM is true, the signal is in its 0-state.

If possible, signal names should be inherently true, e.g. STOP. Signal names that embody an inherent negative such as NORUN should be avoided.

In some cases it may be desirable to employ the solidus (/) as the logical OR symbol and normal juxtaposition to indicate the logical AND. For example, RD/WD (READ OR WRITE) and AUTSTART (AUTOMATIC MODE AND START COMMAND) may be such signals.

The plus sign (+) denotes algebraic addition and the minus sign (–) algebraic subtraction. For example, MAR+1 may be the signal name for MEMORY ADDRESS REGISTER PLUS 1.

The use of logic equations in signal names is not recommended.

Where possible, signals should be named by the function they perform instead of the function of the source that generated them. For example, assume that a signal PRUN is gated with a second signal, TP6, to set a bistable element called RUN. If the output signal is called SETRUN, its function is obvious. However, if it is called PRUNTP6 its use is open to speculation.

Some signals perform such varied functions that it is not feasible to label them according to their use. For example, the alternative instructions to READ or WRITE may control large blocks of logic elements. In this event it would be proper to name the signal RD/WR (READ OR WRITE). For examples of signal name allocation see Figure 1.

Confusion sometimes arises in assigning signal names when the true state causes one action and the false state causes a different action. For example, a bistable element may select device A when cleared and device B when set. In this event the signal name should not refer to either device A or B. It should be such as SELDEV, with a note on the diagram to explain the action causing selection of device A or B.

If it is desirable to inform the user of the fact that a signal originates at a bistable element, the suffix FF may be used, e.g. STARTFF. Other useful suffix letters are:

A	movement forward, e.g. STARTA
B	movement backwards
C	movement clockwise
CC	movement counter-clockwise
D	movement downwards
F	movement fast
L	movement to the left
R	movement to the right
S	movement slow
U	movement upwards
X	movement command executed, e.g. STARTX

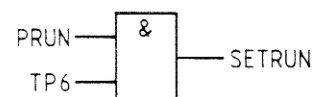
No set rules can avoid the necessity for the designer to execute good judgement and for the user to know how to interpret the significance of signal names.

Appendix A lists commonly used abbreviations and is an effort to unify some of the main signal names of logic systems.

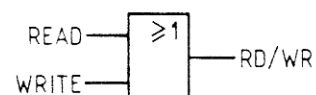
NOTE The examples given in the list represent typical usage in the English language and cannot all be translated without risk of confusion.

New signal names may be assigned according to the recommendations set out in this standard and other meanings may be assigned to the ones listed in Appendix A if no ambiguity results.

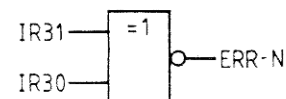
Labelling of an output of a combinative element.
PRUN may stand for PRE RUN and TP6 for TIMING PULSE 6.



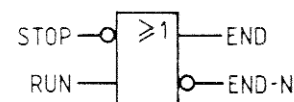
Expression of alternatives as part of a signal name.
RD/WR here stands for READ OR WRITE.



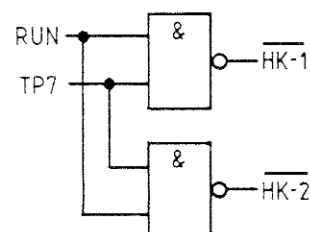
Labelling of a negated output of a combinative element in in-line notation.
ERR may stand for ERROR and IR for INTERMEDIATE REGISTER.



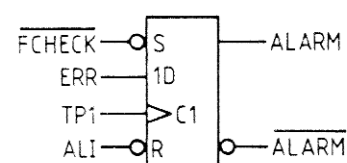
Labelling of the complementary outputs of a combinative element in in-line notation.



Use of serial numbers to identify two outputs carrying the same signal.
HK may stand for HOUSEKEEPING.



Labelling of the complementary outputs of a bistable element.
FCHECK may stand for FUNCTION CHECK and ALI for ALARM INHIBIT.



Labelling of the complementary outputs of a bistable element which is wired up from an AND-OR-NOT element.
RESRUN may stand for RESET RUN.

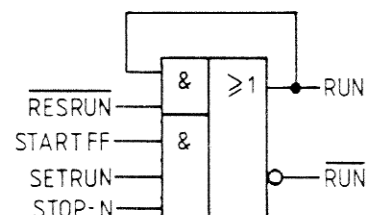
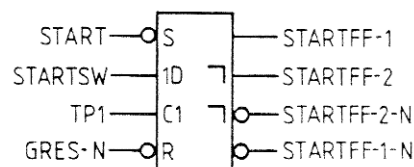


Figure 1 — Examples of signal name allocation

Labelling from the complementary outputs of both the master and slave stages of a bistable element when attention should be drawn to the fact that these signals originate from a bistable element.



Extensive use of serial numbers to identify the various trees of a signal originating at a bistable element.

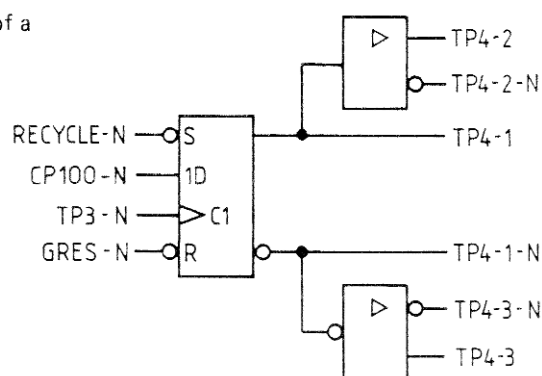


Figure 1 — (concluded)

4.3 Clock pulses

The basic clock and all clocks derived from it may be designated by CP and identified by the clock period. If the basic clock is, for example, 25 ns, the mnemonic might be CP25N. Clocks derived from the basic clock might then be termed CP50N, CP100N and so on.

The timing pulses derived from the clock pulses may be designated by TP and identified by a serial number which indicates their respective order of appearance.

Pulses which are delayed, stretched or shortened may be identified by a suffix D, L or S respectively, e.g. TP1D, TP2L, TP2DL, TP4S may represent such pulses.

Examples of clock pulses are given in Figure 2.

4.4 Bit and byte labelling

To accord with normal reading order, bit and byte labelling should proceed from the most significant to the least significant. Representation should be in order of significance from bottom to top or from right to left (see Figure 3).

4.5 Bus lines

Bus lines may be designated by the term BUS. For example, CBUS00 may be the signal name for line 00 on bus C.

5 Logic diagrams

5.1 Logic states

In logic diagrams a distinction is made at each logic element between the internal logic state and the external logic state.

The logic operation represented by the qualifying symbol is performed on the internal logic states (see Figure 4).

5.2 Negation in logic diagrams

The negation indicator at an input or output indicates that the internal logic state is opposite to the external logic state for that particular input or output. For inputs and outputs without the negation indicator, the internal logic state is equal to the external logic state (see Figure 5 and Figure 6).

The circle depicting the negation indicator should touch the external outline of the symbol. The input or output line may be drawn through the circle. There is no preference for the correct placing of the negation indicator either at the input or at the output. Negation indicators should not be shown at more than one end of a line connecting devices, i.e. they should not be at both the driving end and at the driven end. (This would mean a double negation).

Table 2 gives the combinations that are possible for system condition, signal name, external logic state and internal logic state.

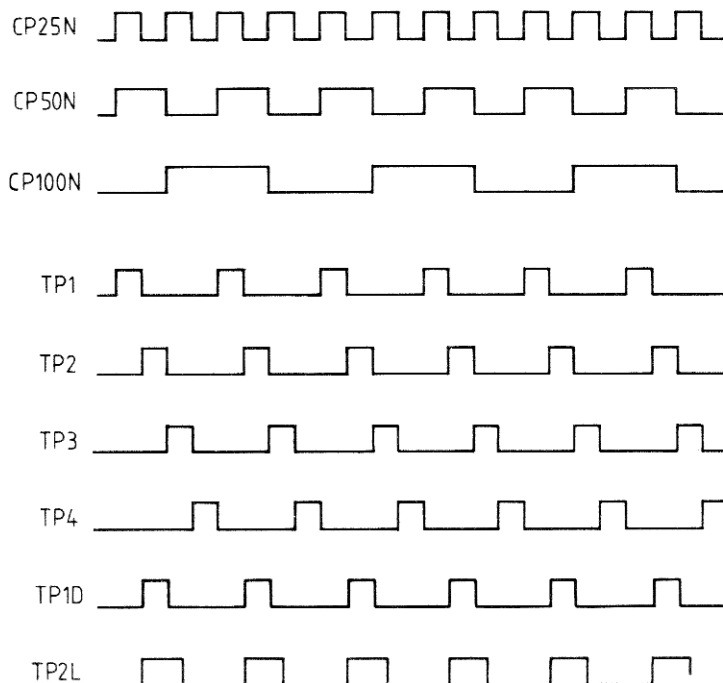


Figure 2 — Examples of clock pulses