

Printed wiring boards —

Part 23: Guide for the design and use of printed wiring boards: surface mounted devices

Committees responsible for this British Standard

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- Electronic Engineering Association
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Foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Policy Committee.

This Part of BS 6221 is a revision and expansion of clause 13 of BS 6221-3:1982 which is deleted by amendment.

The assembly of components on and repairs to printed wiring boards are matters of interest to the designer of printed wiring boards. This Part of BS 6221 should therefore be used in conjunction with Parts 2, 3, 20 and 21 of BS 6221.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, pages 1 to 30, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

1 Scope

This Part of BS 6221 provides guidance on the design of printed wiring boards for surface mounted components. In particular this guide addresses the following:

- a) substrates and mounting of surface mounting device (SMD) carriers;
- b) soldering process considerations;
- c) land design for SMD;
- d) recommended component layouts;
- e) testability.

2 Definitions

For the purposes of this Part of BS 6221 the definitions given in BS 6221-3 apply together with the following.

2.1

automatic component placement (ACP)

the placement of components onto or into their correct locations by a programmable machine

2.2

automatic placement equipment (APE)

a programmable machine, capable of handling components, moving them to a specific area and locating or inserting the component onto or into the correct location

2.3

dual in line package/lead (DIP/L)

an integrated circuit package that has a row of pins for through hole mounting along adjacent sides of the package

2.4

leadless ceramic chip carrier (LCCC)

a ceramic encapsulating package in which an integrated circuit can be mounted to form a surface mounting device. There are no leads, but pads around its perimeter for interconnection to a PWB land

2.5

plastic leaded chip carrier (PLCC)

a plastic encapsulating package in which an integrated circuit can be mounted to form a surface mounting device. A lead frame is formed around its perimeter for interconnection to a PWB land

2.6

printed wiring board (PWB)

a substrate upon which a pattern of conductive tracks is formed to interconnect the components which will be mounted upon it

2.7

plated through hole (PTH)

a hole in which metal is deposited on the wall

2.8

surface mounting component/device (SMC/D)

an electronic device designed for mounting on to lands on the surface of a substrate rather than by insertion into holes in the substrate

2.9

substrate

the basic material which forms the support structure of an electronic circuit

2.10

surface mounting

electrical connection of components on the surface of a conductive pattern without utilizing component holes

2.11

glass transition temperature (T_g)

the temperature at which a material changes from a glass like (rigid) state to a rubber like (flexible) state. The change is completely reversible and the material will behave like a glass below its T_g and a rubber above it

2.12

thermal coefficient of expansion (TCE)

the fractional change in the dimensions or volume of a material per unit change of temperature

2.13

via

an interlayer connection in a multi-layer board

2.14

small outline (SO)

a plastic encapsulating package in which an integrated circuit can be mounted to form a leaded surface mounting device. The leads are formed into a gull wing shape along the two longer sides for connection to PWB lands

2.15

node

a node is a point of connection between a component and a PWB land

2.16

cluster

a cluster is all nodes which are connected directly by PWB track

2.17

open node

a position at which a cluster may be accessed by a test probe

3 Design for surface mounting components

3.1 General

Surface mounted components offer many advantages to the printed board designer, including improved packaging and the subsequent increase in available board area for conductors, since component mounting holes are not required. For the purpose of this guide, the following surface mounting components are considered.

a) Leadless passive devices, for surface mounting:

- 1) chip components such as thick film resistors, tantalum capacitors and multilayer ceramic capacitors (see BS 9075 N001);
- 2) leadless components such as film resistors or cylindrical ceramic capacitors, generally known as metal electrode face bonding (MELF) components.

These may be used on entirely surface mounted assemblies or in conjunction with conventional leaded components mounted on either side of the board. In both cases they may be associated with active surface mounting devices.

b) leadless active device packages for surface mounting including leadless ceramic chip carriers (LCCCs) or plastic leaded chip carriers (PLCCs) that may require specialized mounting techniques or support mechanisms on leaded chip carriers.

c) Leaded active devices for surface mounting such as small outline (SO) devices and PLCCs.

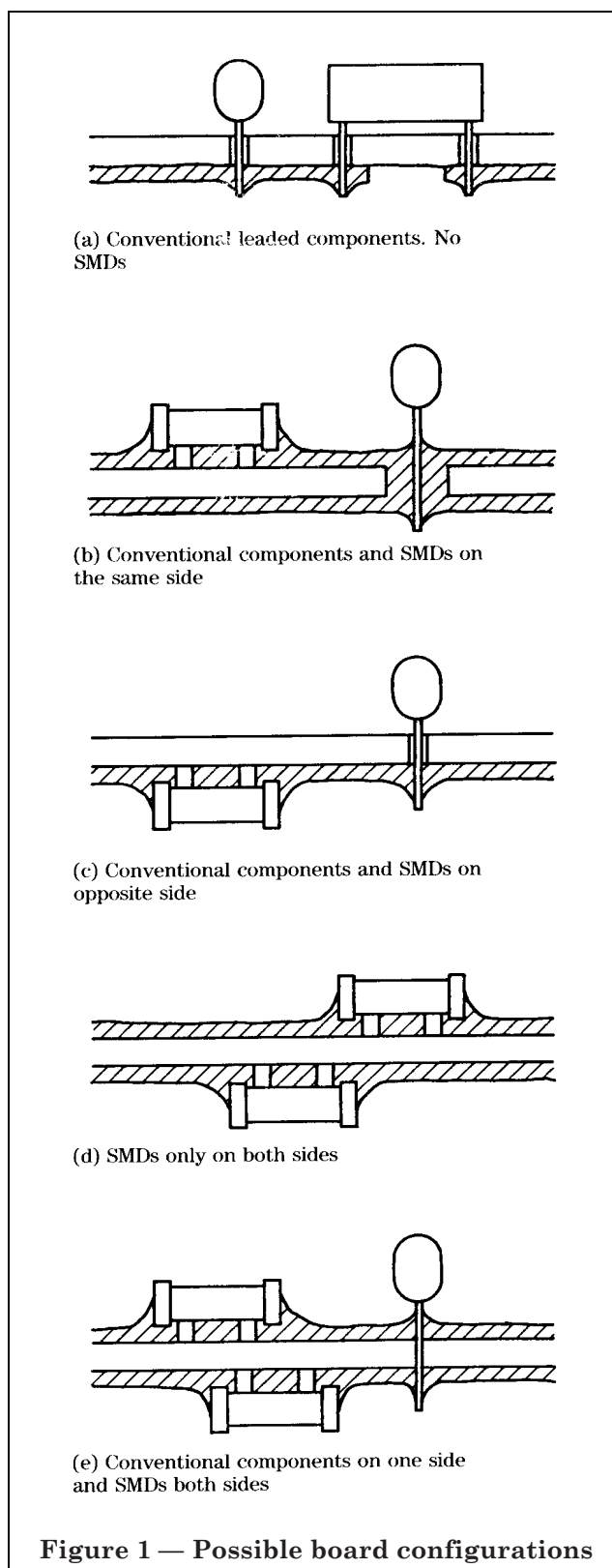
3.2 Design considerations

When designing printed wiring assemblies using surface mounted devices, consideration should be given to the following:

- a) process capabilities including placement and soldering methods;
- b) performance requirements;
- c) test philosophy;
- d) packing density;
- e) component types, i.e. conventional/surface mounted mix;
- f) substrate material.

The above factors will influence the resulting construction of printed wiring assemblies (PWAs). Some examples are illustrated in Figure 1.

Component land design depends on the type of component being used and in the case of chip type components the land shape is related to the degree of flexure the board has to withstand.



Well braced boards, fitted with stiffeners both longitudinally and vertically to prevent flexing or bowing of the board, can be designed with fairly generous land dimensions.

Boards without external mechanical support or metal cores do not provide a stable platform for chip components and the land area is more critical on this type of design.

The reason for this difference between well braced boards and unsupported boards is a result of the relative mechanical strengths of the chip component and the solder bond. If the board deforms as the result of applied load, bending stresses are set up which render the chip component liable to cracking. A large solder joint area provides rigid anchorage which is unlikely to deform before failure of the chip. A small solder joint can provide a degree of flexure as it is able to accommodate the small dimensional changes that occur.

4 Substrates and mounting of chip carriers

4.1 Introduction

The selection of a substrate for use with surface mounting components (SMCs) is an integral part of the design process for an assembly. In principle any substrate used for conventional printed wiring board (PWB) assembly can be used depending upon the assembly processes involved and the final application. The final choice of substrate will need to take into account such factors as the thermal coefficient of expansion (TCE), the likely power dissipation requirements, long term reliability and processing parameters.

Temperature changes may result in thermal mismatch between the component and the substrate causing either joint or component failure. Large pin count leadless ceramic packages (typically 28 pin or more) will need a thermally matched substrate or a substrate with a compliant layer to prevent failure of the solder joints, similar packages made of plastic are less likely to fail when operated under similar conditions mounted on a more conventional board.

The power dissipations of the components also need to be examined closely so that any integral heat sink necessary can be included in the substrate.

The ability of the substrate material to withstand the assembly processes involved in surface mounting technology also needs to be assessed. The various soldering techniques and cleaning processes used may adversely affect some substrate materials. Warping of the substrate during processing may give rise to many problems and loss of yield.

The dimensional stability of the substrate and the photo tools are factors that will become more critical as solder land geometries become smaller and design rules become more stringent.

Apart from the common PWB materials, e.g. phenolic resin bonded paper and the epoxide woven glass series, more substrates designed specifically for surface mounting applications are becoming increasingly available; each of these has its advantages and disadvantages which need to be considered for each application.

4.2 Metal cored substrates

The primary function of the metal core is to constrain the TCE of the substrate material to a factor comparable to that of ceramic packaged SMDs. Multilayer boards can be fabricated using this combination which has the added advantage of built-in thermal management and also the possibility of using the metal core as ground and/or power rails.

4.3 Resin and fabric substrates

Substrates with new resins designed for improved stability over wider temperature ranges are available for surface mount applications. These resins with higher glass transition temperatures (T_g) increase the temperature range over which the substrate's mechanical and electrical properties are maintained. The use of various resins and fabrics permits the tailoring of TCEs to minimize thermal mismatch problems and the fabrication of substrates to meet specific needs.

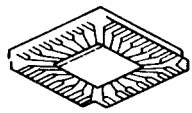
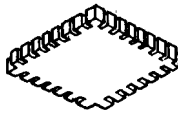
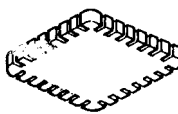
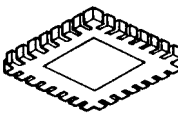
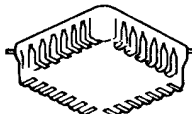
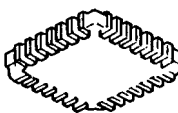
4.4 Leadless ceramic chip carriers (LCCCs) considerations

LCCCs are not suited to mounting on conventional printed boards due to the mismatch between the thermal expansion coefficient (TCE) of the chip ceramic substrate and the glass fibre laminate. The resulting solder joint stress due to thermal cycling of this combination can induce fractures at the joint or damage to the chip, e.g. in packs having pin counts of 28 or more. In addition the rigidity of a glass fibre board is insufficient to prevent fracture of the chip due to flexing.

To mount LCCCs it is therefore necessary to use a laminate whose mechanical and thermal attributes approach those of the chip substrate.

Insulating materials, such as thin glass fibre laminates, fusion bonded polyimide glass laminate or porcelain enamel on the metal base, provide the support for conventional etched conductors (in the case of copper clad insulant) or additive plating or thick film inks.

Table 1 — Mounting of ceramic devices

LCCC 1.27 mm pitch package		Mounting	
		Conventional printed board	Ceramic
Leadless type A		Socket	Socket
Leadless type B		Socket	Socket or solder
Leadless type C		Socket	Socket or solder
Leadless type D		Socket	Socket or solder
Leaded type A		Socket or solder	Socket or solder
Leaded type b		Solder	Solder
Mini-pak		Solder	N/A

By using thick film techniques and sequential layers of dielectrics, multi-layer metal cored materials may be constructed. Small via holes form layer interconnections and plated pillars, formed direct to the metal core, can be used for heat sinking.

Where thick film inks are used, interconnections between layers are provided by leaving voids in the interleaving dielectric and infilling the required via hole with a conductive material.

Conventional glass epoxide laminates can be used for LCCCs but a compliant surface may be required beneath the metal clad chip. In the build of the laminate an elastomeric layer is formed on the outer surface of the epoxide glass material and, depending on the process to be used, it is either copper clad or prepared for additive plating. The resultant printed board produced by this process still has the TCE of conventional glass epoxide materials but solder joint stress on LCCCs is greatly reduced due to the elastomeric coating. Flexing of the board is still a problem with this process and it is recommended that, where mechanical stress is possible, framed or stiffened boards should be used.

Sockets may be used to provide a semi-flexible interface between conventional board materials and LCCCs. However, depending on physical size constraints and socket reliability, the use of sockets is subject to individual application.

4.5 Plastic leaded chip carriers (PLCCs)

Plastic packages are more resilient to thermal shock than LCCCs and can be mounted on conventional printed board materials without special features.

The contact material used in PLCCs is of higher thermal conductivity than that used in ceramic devices and benefits can be gained from improved heat sinking ability into the solder lands.

4.6 Mounting considerations

The dimensions of LCCC and PLCC devices are controlled by JEDEC¹⁾. These devices are based on a contact pitch of 1.27 mm.

The primary differences between types are the internal features which affect the mounting orientations. The position of the cavity and its relationship to the back side of the die, which is the primary heat transfer source, varies between types of package.

In comparison most conventional DIPs are mounted in the "cavity up" configuration. This places the heat radiating surface down adjacent to the mounting surface and limits the heat transfer capability.

Table 1 gives recommendations for the mounting of ceramic devices.

Types A and D leadless devices are designed for "cavity down" mounting and are therefore suitable for use with heat sinks where the sink can be mounted directly on the primary heat radiating surface. Types B and C have a larger internal cavity but at the expense of lower thermal performance.

5 Soldering process considerations

5.1 Introduction

Designers of surface mounted assemblies should be aware of the different soldering process environment experienced by SMDs compared with that experienced by through hole leaded components. The critical difference is the substantially higher temperature experienced by an SMD when it is either wave or reflow soldered. The designer should ensure that the materials, from which the selected components are made, are able to withstand the extremes of temperatures encountered.

The following table gives an indication of the likely maximum time and temperatures that SMDs will experience during the soldering process.

Soldering method	Temperature	Time	Comments
Vapour phase 1	215 °C	1 min (note 1)	Immersed in vapour
Vapour phase 2	225 °C	1 min (note 1)	Immersed in vapour
Wave soldering	260 °C	6 s	Immersed in solder
Infra-red 1	400 °C	30 s	Shortwave infra-red (note 2)
Infra-red 2	200 °C	30 s	Longwave infra-red
NOTE 1 With larger assemblies that have large thermal masses, dwell times at the maximum temperature may need to be lengthened.			
NOTE 2 Maximum temperature achieved depends on the colour sensitivity of the components used.			

5.2 Designing for soldering

The criteria for a correct soldering process are three-fold:

- the solder reaches the solder land and the metallization of the device;
- there are no short circuits between devices or between devices and conductors;
- there are no flux residues trapped.

With through hole mounting using leaded devices, the solder can easily flow around the clinched end of the leads, and the flux gases can escape up the PTH. Two processes known to give satisfactory results for the majority of surface mounted devices are briefly described below:

- wave soldering;
- reflow soldering.

5.3 Wave soldering

SMDs are placed in close proximity to the substrate. This means that the solder cannot flow underneath the device to reach the metallization areas and needs to flow around the device. Thus in situations such as shown in Figure 2(a), one end of a device can block the other from the flow of solder (the so-called shadow effect). Obviously this phenomenon becomes more critical due to the high component densities that can be achieved with SMDs. Equally obviously, drag soldering is impractical since it relies on a horizontal flow of solder over the substrate.

¹⁾ JEDEC: US Joint Electronic Device Engineering Council.

Since good wetting cannot be achieved only with a horizontal flow of solder, Z-axis flow needs to be used in addition. Instead of moving the substrate through a bath of solder the solder is directed up against the underside of the board using a jet or wave of solder. However a relatively large amount of solder is required to accomplish good wetting and this can introduce short circuits.

Dual-wave soldering is one method to overcome this problem. The first wave directs a jet of solder up to ensure good wetting of the metallization areas. The second, gentler wave removes the excess solder and ensures that there are no short circuits.

The primary wave is sometimes followed by an “air knife”, which removes excess solder and bridges, thus dispensing with the need for a secondary wave.

Good wetting has to be accomplished in a limited time as the substrate moves through the bath; therefore to ensure that the wave reaches the solder land in time, it is recommended that the land be extended by approx. 0.4 mm.

With this extension the leading edge of the solder wave reaches and wets the land and as a result the rest of the wave can “creep back” and make a satisfactory solder joint.

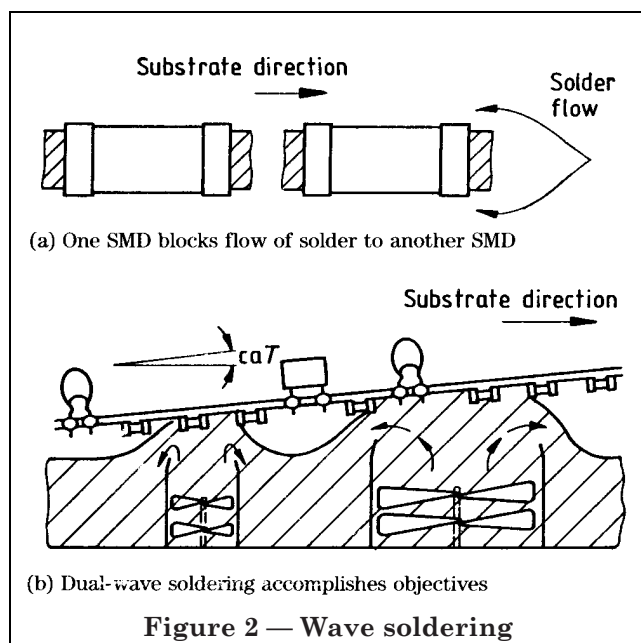


Figure 2 — Wave soldering

5.4 The infra-red (IR) reflow soldering process

In its basic form, an IR reflow machine consists of a conveyor passing between infra-red lamps. However, the reflow machine must provide temperature uniformity and stability across the entire working width of the conveyor, rapid response to variable product loading and multiple zone temperature control to tailor heat application to different products.

The radiation emission and intensity patterns of IR heaters depend not only on the energy of the heater, but also on the insulation materials, reflectors, covers and mounting arrangement.

The main criteria when selecting IR reflow soldering equipment is the temperature uniformity across the process width and the usable wavelength at relatively low temperatures (200 °C to 245 °C). The IR emission wavelengths in the middle to far infra-red zone (4 microns to 6 microns) are ideal for SMD reflow, since this range is close to the absorption wavelength of PWB laminates.

Temperature profiles can be closely controlled by the use of variable forced hot air recirculation within the IR chamber, thereby limiting the effect of shadowing.

IR machines developed for SMD assembly are usually computer controlled for maximum efficiency.

Solder is supplied to the assembly typically as paste before component placement.

5.5 The condensation reflow soldering process (vapour phase)

Condensation or vapour phase soldering is a mass reflow soldering process that utilizes the latent heat of vaporization of a saturated condensing vapour. When an assembly is immersed in such a vapour, condensation occurs almost simultaneously on all exposed surfaces, so that the shape and size of the assembly being soldered has little influence on the uniformity of heating as long as a saturated vapour is maintained. The release of the latent heat of vaporization heats the metals to be joined rapidly and uniformly to the vapour temperature and reflows the solder paste which is typically applied to the assembly before component placement.

5.6 Onsertion machine to pattern alignment

Whereas there are several methods available for the alignment of conventional drilled PWBs with their automatic component placement equipment (APE), a problem arises with surface mounted boards with no component mounting holes.