

Semiconductor devices: discrete devices and integrated circuits —

Part 1: Discrete devices —

Section 1.8 Recommendations for field-effect transistors

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- Electronic Engineering Association
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National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with IEC Publication 747-8 “*Semiconductor devices. Discrete devices and integrated circuits Part 8: Field-effect transistors*”, as amended by Amendment No. 1 published in July 1991, and Amendment No. 2 published in December 1993, by the International Electrotechnical Commission (IEC).

This British Standard constitutes Section 1.8 of the British Standard for semiconductor devices (BS 6493). (See national foreword of BS 6493-1.1:1984.)

Terminology and conventions. The text of the International Standard has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards.

Cross-reference

International Standard	Corresponding British Standard
IEC 747-1:1983	BS 6493 <i>Semiconductor devices: discrete devices and integrated circuits</i> Section 1.1:1984 <i>General</i> (Identical)

A British Standard does not purport to include all the necessary provisions of a contract. Users of British Standards are responsible for their correct application.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, pages 1 to 48, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Chapter I. General

1 Introductory note

As a rule, it will be necessary to use Publication 747-1 together with the present publication. In 747-1, the user will find all basic information on:

- terminology;
- letter symbols;
- essential ratings and characteristics;
- measuring methods;
- acceptance and reliability.

The sequence of the different chapters is in accordance with Publication 747-1, Chapter III, Sub-clause 2.1.

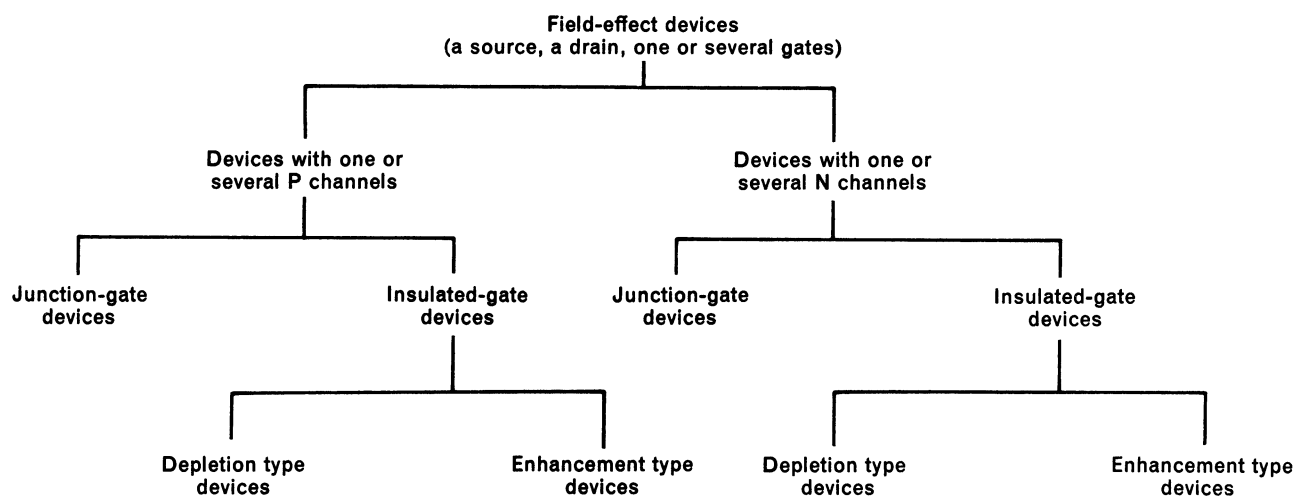
2 Scope

The present publication gives standards for the following categories of field-effect transistors:

- Type A: junction-gate type;
- Type B: insulated-gate depletion type;
- Type C: insulated-gate enhancement type.

3 Classification

Since a field-effect transistor may have one or several gates, the following classification results:



Chapter II. Terminology and letter symbols

1 Types of field-effect transistors

1.1 N-channel field-effect transistor

A field-effect transistor which has an N-type conduction channel.

1.2 P-channel field-effect transistor

A field-effect transistor which has a P-type conduction channel.

1.3 Junction-gate field-effect transistor

A field-effect transistor having one or more gate regions which form PN junction(s) with the channel.

1.4 Insulated-gate field-effect transistor

A field-effect transistor having one or more gate electrodes which are electrically insulated from the channel.

1.5 Metal-oxide-semiconductor field-effect transistor

An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material.

1.6 Depletion type field-effect transistor

A field-effect transistor having appreciable channel conductivity for zero gate-source voltage; the channel conductivity may be increased or decreased according to the polarity of the applied gate-source voltage.

1.7 Enhancement type field-effect transistor

A field-effect transistor having substantially zero channel conductivity for zero gate-source voltage; the channel conductivity may be increased by the application of a gate-source voltage of appropriate polarity.

1.8 Triode field-effect transistor

A field-effect transistor having a gate region, a source region and a drain region.

NOTE Where no confusion is likely to occur, the term may be abbreviated to “field-effect triode”.

1.9 Tetrode field-effect transistor

A field-effect transistor having two independent gate regions, a source region and a drain region.

NOTE Where no confusion is likely to occur, the term may be abbreviated to “field-effect tetrode”.

2 General terms

2.1 Source region of a field-effect transistor

A region from which majority carriers flow into the channel.

2.2 Drain region of a field-effect transistor

A region into which majority carriers flow from the channel.

2.3 Gate region of a field-effect transistor

A region associated with the gate electrode, in which the electric field due to the control voltage is effective.

2.4 Depletion mode operation

The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value decreases the magnitude of the drain current.

2.5 Enhancement mode operation

The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value increases the magnitude of the drain current.

2.6 Channel

A thin semiconductor layer between the source region and the drain region, in which the current flow is controlled by the gate potential.

2.7 Substrate

2.7.1 *Substrate (of a junction-gate field-effect transistor)/substrate (of an insulated-gate field-effect transistor)*

A semiconductor material which contains a channel, a source and a drain and which may have a non-rectifying contact.

2.7.2 *Substrate (of a thin-film field-effect transistor)*

An insulator which supports the source and drain electrodes, the insulated gate layer and the thin semiconductor layer.

3 Terms related to ratings and characteristics

NOTE When several distinctive forms of a letter symbol exist, the most commonly used form is given.

3.1 “Reverse” and “forward” directions

Here, “reverse” means: the direction in which the channel carriers are decreased (depleted), and “forward” means: the direction in which the channel carriers are increased (enhanced).

3.2 Threshold voltage (of an enhancement type field-effect transistor) ($V_{GS(TO)}$)

The gate-source voltage at which the magnitude of the drain current reaches a specified low value.

3.3 Cut-off voltage (of a depletion type field-effect transistor) ($V_{GS(off)}$)

The gate-source voltage at which the magnitude of the drain current reaches a specified low value.

3.4 Gate cut-off current (of a junction-gate field-effect transistor)

The current flowing in the gate terminal of a junction field-effect transistor when the gate junction is biased in the reverse direction.

3.5 Gate leakage current (of an insulated-gate field-effect transistor)

The leakage current flowing in the gate terminal of an insulated-gate field-effect transistor.

3.6 Input capacitance

The capacitance between gate and source terminals with the drain short-circuited to the source for a.c. signals, under specified bias and frequency conditions.

3.7 Gate-source resistance (r_{GS})

The d.c. resistance between gate and source terminals at specified gate-source and drain-source voltages.

4 Letter symbols

4.1 General

Clauses 2, 3 and 4 of Publication 747-1, Chapter V, apply.

4.2 Additional general subscripts

In addition to the list of recommended general subscripts given in Publication 747-1, Chapter V, Sub-clause 2.1.2, the following special subscripts are recommended for the field of field-effect transistors:

D, d	= drain
G, g	= gate
S, s	= source
B, b; U, u	= substrate
T; th; (TO)	= threshold

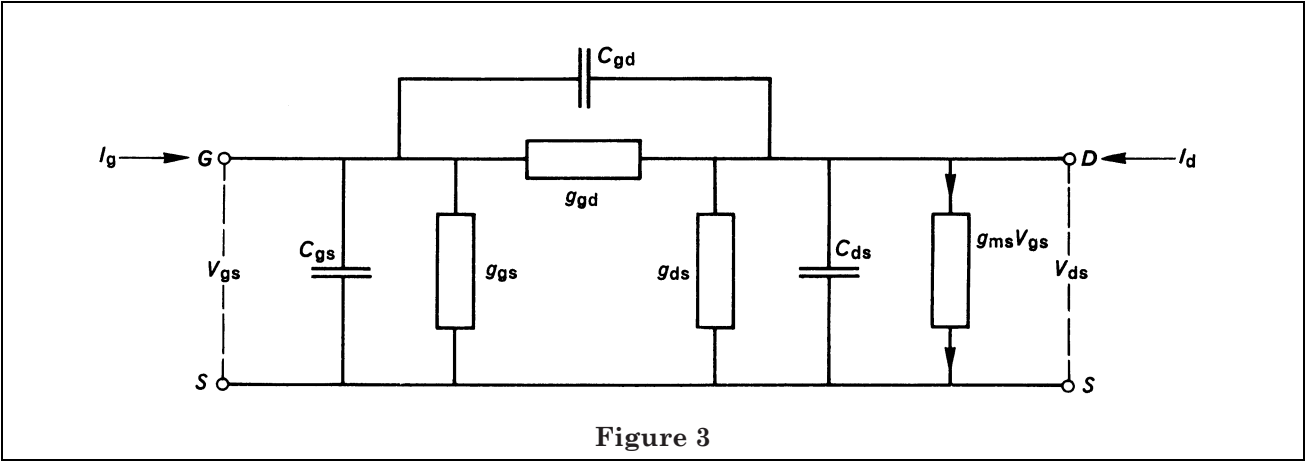
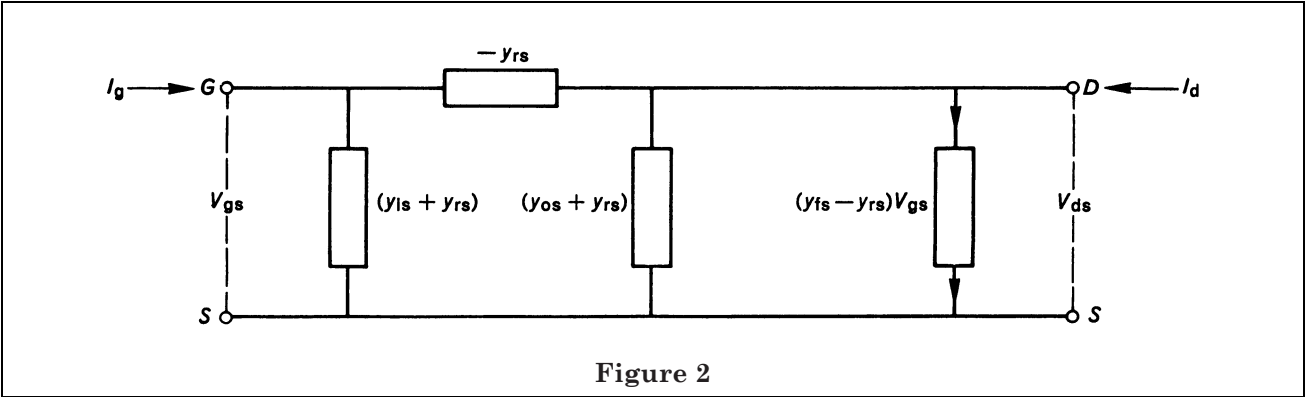
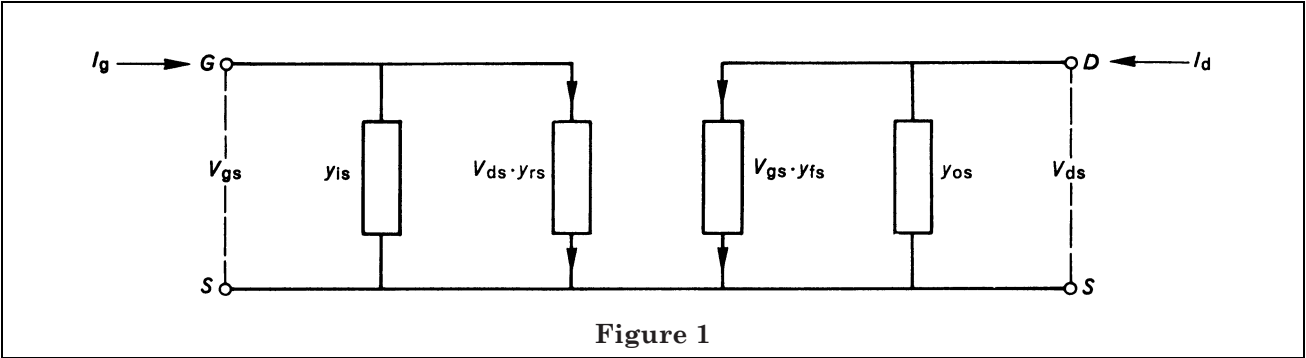
4.3 List of letter symbols

Name and designation	Letter symbol	Remarks
4.3.1 Voltages		
Drain-source (d.c.) voltage	V_{DS}	
Gate-source (d.c.) voltage	V_{GS}	
Gate-source cut-off voltage (of a junction field-effect transistor and of a depletion type insulated-gate field-effect transistor)	$V_{GS(OFF)}$; $V_{GS(off)}$	
Gate-source threshold voltage (of an enhancement type insulated-gate field-effect transistor)	V_{GST} ; $V_{GS(th)}$; $V_{GS(TO)}$	
Forward gate-source (d.c.) voltage	V_{GSF}	
Reverse gate-source (d.c.) voltage	V_{GSR}	
Gate-drain (d.c.) voltage	V_{GD}	
Source-substrate (d.c.) voltage	V_{SB} ; V_{SU}	
Drain-substrate (d.c.) voltage	V_{DB} ; V_{DU}	
Gate-substrate (d.c.) voltage	V_{GB} ; V_{GU}	
Gate-gate voltage (for multi-gate devices)	V_{G1-G2}	
Gate-source breakdown voltage with drain short-circuited to source	$V_{(BR)GSS}$	
4.3.2 Currents		
Drain (d.c.) current	I_D	
Drain current, at a specified gate-source condition	I_{DSX}	
Drain current, at a specified (external) gate-source resistance	I_{DSR}	
Drain current, with gate short-circuited to source ($V_{GS} = 0$)	I_{DSS}	
Source (d.c.) current	I_s	
Source current, at a specified gate-drain condition	I_{sdx}	
Source current, with gate short-circuited to drain ($V_{GD} = 0$)	I_{SDS}	
Gate (d.c.) current	I_G	
Forward gate current	I_{GF}	
Gate cut-off current (of a junction field-effect transistor), with source open-circuited	I_{GDO}	
Gate cut-off current (of a junction field-effect transistor), with drain open-circuited	I_{GSO}	

Name and designation	Letter symbol	Remarks
Gate cut-off current (of a junction field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate leakage current (of an insulated-gate field-effect transistor), with drain short-circuited to source	I_{GSS}	
Gate cut-off current (of a junction field-effect transistor), with specified drain-source circuit conditions	I_{GSX}	
Substrate current	$I_{\text{B}}; I_{\text{U}}$	
4.3.3 Power dissipation		
Drain-source (d.c.) power dissipation	P_{DS}	
4.3.4 Resistances (or conductances) and capacitances		
Drain-source resistance	$r_{\text{DS}}; r_{\text{ds}}$	
Gate-source resistance	$r_{\text{GS}}; r_{\text{gs}}$	
Gate-drain resistance	$r_{\text{GD}}; r_{\text{gd}}$	
Gate resistance (with $V_{\text{DS}} = 0$ or $v_{\text{ds}} = 0$)	$r_{\text{GSS}}; r_{\text{gss}}$	
Drain-source on-state resistance	$r_{\text{DS(ON)}}; r_{\text{ds(on)}}; r_{\text{DSon}}$	
Drain-source off-state resistance	$r_{\text{DS(OFF)}}; r_{\text{ds(off)}}; r_{\text{DSoff}}$	
Open-circuit gate-source capacitance (drain-source and gate-drain open-circuited to a.c.)	C_{gso}	
Open-circuit gate-drain capacitance (drain-source and gate-source open-circuited to a.c.)	C_{gdo}	
Open-circuit drain-source capacitance (gate-drain and gate-source open-circuited to a.c.)	C_{dso}	
Short-circuit input capacitance in common-source configuration; gate-source capacitance (drain-source short-circuited to a.c.)	$C_{\text{iss}}; C_{\text{11ss}}$	
Short-circuit output capacitance in common-source configuration; drain-source capacitance (gate-source short-circuited to a.c.)	$C_{\text{oss}}; C_{\text{22ss}}$	
Short-circuit input conductance in common-source configuration	g_{iss}	
Short-circuit output conductance in common-source configuration	g_{oss}	
Common-source reverse transfer capacitance with input short-circuited to a.c.	$C_{\text{rss}}; C_{\text{12ss}}$	
Short-circuit output capacitance in common-drain configuration (gate-drain short-circuited to a.c.)	$C_{\text{ods}}; C_{\text{22ds}}$	

Name and designation	Letter symbol	Remarks
4.3.5 Small-signal y parameters in common-source configuration and π equivalent circuit parameters (see Figure 1, Figure 2 and Figure 3, page 7).		
Short-circuit input admittance	$y_{is} = \text{Re}_{(yis)} + j\omega C_{is}$ $y_{11s} = \text{Re}_{(y11s)} + j\omega C_{11s}$	
Short-circuit reverse transfer admittance	$y_{rs} = \text{Re}_{(yrs)} + j\omega C_{rs}$ $y_{12s} = \text{Re}_{(y12s)} + j\omega C_{12s}$	
Short-circuit forward transfer admittance	$y_{fs} = \text{Re}_{(yfs)} + j\text{Im}_{(yfs)}$ $y_{21s} = \text{Re}_{(y21s)} + j\text{Im}_{(y21s)}$	
Short-circuit output admittance	$y_{os} = \text{Re}_{(yos)} + j\omega C_{os}$ $y_{22s} = \text{Re}_{(y22s)} + j\omega C_{22s}$	
Modulus of the short-circuit reverse transfer admittance	$ y_{rs} ; y_{12s} $	
Phase of the short-circuit reverse transfer admittance	$\varphi_{yrs}; \varphi_{y12s}$	
Modulus of the short-circuit forward transfer admittance	$ y_{fs} ; y_{21s} $	
Phase of the short-circuit forward transfer admittance	$\varphi_{yfs}; \varphi_{y21s}$	
Gate-source conductance (in the π equivalent circuit)	g_{gs}	
Gate-drain conductance (in the π equivalent circuit)	g_{gd}	
Drain-source conductance (in the π equivalent circuit)	g_{ds}	
Forward transconductance (in the π equivalent circuit)	$g_{ms}; g_m$	
Gate-source capacitance (in the π equivalent circuit)	C_{gs}	
Gate-drain capacitance (in the π equivalent circuit)	C_{gd}	
Drain-source capacitance (in the π equivalent circuit)	C_{ds}	
4.3.6 Other parameters		
Power gain	$G_p; G_p$	
Cut-off frequency (in the common-source configuration)	f_{yfs}	
Noise voltage	V_n	
Noise figure	F	
Temperature coefficient of drain current	α_{ID}	
Temperature coefficient of drain-source resistance	α_{rds}	

Name and designation	Letter symbol	Remarks
Turn-on delay time	$t_{d(\text{on})}$	Switching times (see Figure 4, Page 8) $t_{\text{on}} = t_{d(\text{on})} + t_r$ $t_{\text{off}} = t_{d(\text{off})} + t_f$
Turn-off delay time	$t_{d(\text{off})}$	
Rise time	t_r	
Fall time	t_f	
Turn-on time	t_{on}	
Turn-off time	t_{off}	



Small-signal y parameters in common-source configuration and π equivalent circuit parameters

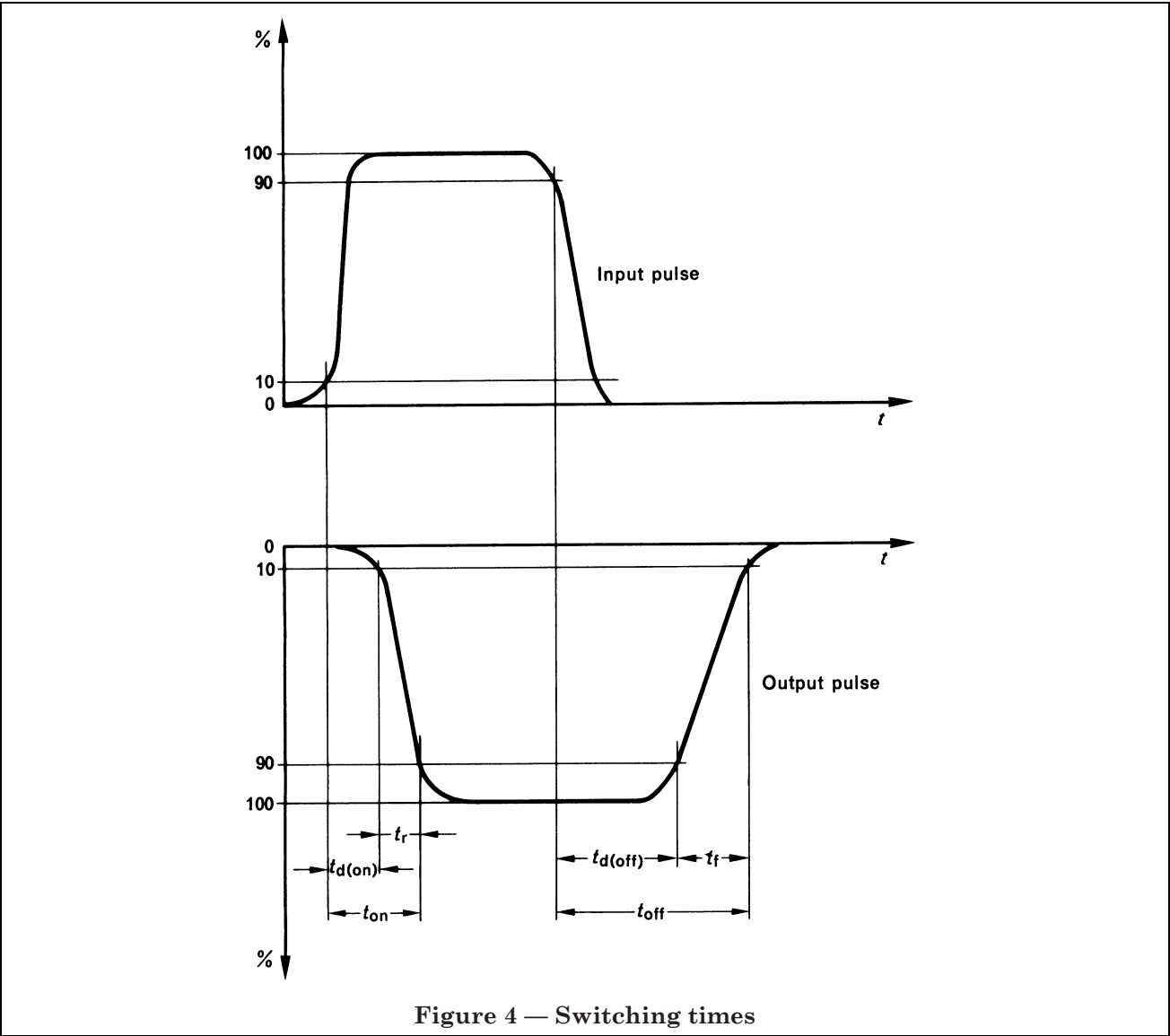


Figure 4 — Switching times

4.3.7 Matched-pair field-effect transistors

Name and designation	Letter symbol	Remarks
Difference of gate leakage currents (for insulated-gate field-effect transistors) and difference of gate cut-off currents (for junction field-effect transistors)	$I_{G1} - I_{G2}$	The smaller value is subtracted from the larger value
Ratio of drain currents for zero gate-source voltage	I_{DSS1}/I_{DSS2}	The smaller of the two values is taken as the numerator
Difference of small-signal common-source output conductances	$g_{os1} - g_{os2}$	The smaller value is subtracted from the larger value
Ratio of small-signal common-source forward transfer conductances	g_{fs1}/g_{fs2}	The smaller of the two values is taken as the numerator
Difference of gate-source voltages	$V_{GS1} - V_{GS2}$	The smaller value is subtracted from the larger value
Change in difference of gate-source voltages between two temperatures	$ \Delta(V_{GS1} - V_{GS2}) _{\Delta T}$	

Chapter III. Essential ratings and characteristics

1 General

1.1 Device categories

Field-effect transistors are divided into three categories:

- Type A Junction-gate type.
- Type B Insulated-gate depletion type.
- Type C Insulated-gate enhancement type.

1.2 Multiple-gate devices

For multiple-gate devices, the required gate ratings and characteristics shall be given for each gate separately, except where otherwise stated.

1.3 Handling precautions

Because of the very high input resistance of field-effect transistors, the gate insulation layer (for insulated-gate types) or the gate junction (for junction-gate types) may be irreversibly damaged if an excessive voltage is allowed to build up, e.g. due to contact with electrostatically charged persons, leakage currents from soldering irons, etc.

When handling these devices, the handling precautions given in Publication 747-1, Chapter IX, Clause 1, shall therefore be observed.

2 Ratings (limiting values)

2.1 Temperatures

2.1.1 Minimum and maximum storage temperatures (T_{stg})

2.1.2 Minimum and maximum operating temperature (ambient or case) (T_{amb} or T_{case})

2.2 Power dissipation (P_{tot})

2.2.1 Maximum total power dissipation ($P_{tot,max}$) over the specified range of operating temperatures (ambient or case). Any special requirements for ventilation and/or mounting shall be stated.

Either:

2.2.1.1 A curve showing $P_{tot,max}$ as a function of operating temperature (T_{amb} or T_{case}),

or (for power MOSFET only):

2.2.1.2 a) Maximum virtual channel temperature ($T_{vj,max}$), and

2.2.1.2 b) Absolute limiting value of total power dissipation ($P_{tot,abs}$).

NOTE When $T_{vj,max}$ and $P_{tot,abs}$ are specified R_{th} and, where appropriate, Z_{th} should also be specified (see the relevant subclauses in clause 3).

2.2.2 For power MOSFET only:

Maximum peak total power dissipation ($P_{totM,max}$).

A curve, showing $P_{totM,max}$ (where appropriate).

2.2.3 For power MOSFET only:

Safe operating area (SOAR), where appropriate, over the specified range of operating temperatures, under specified pulse conditions.

2.3 Voltages and currents

Ratings shall be given preferably by a curve over the range of operating temperatures, or at 25 °C and one other higher operating temperature, chosen from the list in Publication 747-1, Chapter VI, Clause 5.

2.3.1 Maximum drain-source voltage, under specified conditions

TYPES		
A	B	C
+	+	+
+	+	+
+	+	+
+	+	+
+	+	+
+	+	+
+	+	+
+	+	+
+	+	+

2.3.2 Maximum reverse gate-source voltage and, where appropriate, maximum forward gate-source voltage, under specified conditions

2.3.3 Maximum gate-drain voltage, under specified conditions

2.3.4 Maximum gate-gate voltage (for multiple-gate devices), under specified conditions

2.3.5 For insulated-gate field-effect transistors with separate source and substrate terminals (chopper or analog-switch types):

- maximum gate-substrate voltage, under specified conditions
- maximum drain-substrate voltage, under specified conditions
- maximum source-substrate voltage, under specified conditions

2.3.6 Drain current

2.3.6.1 Maximum drain current (I_D)

2.3.6.2 For power MOSFET only:

Maximum peak drain current (I_{DM}), under specified pulse conditions.

2.3.7 Maximum forward gate current

2.3.8 Forward current of the inverse diode (for power MOSFET) in the following applications:

- low-frequency amplifier
- switching transistor
- chopper
- low-level d.c. amplifier.

2.3.8.1 Maximum continuous (d.c.) source current ($I_{S(B)}$)

2.3.8.2 Maximum peak source current ($I_{SM(B)}$), under specified pulse conditions.

2.4 Mechanical data

The requirements for mechanical data, valid for other semi-conductor devices, apply to these devices.

3 Characteristics

Characteristics are to be given at 25 °C, except where otherwise stated; other temperatures should be taken from the list in Publication 747-1, Chapter VI, Clause 5.

3.1 Characteristics for low-frequency amplifier applications

3.1.1 Gate cut-off current

Gate leakage current

Maximum value, at specified gate-source or drain-gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

Together with:

Maximum value of the current of all gates connected together, at specified gate-source or drain-gate voltage, at an operating temperature of 25 °C and at one specified higher operating temperature.

TYPES		
A	B	C
+	+	+
+	+	+
+	+	+
	+	+
	+	+
	+	+
+	+	+
	+	+
+		
	+	+
	+	+
+	+	+
+		
	+	+

3.1.2 Drain cut-off current

Maximum value, at specified drain-source and gate-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and at one specified higher operating temperature.

3.1.3 Drain current at zero gate-source voltage (I_{DSS})

Minimum and maximum values, for zero gate-source voltage, at a specified drain-source voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

3.1.4 Drain current at specified gate-source voltage (I_D)

Minimum and maximum values, for specified gate-source and drain-source voltages, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

3.1.5 Gate-source cut-off voltage (V_{GSoff})

Minimum and maximum values of gate-source voltage at which the drain current has been reduced to a specified low value, other terminal connections being specified, over the range of operating temperatures.

3.1.6 Gate-source threshold voltage ($V_{GS(T0)}$)

Minimum and maximum values, at a specified high value of drain-source voltage, and at a value of drain current equal to or more than 10 times the maximum value of drain current at zero gate voltage, other terminal connections being specified, at an operating temperature of 25 °C and, where appropriate, at one specified higher operating temperature.

3.1.7 Short-circuit input capacitance (C_{iss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the output short-circuited to a.c.

3.1.8 Short-circuit output conductance and, where appropriate, capacitance (g_{oss} , C_{oss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

3.1.9 Short-circuit feedback capacitance (where appropriate) (C_{rss})

Maximum small-signal value, in common-source configuration, under specified bias conditions and at a specified low frequency, with the input short-circuited to a.c.

3.1.10 Forward transconductance (g_{fs})**3.1.10.1 (Not applicable to power MOSFET)**

Minimum and maximum values under specified bias conditions and at a specified low frequency.

3.1.10.2 For power MOSFET only

Minimum value, for specified drain-source voltage and drain current, at an operating temperature of 25 °C and, where appropriate, at a specified higher temperature.

TYPES		
A	B	C
+	+	+
+	+	
		+
+	+	
		+
+	+	+
+	+	+
+	+	+
	+	+