
British Standard

Semiconductor devices

Part 2. Integrated circuits

Section 2.2 Recommendations for digital integrated circuits

Dispositifs à semiconducteurs

Partie 2. Circuits intégrés

Section 2.2 Recommandations pour circuits intégrés digitaux

Halbleiter-Bauelemente

Teil 2. Integrierte Schaltungen

Abschnitt 2.2 Empfehlungen für integrierte digitale Schaltungen

National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with IEC Publication 748-2 'Semiconductor devices. Integrated circuits Part 2 : Digital integrated circuits' published in 1985 by the International Electrotechnical Commission (IEC).

This British Standard constitutes Section 2.2 of the British Standard for semiconductor devices (BS 6493). BS 6493 is identical with IEC Publications 747, 748 and 749 and will be issued in a series of separately published Sections corresponding to the individual Parts of the IEC publications.

Terminology and conventions. The text of the international standard has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards; attention is drawn especially to the following.

Wherever page numbers are quoted, they are IEC page numbers.

Cross-references

International standards	Corresponding British Standards
IEC 747-1 : 1983	BS 6493 Semiconductor devices: discrete devices and integrated circuits Section 1.1 : 1984 General (Identical)
IEC 748-1 : 1984	Section 2.1 : 1985 General (Identical)

Compliance with a British Standard does not of itself confer immunity from legal obligations.

Amendment No. 1
published and effective from 15 July 1992
to BS 6493 : Section 2.2 : 1986

Semiconductor devices
Part 2. Integrated circuits
Section 2.2 Recommendations for digital
integrated circuits

AMD 7003
Amendment No. 1
to IEC 748-2 : 1985

NOTE. This amendment implements Amendment No. 1 published in September 1991 to IEC Publication 748-2. Consequent amendments to the contents list and national foreword have also been made.

Revised text

AMD 7003
July 1992

National foreword

In line 3, after the title of IEC 748-2, insert ', as amended by Amendment No. 1 published in September 1991,'.

AMD 7003
July 1992

Contents

After the entry for clause 1.4 of chapter II, insert the following new entry.

'1.5 Latch-up concept'

After the entry for clause 3.5 of chapter II, insert the following new entry.

'3.6 Terms and descriptions for test patterns for memory testing'

After the entry for clause 7 of chapter II, insert the following new entry.

'8. Additional terms and definitions for digital integrated circuits'

After the entry for clause 5 of section three of chapter IV, insert the following new entry.

'6. Method of verification of the function of a digital integrated circuit'

At the end of the clause, after subclause 1.4, insert the following new subclause.

1.5 Latch-up concept

1.5.1 Latch-up state

A state in which a low-impedance path has resulted from and persists following the current resulting from an input, output or supply overvoltage that triggers a parasitic four-layer bipolar structure.

NOTE - In the latch-up state, the device becomes inoperable.

1.5.2 Latch-up effect

A process that results in a latch-up state.

1.5.3 Latch-up on-state voltage ($V_{CC(L)}$, $V_{DD(L)}$)

The voltage between the supply voltage terminals of an integrated circuit at a specified current when the integrated circuit is in the latch-up state.

1.5.4 Latch-up current (I_{latch})

The lowest current that flows into or out of a specified terminal of an integrated circuit at the onset of latch-up.

At the end of the clause, after figure 17, insert the following new subclause, including figures 75 to 88.

3.6 Terms and descriptions for test patterns for memory testing

3.6.1 Introduction

3.6.1.1 Working definitions for principal terms

3.6.1.1.1 *Data pattern*

An array of logic ZEROs (0's) and logic ONEs (1's) within a field of memory cells.

NOTE - A field is usually subdivided into "rows" and "columns".

3.6.1.1.2 *Address sequence*

A specified sequence of addresses.

3.6.1.1.3 *Test pattern*

A specified address sequence with the operations specified for each address so as to create a specified data pattern.

3.6.1.2 *General*

The enumeration given in subclauses 3.6.2 to 3.6.4.2 is not exhaustive and is limited to descriptions only.

No considerations are made regarding elapsed test times or failure modes and related test patterns. All test patterns described in subclause 3.6.4 are intended to perform tests on a specified data pattern. For each description, an assumption is made on the allocation of the memory addresses to the topological location of the memory cells. On this basis, the address sequence is chosen.

In practice, a different allocation may be chosen by the manufacturer, for example, in a 4 k RAM, cell number 4095 may be located in the upper left corner of the field of memory cells, adjacent to cell number 0. Then the address sequence corresponding to the specified data pattern shall be changed accordingly.

In all specifications, the address sequence corresponding to the specified data pattern shall be stated by the manufacturer. Examples given are based on a square field where the numbers of "rows" and "columns" are equal.

To the extent that much of the information given relates to data patterns within the memory, the logic symbols "0" and "1" have been used (instead of L and H).

NOTE - N means the number of memory cells. The addresses run from 0 to N-1.

3.6.2 *Data patterns*

In the figures representing data patterns, the number of memory cells is represented by the sequence 0 to N-1, where N is the total number of cells. The numbering used is row-by-row and from left to right.

NOTE - Representations may be in either logical or graphical form as shown in the a) or b) versions of the figures given.

3.6.2.1 All ONE (all ZERO)

A data pattern consisting of all 1's (all 0's) (see Figure 75 for all 1's).

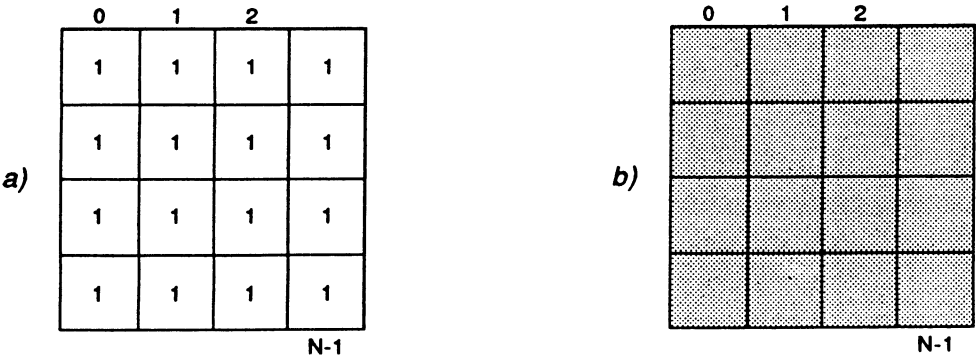


Figure 75

3.6.2.2 Single ONE (single ZERO)

A data pattern consisting of a single 1 (single 0) on a background of all 0's (all 1's) (see Figure 76 for a single 1).

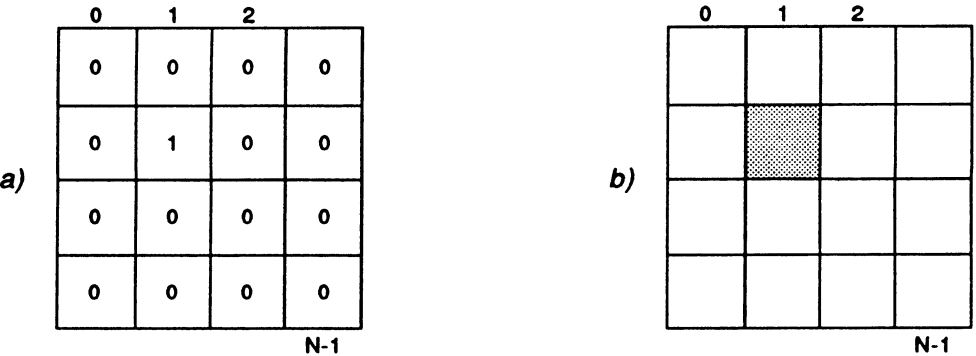


Figure 76

3.6.2.3 Column bars

A data pattern of alternating columns of 0's and 1's (see Figure 77).

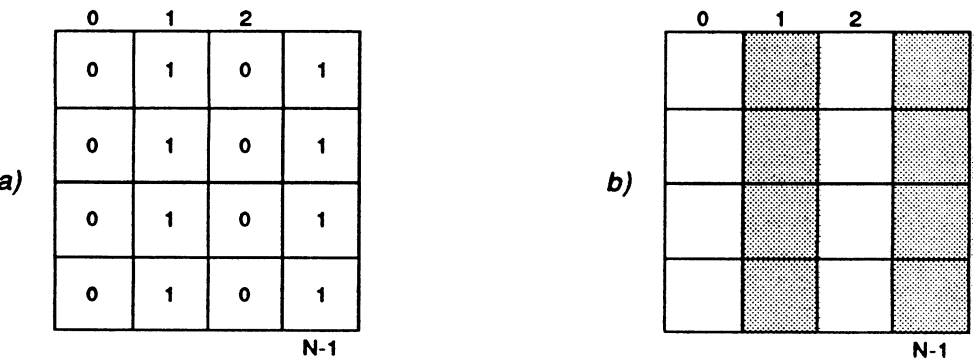


Figure 77

3.6.2.4 Row bars

A data pattern of alternating rows of 0's and 1's (see Figure 78).

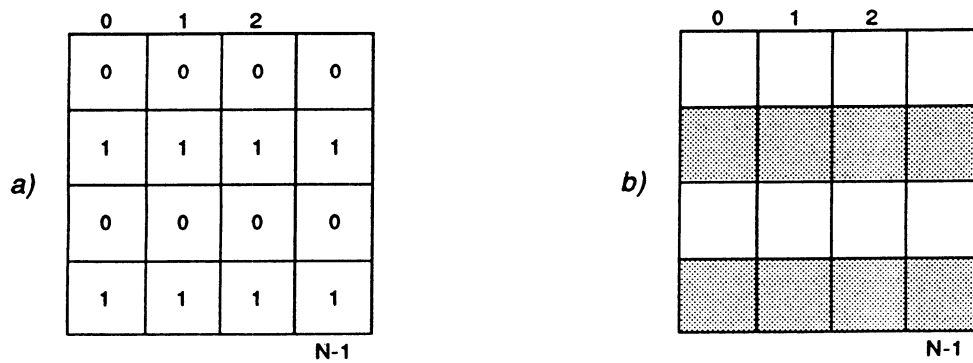


Figure 78

3.6.2.5 Diagonal

A data pattern of diagonal 1's or 0's on the background of complementary data.

NOTE - In a square array of memory cells, "diagonal" denotes a configuration in which all cells are located either on a main diagonal (see Figure 79) or on two parallel diagonals such that only one memory cell is located in each row and each column (see Figure 80).

Example 1:

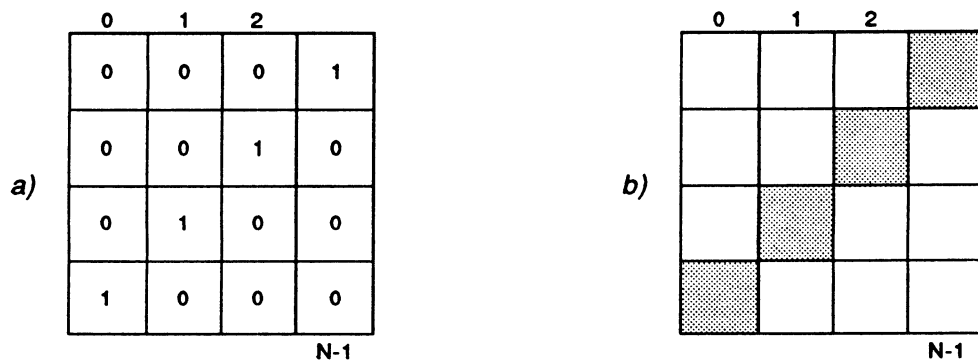


Figure 79

Example 2:

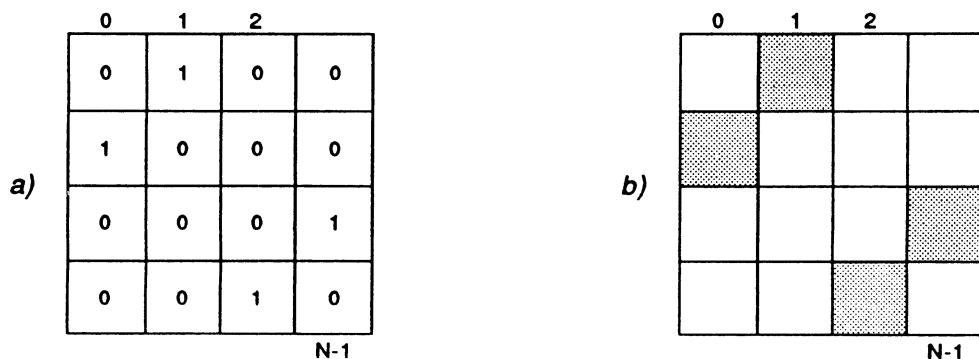


Figure 80

3.6.2.6 Checkerboard

A data pattern of alternating 0s and 1s in both directions (that is, columns and rows) (see Figure 81).

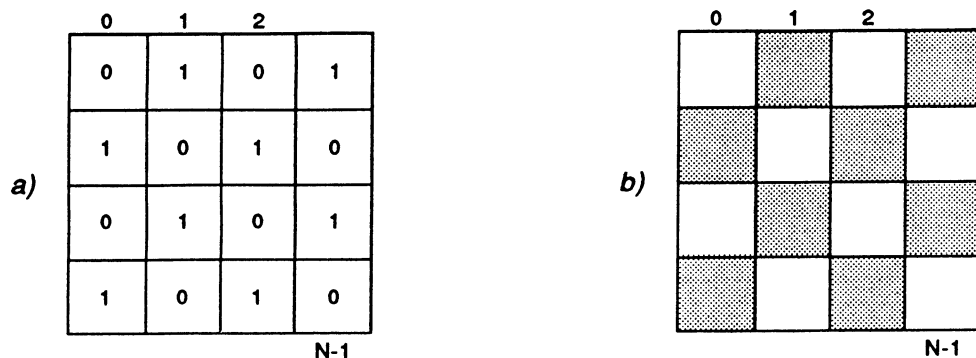


Figure 81

3.6.3 Address sequences

NOTE - By means of suitable address sequences, data patterns can be shifted, complemented or extended within memory fields.

3.6.3.1 Marching

An address sequence by means of which all cells are sequentially read and rewritten with complementary data.

NOTE - Background data and rewritten data are complementary to each other (see Figure 82).

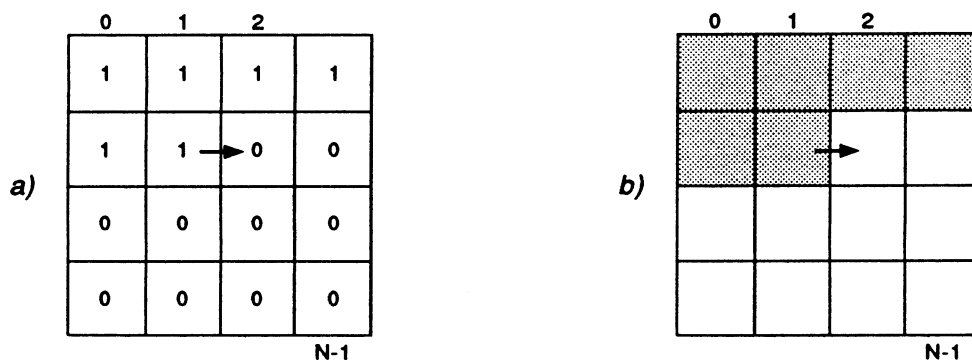


Figure 82

3.6.3.2 Walking

An address sequence by means of which a specified pattern in one or more consecutive cells is shifted through the whole memory, all cells except those written with the shifted pattern being read after each shifting (see Figure 83).

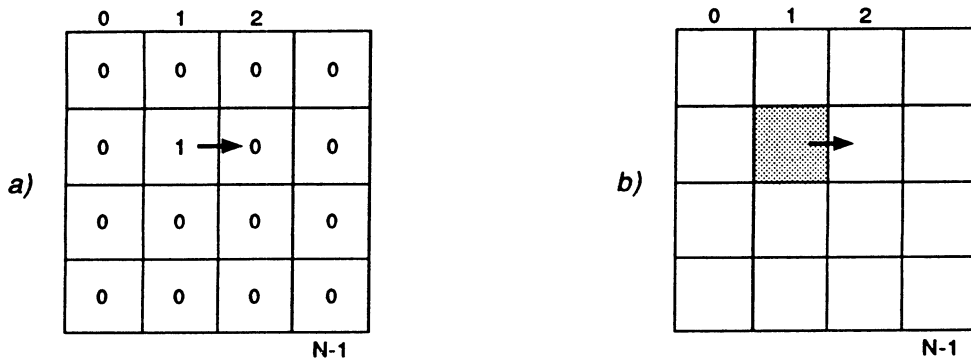


Figure 83

3.6.4 Test patterns (examples)

3.6.4.1 Marching ONE's (marching ZERO's: see Note 2 below)

A test pattern with the following generation scheme:

A. A background pattern of all 0's is written to the memory (see Figure 84).

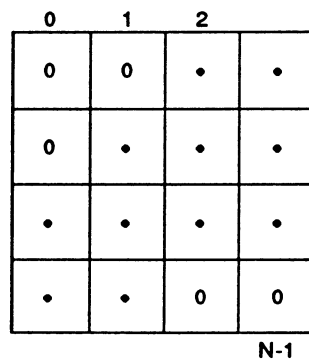


Figure 84

B. Each of the N memory cells is first read and then complemented, so that the memory finally contains the complement of the initial background pattern (see Figure 85).

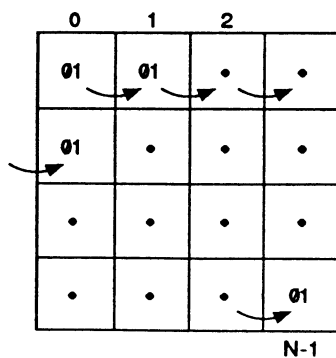


Figure 85

NOTES

- 1 "01" indicates a "0" changed to a "1".
- 2 Starting from a background pattern of all 1's, this test pattern is called "Marching ZERO's".

3.6.4.2 Walking (single) ONE's (Walking single ZERO's: see Note 2 below)

A test pattern with the following generation scheme:

- A. A background pattern of all 0's is written to the memory (see Figure 86).

0	1	2	
0	0	•	•
0	•	•	•
•	•	•	•
•	•	0	0
N-1			

Figure 86

- B. Into a test cell, the complement is written (see Figure 87).

0	1	2	
01	0	•	•
0	•	•	•
•	•	•	•
•	•	0	0
N-1			

Figure 87

- C. The remaining cells of the memory are read.
- D. The test cell is read.
- E. Its complement is written in, that is, rewrite a 0, so that the test cell is now in its initial background state (see Figure 88).

0	1	2	
10	0	•	•
0	•	•	•
•	•	•	•
•	•	0	0
N-1			

Figure 88

F. The sequence of steps B to E is sequentially repeated for each memory cell.

NOTES

1 "10" indicates a "1" changed to a "0".

2 Starting from a background pattern of all 1's, this test pattern is called "Walking single ZERO's".`

AMD 7003
July 1992

New clause 8 of chapter II. Additional terms and definitions for digital integrated circuits

At the end of chapter II, insert the following new clause.

8 Additional terms and definitions for digital Integrated circuits

8.1 *Logic array*

An integrated circuit consisting of an array of logic elements or circuits whose interconnections are either determined during manufacture or by the user to perform user-defined logic functions.

Gate array

An integrated circuit consisting of an array of logic gates.

NOTE - Integrated circuits of this type are also known by the names "Mask programmable Logic Array (MPLA)" and "Uncommitted Logic Array (ULA)".

8.2 *Programmable logic array*

An integrated circuit consisting of arrays of combinatorial and sequential logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions.

NOTE - Integrated circuits of this type are also known by the abbreviation "PLA".`

Figure 27. Output currents associated with output voltages
Delete the existing figure and substitute the following new figure.

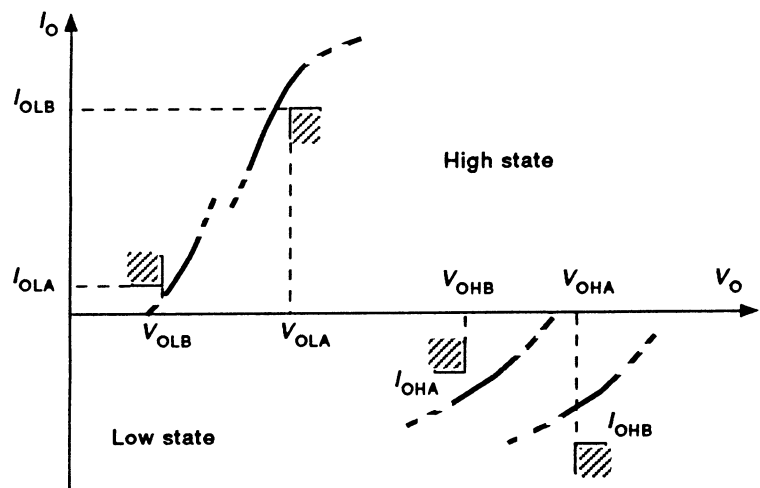


Figure 27 – Output currents associated with output voltages

Figure 28. Input currents associated with input voltages
Delete the existing figure and substitute the following new figure.

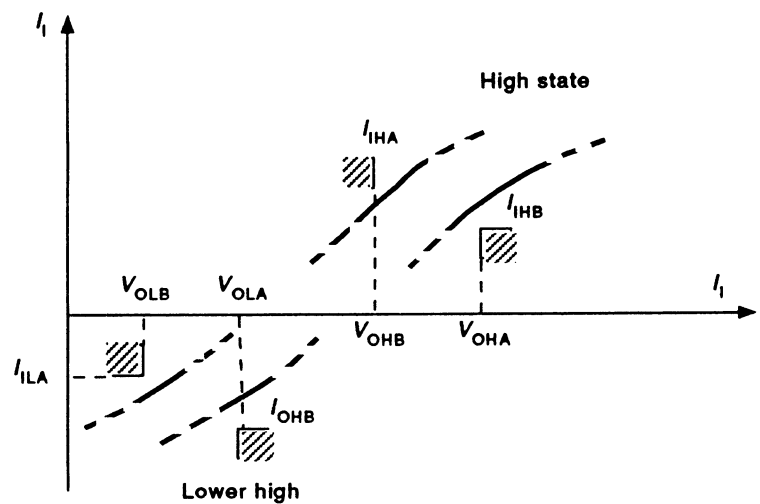


Figure 28 – Input currents associated with input voltages

NOTE - In Figures 27 and 28, the axes do not necessarily represent zero voltage or current.

Delete 'Under consideration.' and substitute the following.

5.3.2.1 Output off-state current (I_{OZ})

Maximum absolute value of the output off-state current when any voltage within the specified range is applied to the output, for specified values:

- supply voltage;
- range of applied voltages at the output terminal;
- input voltages at other terminals.

At the end of section three, insert the following new clause, including figure 89.

6 Method of verification of the function of a digital Integrated circuit

a) Purpose

To verify the function of the digital integrated circuit.

b) Circuit diagram

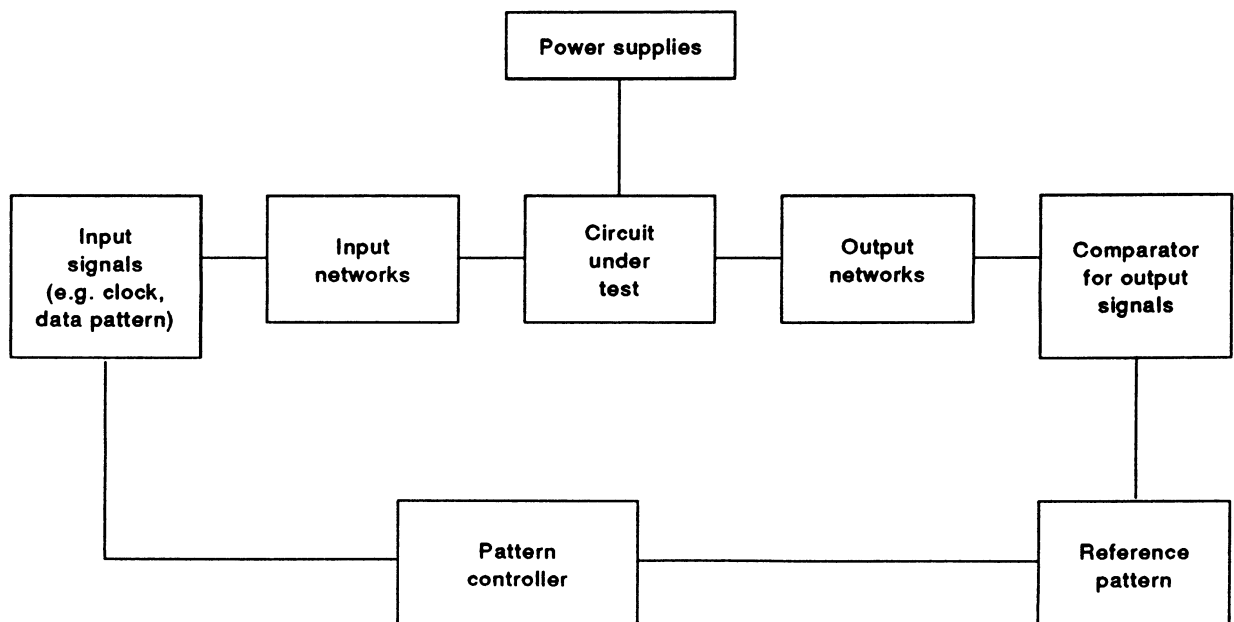


Figure 89

c) *Circuit description and requirements*

The measuring equipment shall be capable of supplying the necessary power supply voltages and, if more than one power supply is used, it should also be capable of providing the proper sequence of their application and removal and, where appropriate, controlling their rates of rise and fall. The measuring equipment shall keep the integrated circuit under test at the specified temperature. It shall be capable of providing the specified input patterns, i.e. specified sequences and combinations of input signal voltages and currents that meet the specified input timing conditions, and also the resulting output patterns. It shall also be capable of comparing the actual output signals with an output pattern.

The input pattern generator shall be capable of exercising the functional operations that are to be verified for the integrated circuit under test. For each operation that is tested, the input pattern generator shall provide any sequences and combinations of input signals necessary to bring the integrated circuit into a desired state (an initialization sequence) before the application of the pattern that exercises that operation. The reference pattern generator shall provide the output pattern that should result from the operation. The essential timing conditions and relationships between input and output signals shall apply to the output pattern.

d) *Precautions to be observed*

Special precautions: if appropriate (for instance latch-up for C-MOS devices).

e) *Verification procedure*

The temperature of the integrated circuit under test is set to the specified value and checked before and after the test.

The input, output and power supply terminals are connected as specified.

The power supply voltages are set to their specified values in the specified sequence of application.

The input signals corresponding to an input pattern, including any necessary initialization sequence, at the appropriate voltage and current levels and essential timing conditions, are applied to the inputs.

Each valid output signal is compared with the output pattern to verify that it lies within the specified voltage or current ranges and meets any essential timing relationships.

f) *Specified conditions*

- Ambient or case temperature (T_{amb} or T_{case}).
- Supply voltages:
 - values;
 - sequences, where appropriate;
 - rates of rise and fall, where appropriate.

- Input terminal connections.
 - Output terminal connections.
 - Input signal voltage levels and, where appropriate, current levels.
 - Output voltage ranges and, where appropriate, current ranges.
 - Essential input timing conditions:
 - rise and fall times, where appropriate;
 - set-up and hold times;
 - clock frequency, etc.
 - Essential output timing conditions:
 - transitions times;
 - relations between input and output signals, etc.
 - Functional operations to be verified:
 - input pre-setting initialization;
 - input patterns to exercise operations;
 - output patterns.
 - Input and output networks.
 - Circuit diagram.
 - Loading conditions, where appropriate.
 - Additional networks, where appropriate.
 - Conditions at the other terminals. ’
-

Amendment No. 2
published and effective from 15 April 1994
to BS 6493 : Section 2.2 : 1986

Semiconductor devices
Part 2. Integrated circuits
Section 2.2 Recommendations for digital integrated circuits

NOTE. This amendment implements Amendment No. 2 to IEC 748-2, published in December 1993 which incorporates Amendment No. 1 published in September 1991. The text of Amendment No. 2 is indicated by a vertical line in the margin.

Revised text

National foreword (as amended by Amendment No. 1)

In line 3, after title of IEC 748-2 delete 'as amended by Amendment No. 1 published in September 1991' and substitute 'as amended by Amendment No. 2 published in December 1993 incorporating Amendment No. 1 published in September 1991'.

AMD 8183/April 1994

Text of BS 6493 : Section 2.2

Amend the text of the British Standard in accordance with details given in the attached pages. All reference to page numbers in the amendment refer to the original page numbering found in the bottom corner of each page of the British Standard.

AMD 8183/April 1994

Page 3

CONTENTS

CHAPTER II: TERMINOLOGY AND LETTER SYMBOLS

Add the titles of the following new subclauses and clause:

1.5	Latch-up concept	35
3.6	Terms and descriptions for test patterns for memory testing	73
8	Additional terms and definitions for digital integrated circuits	113

CHAPTER III – ESSENTIAL RATINGS AND CHARACTERISTICS

Section One – Digital integrated circuits, general

Add the titles of the following new subclauses and:

5	Static electrical characteristics for bipolar integrated circuits, figures 27 and 28	125
5.3.2.1	Output off-state current I_{OZ}	127

5.5	Latch-up characteristics
6.3	Latch-up characteristics

Page 5

Section Two – Integrated circuit memories

Add a new subdivision C with the following titles:

C – Content addressable memories (CAM)

1	Circuit identification and description
2	Functional specifications
2.1	Block diagram
2.2	Functional description
2.3	Instruction set
2.4	Operation mode
3	Ratings (limiting values)
4	Recommended operating conditions (within the specified operating temperature range)
5	Static electrical characteristics for bipolar memories
6	Static electrical characteristics for MOS memories
7	Dynamic electrical characteristics
7.1	Times characterizing the response of the circuit
7.2	Requirements at the inputs to ensure correct sequential operation
7.3	Input and output capacitances
8	Power or current drawn from each supply (static operation)
9	Power or current drawn from each supply (dynamic operation)
10	Mechanical ratings, characteristics and other data

11	Supplementary information
11.1	Output loading capability
11.2	Noise margins
11.3	Interconnections of similar units
11.4	Type of output circuit
11.5	Interconnections to other types of circuits
12	Handling precautions

Page 7

CHAPTER IV – MEASURING METHODS

Section Two – Measuring methods of static characteristics

Add, on page 9, the titles of the following new clauses:

- 6 Input clamping voltage (V_{IK})
- 7 Off-state output current (I_{OZ})
- 8 Latch-up characteristics

Section Three – Dynamic measurements

Add, on page 9, the title of the following new clause:

- 6 Method of verification of the function of a digital integrated circuit 275

Page 19

CHAPTER II: TERMINOLOGY AND LETTER SYMBOLS

1 Terminology for combinatorial and sequential Integrated circuits

Add, after subclause 1.4.16, page 35, the following new subclauses:

- 1.5 Latch-up concept
- 1.5.1 Latch-up state

A state in which a low-impedance path has resulted from and persists following the current resulting from an input, output or supply overvoltage that triggers a parasitic four-layer bi-polar structure.

NOTE - In the latch-up state, the device becomes inoperable.

1.5.2 *Latch-up effect*

A process that results in a latch-up state.

1.5.3 *Latch-up on-state voltage ($V_{CC(L)}$, $V_{DD(L)}$)*

The voltage between the supply voltage terminals of an integrated circuit at a specified current when the integrated circuit is in the latch-up state.

1.5.4 *Latch-up current (I_{latch})*

The lowest current that flows into or out of a specified terminal of an integrated circuit at the onset of latch-up.

Page 77

Add, after figure 17, the following new subclauses:

3.6 *Terms and descriptions for test patterns for memory testing*

3.6.1 *Introduction*

3.6.1.1 *Working definitions for principal terms*

3.6.1.1.1 *Data pattern*

An array of logic ZEROS (0's) and logic ONES (1's) within a field of memory cells.

NOTE - A field is usually subdivided into "rows" and "columns".

3.6.1.1.2 *Address sequence*

A specified sequence of addresses.

3.6.1.1.3 *Test pattern*

A specified address sequence with the operations specified for each address so as to create a specified data pattern.

3.6.1.2 *General*

The enumeration given in subclauses 3.6.2 to 3.6.4.2 is not exhaustive and is limited to descriptions only.

No considerations are made regarding elapsed test times or failure modes and related test patterns. All test patterns described in subclause 3.6.4 are intended to perform tests on a specified data pattern. For each description, an assumption is made on the allocation of the memory addresses to the topological location of the memory cells. On this basis, the address sequence is chosen.

In practice, a different allocation may be chosen by the manufacturer, for example, in a 4 k RAM, cell number 4095 may be located in the upper left corner of the field of memory cells, adjacent to cell number 0. Then the address sequence corresponding to the specified data pattern shall be changed accordingly.

In all specifications, the address sequence corresponding to the specified data pattern shall be stated by the manufacturer. Examples given are based on a square field where the numbers of "rows" and "columns" are equal.

To the extent that much of the information given relates to data patterns within the memory, the logic symbols "0" and "1" have been used (instead of L and H).

NOTE - N means the number of memory cells. The addresses run from 0 to N-1.

3.6.2 Data patterns

In the figures representing data patterns, the number of memory cells is represented by the sequence 0 to N-1, where N is the total number of cells. The numbering used is row-by-row and from left to right.

NOTE - Representations may be in either logical or graphical form as shown in the a) or b) versions of the figures given.

3.6.2.1 All ONE (all ZERO)

A data pattern consisting of all 1's (all 0's) (see Figure 75 for all 1's).

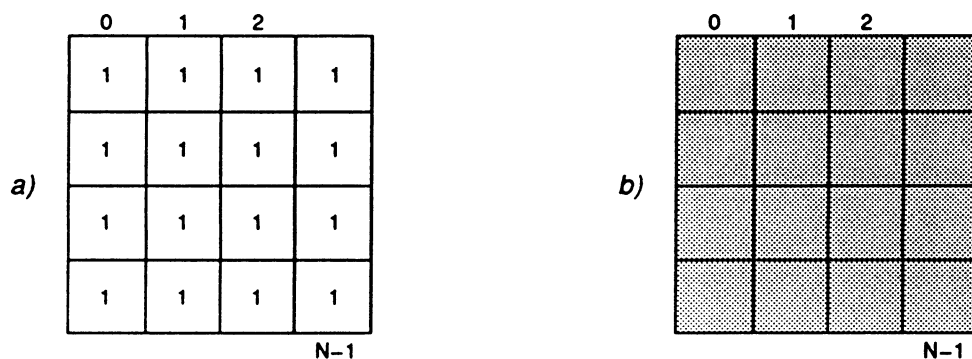


Figure 75

3.6.2.2 *Single ONE (single ZERO)*

A data pattern consisting of a single 1 (single 0) on a background of all 0's (all 1's) (see Figure 76 for a single 1).

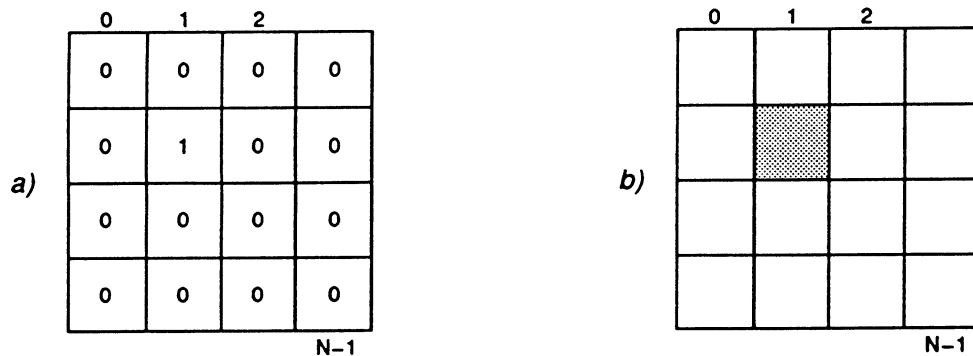


Figure 76

3.6.2.3 *Column bars*

A data pattern of alternating columns of 0's and 1's (see Figure 77).

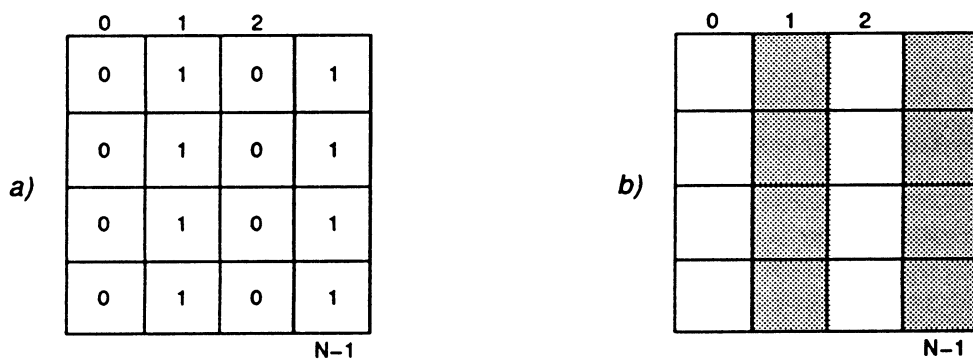


Figure 77

3.6.2.4 *Row bars*

A data pattern of alternating rows of 0's and 1's (see Figure 78).

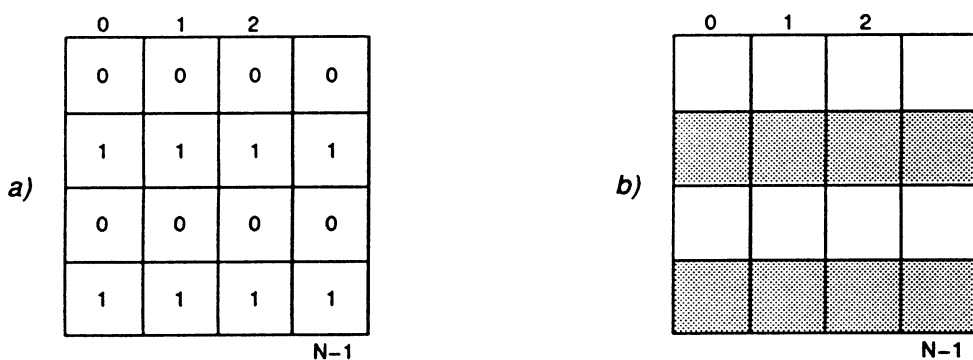


Figure 78

3.6.2.5 *Diagonal*

A data pattern of diagonal 1's or 0's on the background of complementary data.

NOTE - In a square array of memory cells, "diagonal" denotes a configuration in which all cells are located either on a main diagonal (see Figure 79) or on two parallel diagonals such that only one memory cell is located in each row and each column (see Figure 80).

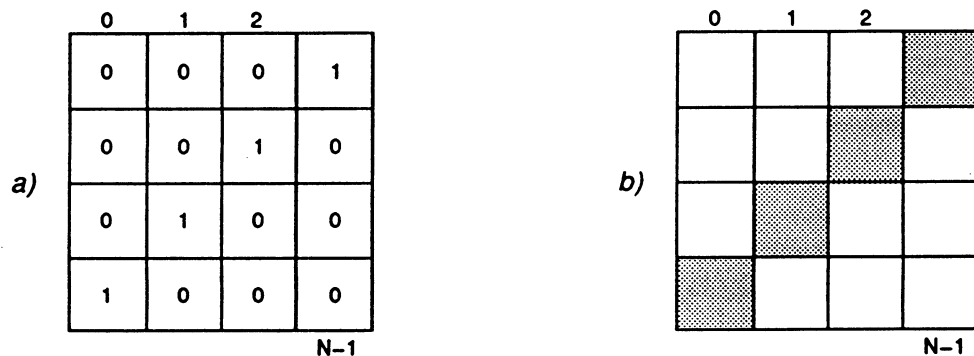
Example 1:

Figure 79

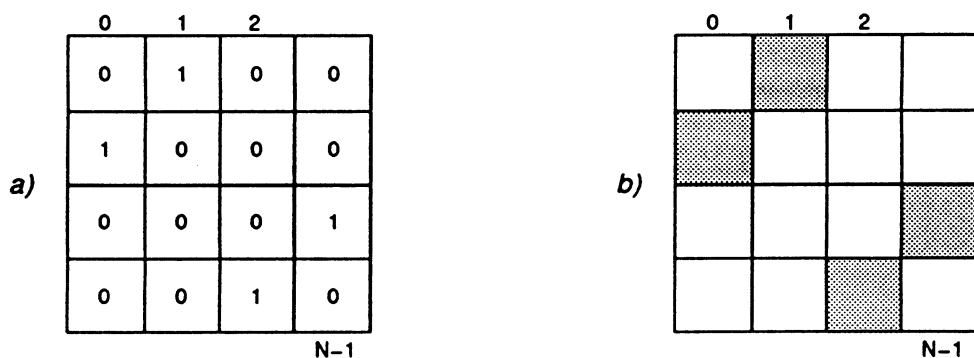
Example 2:

Figure 80

3.6.2.6 Checkerboard

A data pattern of alternating 0s and 1s in both directions (that is, columns and rows) (see Figure 81).

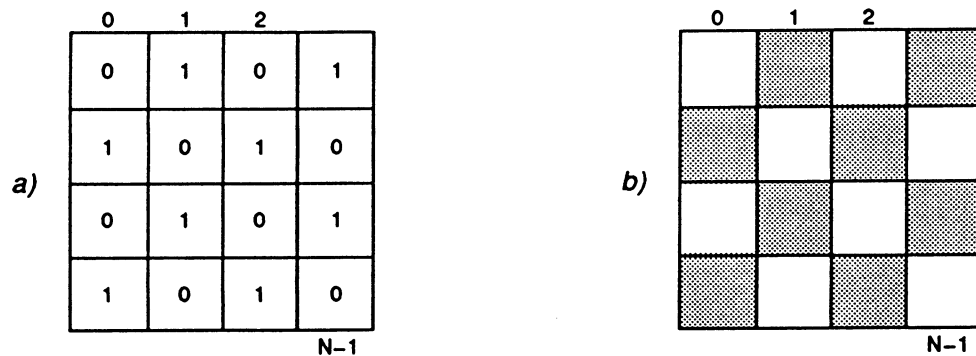


Figure 81

3.6.3 Address sequences

NOTE - By means of suitable address sequences, data patterns can be shifted, complemented or extended within memory fields.

3.6.3.1 Marching

An address sequence by means of which all cells are sequentially read and rewritten with complementary data.

NOTE - Background data and rewritten data are complementary to each other (see Figure 82).

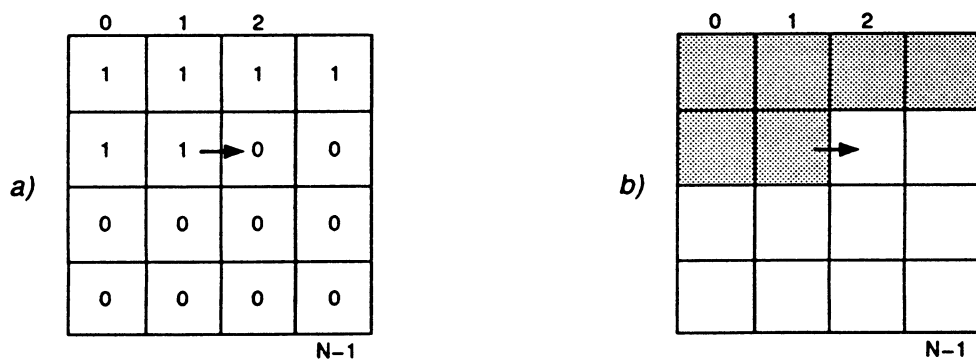


Figure 82

3.6.3.2 *Walking*

An address sequence by means of which a specified pattern in one or more consecutive cells is shifted through the whole memory, all cells except those written with the shifted pattern being read after each shifting (see Figure 83).

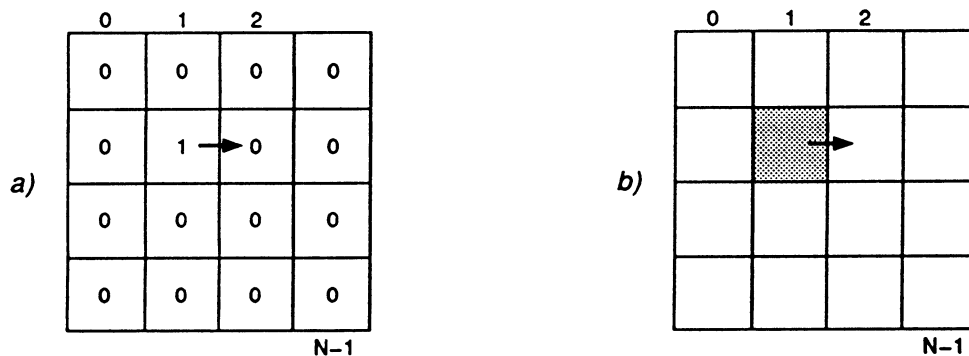


Figure 83

3.6.4 *Test patterns (examples)*3.6.4.1 *Marching ONE's* (marching ZERO's: see Note 2 below)

A test pattern with the following generation scheme:

A. A background pattern of all 0's is written to the memory (see Figure 84).

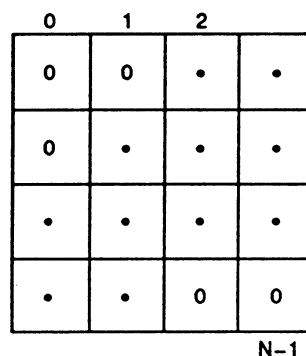


Figure 84

B. Each of the N memory cells is first read and then complemented, so that the memory finally contains the complement of the initial background pattern (see Figure 85).

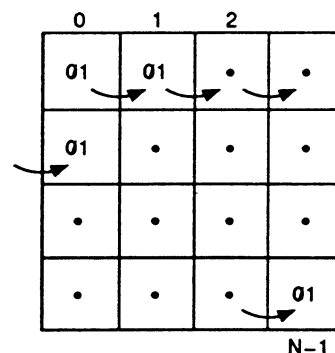


Figure 85

NOTES

- 1 "01" indicates a "0" changed to a "1".
- 2 Starting from a background pattern of all 1's, this test pattern is called "Marching ZERO's".

3.6.4.2 *Walking (single) ONE's (Walking single ZERO's: see Note 2 below)*

A test pattern with the following generation scheme:

- A. A background pattern of all 0's is written to the memory (see Figure 86).

0	1	2	
0	0	•	•
0	•	•	•
•	•	•	•
•	•	0	0
N-1			

Figure 86

- B. Into a test cell, the complement is written (see Figure 87).

0	1	2	
01	0	•	•
0	•	•	•
•	•	•	•
•	•	0	0
N-1			

Figure 87

- C. The remaining cells of the memory are read.
 D. The test cell is read.
 E. Its complement is written in, that is, rewrite a 0, so that the test cell is now in its initial background state (see Figure 88).

0	1	2	
10	0	•	•
0	•	•	•
•	•	•	•
•	•	0	0
N-1			

Figure 88

