

Specification for

Semiconductor devices of assessed quality: Generic data and methods of test

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- British Broadcasting Corporation
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- Electronic Engineering Association
- Engineering Equipment Users' Association
- Ministry of Defence
- National Supervising Inspectorate
- Post Office
- Telecommunications Engineering and Manufacturers' Association

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Foreword

It was reviewed by the Electronic Components Standards Committee, which succeeded the Telecommunication Industry Standards Committee, and confirmed in March 1980.

This British Standard, which has been reviewed and confirmed under the direction of the Electronic Components Technical Committee, is the generic specification for semiconductor devices in the system of standards for electronic parts of assessed quality. This standard excludes integrated circuits. It calls for the use of substances and/or test procedures that may be injurious to health if adequate precautions are not taken. It refers only to technical suitability and in no way absolves either the supplier or the user from statutory obligations relating to health and safety at any stage of manufacture or use.

A British Standard does not purport to include all the necessary provisions of a contract. Users of British Standards are responsible for their correct application.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

Summary of pages

This document comprises a front cover, an inside front cover, pages i to viii, pages 1 to 417 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Section 1. Principles and mandatory requirements

1.1 General matters

1.1.1 Scope

This standard forms part of the system of Common Standard Specifications for Electronic Parts of Assessed Quality and should be read in conjunction with the standards in the series BS 9000-1:1981, BS 6001, etc. It applies to semiconductor devices as defined in **1.1.3.3–1.1.3.12** and gives the terms, definitions, symbols, test methods, outlines, dimensions and other material necessary to implement fully the detail specifications for these parts.

This standard also includes, in Section 2, the general rules for the preparation of detail specifications. Associated with Section 2 of this standard are additional special rules for the preparation of detail specifications and these are given in document BS 9301 *et seq.*, for the various functional or application classes of semiconductor devices.

In accordance with **6.5** of BS 9000, where any omissions, conflicts, ambiguities or inconsistencies occur, documents shall rank in the following order of authority:

- 1) The detail specification
- 2) This generic specification
- 3) BS 9000, BS 6001, etc., and other standards to which reference is made.

1.1.2 Related documents

The following standards are referred to in the text of this document:

BS 2011, *Basic environmental testing procedures*. (See also IEC publication 68.)

BS 3363, *Schedule of letter symbols for semiconductor devices*. (See also IEC publication 148.)

BS 3934, *Dimensions of semiconductor devices*. (See also IEC publication 191-2.)

BS 3939, *Graphical symbols for electrical power, telecommunications and electronics diagrams*. (See also IEC publication 117.)

BS 4000, *Sizes of papers and boards*.

BS 4727, *Glossary of electrotechnical, power, telecommunications, electronics, lighting and colour terms*.

IEC 134, *Rating systems for electronic tubes and valves and analagous semiconductor devices*.

1.1.3 Terminology

For the purposes of this British Standard, the following terms and definitions apply. Additional terms may be found in BS 4727.

1.1.3.1 General terms

1.1.3.1.1

semiconductor device

a device including its encapsulation and terminals and whose essential characteristics are governed by the flow of charge carriers within a semiconductor material

1.1.3.1.2

extrinsic semiconductor material

a semiconductor material with charge carrier concentration dependent upon impurities or other imperfections

1.1.3.1.3

n-type semiconductor material

an extrinsic semiconductor material in which the conduction-electron density greatly exceeds the mobile hole density

1.1.3.1.4

p-type semiconductor material

an extrinsic semiconductor material in which the mobile hole density greatly exceeds the conduction-electron density

1.1.3.1.5

I-type (intrinsic) semiconductor material

a semiconductor material in which the electron and hole densities are effectively equal under conditions of thermal equilibrium

1.1.3.1.6

junction

a region of transition between semiconducting regions of different electrical properties

1.1.3.1.7

p-n junction

a junction between p and n type regions in a semiconductor material

1.1.3.1.8

alloyed junction

a junction formed by alloying one or more materials to a semiconductor crystal

1.1.3.1.9

diffused junction

a junction formed by the diffusion of an impurity within a semiconductor crystal

1.1.3.1.10

grown junction

a junction produced during the growth of a semiconductor crystal from a melt

1.1.3.1.11

electrode (of a semiconductor device)

that part providing the electrical contact between the specified region of a semiconductor device and the lead to its terminal

1.1.3.1.12

terminal (of a semiconductor device)

a specified externally available point of connection

1.1.3.1.13

anode terminal (of a semiconductor rectifier diode or thyristor)

the terminal to which forward current flows from the external circuit

1.1.3.1.14

cathode terminal (of a semiconductor rectifier diode or thyristor)

the terminal from which forward current flows to the external circuit

1.1.3.1.15

rating

the value of any electrical, thermal, mechanical or environmental quantity assigned to define the operating conditions under which a component, machine, apparatus, electronic device, etc., is expected to give satisfactory service

NOTE "Rating" is a generic term but see also "Rating (limiting value)".

1.1.3.1.16

rating (limiting value)

a rating which establishes either a limiting capability or a limiting condition beyond which damage to the device may occur

NOTE Limiting conditions may be either maxima or minima, known as "maximum ratings" and "minimum ratings" respectively. for further information on rating systems, see IEC publication 134

1.1.3.1.17

breakpoint

the temperature at the point on a derating curve relating a specified parameter to the reference point temperature, at which the value of the specified parameter begins to fall below its maximum

1.1.3.1.18**reference axis (main axis)**

the axis which lies in a plane passing through the centre of the device and parallel with the leads, pins and/or stud of the device

1.1.3.1.19**Forward direction**

a) Of a p-n junction or a semiconductor diode. The direction of the flow of unidirectional current in which the junction or diode has the lower resistance.

b) Of a tunnel diode. The direction of current flow within the diode for which the characteristic includes negative differential conductance.

1.1.3.1.20**Reverse direction**

a) Of a p-n junction or a semiconductor diode. The direction of the flow of unidirectional current in which the junction or diode has the higher resistance.

b) Of a tunnel diode. The direction of current flow within the diode for which the characteristic includes only positive differential conductance.

1.1.3.1.21**pulse**

a flow of electrical energy of short duration which is deliberately generated (see Figure 1)

1.1.3.1.22**pulse average time**

the time duration from a point on the leading edge which is 50 % of the maximum amplitude to a point on the trailing edge which is 50 % of the maximum amplitude (see Figure 1)

1.1.3.1.23**pulse fall time**

that time duration during which the amplitude of its trailing edge is decreasing from 90 % to 10 % of the maximum amplitude (see Figure 1)

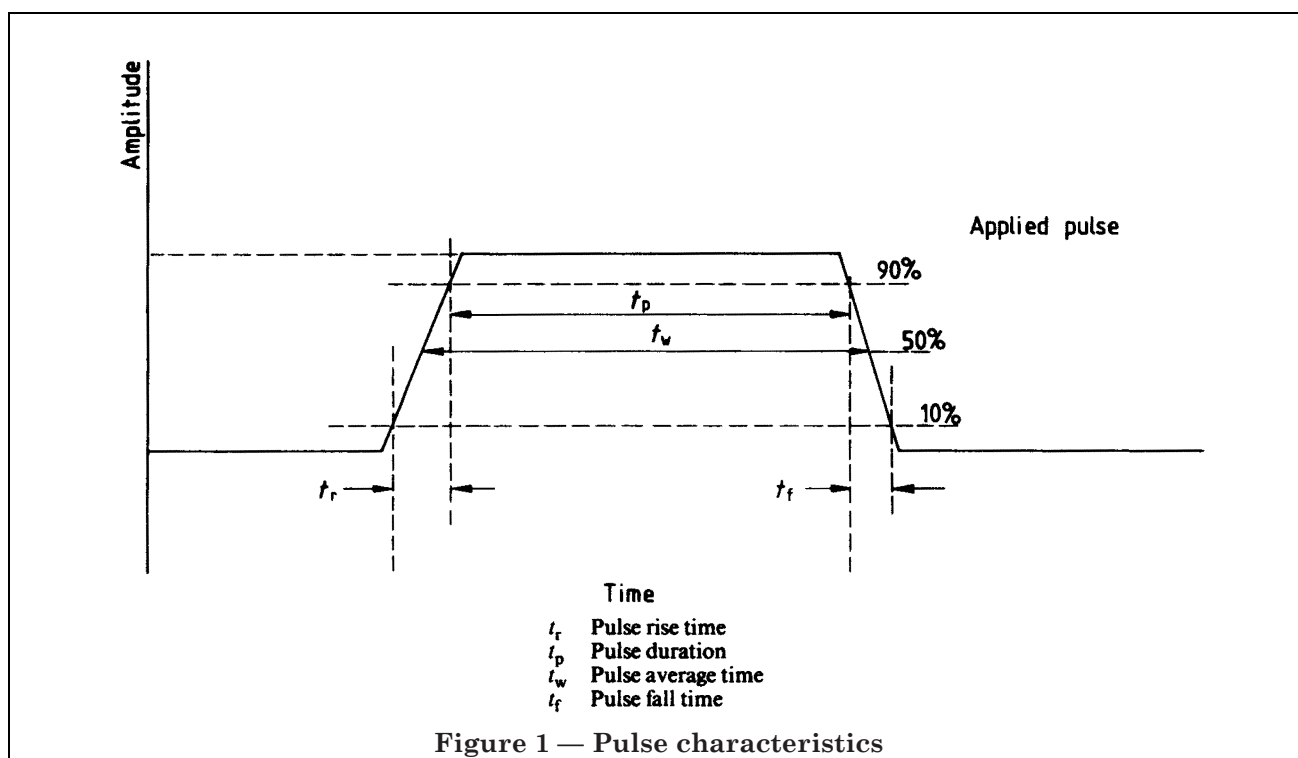


Figure 1 — Pulse characteristics

1.1.3.1.24**pulse rise time**

that time duration during which the amplitude of its leading edge is increasing from 10 % to 90 % of the maximum amplitude (see Figure 1)

1.1.3.1.25**pulse duration**

the time duration from the point on the leading edge which is 90 % of the maximum amplitude to the point on the trailing edge which is 90 % of the maximum amplitude (see Figure 1)

1.1.3.1.26**reverse recovery time**

the time required for the current or voltage to recover to a specified value

1.1.3.1.27**breakdown** (of a reverse biased p-n junction)

a phenomenon, the initiation of which is observed as a transition from a state of high dynamic resistance to a state of substantially lower dynamic resistance for increasing magnitude of reverse voltage

1.1.3.1.28**avalanche breakdown** (of a p-n junction)

a breakdown that is caused by the cumulative multiplication of free charge carriers in a semiconductor under the action of a strong electric field which causes some free carriers to gain enough energy to liberate new hole-electron pairs by ionization

1.1.3.1.29**thermal equilibrium**

the state of equilibrium which is reached when a two-to-one increase in the test time interval does not produce a change due to thermal effects in the parameter being measured that is greater than the required accuracy of the measurement

1.1.3.1.30**thermal derating factor**

the factor by which the power dissipation rating must be reduced with increase of ambient or case temperature

1.1.3.1.31**thermal resistance** (of a semiconductor device)

the quotient of the temperature difference between two specified points or regions and the heat flow between these two points or regions under conditions of thermal equilibrium

NOTE For most case the heat flow can be assumed to be equal to the power dissipation.

1.1.3.1.32**transient thermal impedance**

the temperature rise between two specified points, per unit power dissipation applied for a specified time interval

NOTE This data is usually presented as a curve of °C/W versus time.

1.1.3.1.33**ambient temperature**

the air temperature measured below a semiconductor device in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces

1.1.3.1.34**reference point temperature**

the temperature measured at a specified point on the device

NOTE This point may, for example, be the mounting base, case or stud.

1.1.3.1.35**storage temperature**

the temperature at which the device is stored without any voltage applied

1.1.3.1.36**noise factor**

the ratio of the available signal-to-noise power ratio at the input to the available signal-to-noise power ratio at the output of the device

1.1.3.1.37**noise figure**

the noise factor expressed in decibels

1.1.3.1.38**virtual junction temperature**

a theoretical temperature which is based on a simplified representation of the thermal and electrical behaviour of a semiconductor device

1.1.3.2 General characteristic terms**1.1.3.2.1****forward current** (of a diode)

the current flowing through the diode in the forward direction

1.1.3.2.2**mean forward current**

the value of the forward current averaged over a specified time. For a large-current diode or thyristor the specified time is a full cycle

1.1.3.2.3**Reverse current**

- a) Of a diode. The current flowing through the diode in the reverse direction.
- b) Of a thyristor. The principal current for negative anode voltage.

1.1.3.2.4**anode-to-cathode voltage** (abbreviation: anode voltage)

the voltage between the anode terminal and the cathode terminal

NOTE It is called positive when the anode is positive with respect to the cathode and negative when the anode is negative with respect to the cathode.

1.1.3.2.5**applied voltage** (on a terminal)

the voltage between the terminal and the reference point

1.1.3.2.6 Forward voltage**1.1.3.2.6.1****of a diode**

the voltage across the terminals which results from the flow of current in the forward direction

1.1.3.2.6.2**of a thyristor**

a positive anode voltage

1.1.3.2.7**Reverse voltage**

- a) The voltage across a junction or a diode in the reverse direction.
- b) Of a thyristor. A negative anode voltage.

1.1.3.2.8**continuous (direct) reverse voltage**

the value of the constant voltage applied to a diode in the reverse direction

1.1.3.2.9

mean reverse voltage

the value of the reverse voltage averaged over a specified time

1.1.3.2.10

crest working reverse voltage

the highest instantaneous value of the reverse voltage which occurs across a semiconductor diode or reverse-blocking thyristor, excluding all repetitive and non-repetitive transient voltages

1.1.3.2.11

repetitive peak reverse voltage

the highest instantaneous value of the reverse voltage which occurs across a semiconductor diode or reverse-blocking thyristor including all repetitive transient voltages but excluding all non-repetitive transient voltages

1.1.3.2.12

non-repetitive peak reverse voltage

the highest instantaneous value of any non-repetitive transient reverse voltage which occurs across a semiconductor diode or reverse-blocking thyristor

NOTE The repetitive voltage is usually a function of the circuit and increases the power dissipation of the device. A non-repetitive transient voltage is usually due to an external cause and it is assumed that its effect has completely disappeared before the next transient arrives.

1.1.3.2.13

floating voltage

the voltage between an open-circuited terminal and the reference point when a specified voltage is applied to any of the other terminals

1.1.3.2.14

forward d.c. resistance (of a diode)

the quotient of forward voltage across the diode and the corresponding forward current

1.1.3.2.15

reverse d.c. resistance (of a diode)

the quotient of reverse voltage across the diode and the corresponding reverse current

1.1.3.2.16

breakdown voltage

the reverse voltage at which the reverse current of the junction becomes greater than a specified value

1.1.3.2.17

avalanche voltage

the applied voltage at which avalanche breakdown occurs

1.1.3.2.18

total power loss (of a semiconductor device)

the sum of the losses due to currents in the forward and reverse directions under specified conditions

1.1.3.2.19

cut-off frequency

the frequency at which the modulus of a measured parameter has decreased to $1/\sqrt{2}$ of its mid-frequency value

NOTE For a transistor, the cut-off frequency usually applies to the short-circuit small-signal forward current transfer ratio for either the common-base or common-emitter configuration.

1.1.3.2.20

forward recovery time (of a diode)

the time required for the current or voltage to recover to a specified value after instantaneous switching from zero or a specified reverse voltage to a specified forward bias condition

1.1.3.2.21

reverse recovery time (of a diode)

the time required for the current or voltage to recover to a specified value after instantaneous switching from a specified forward current condition to a specified reverse bias condition

1.1.3.3 Signal diodes**1.1.3.3.1**

signal diode

a semiconductor diode used for the purpose of extracting or processing information contained in an electrical signal which varies with time and may be either analogue or digital in nature

1.1.3.3.2

semiconductor photo-diode

a semiconductor diode utilizing the photo-electric effect

1.1.3.3.3

differential resistance

the resistance measured between the terminals of the diode under small-signal and specified bias conditions

1.1.3.3.4

small-signal capacitance

the differential capacitance at the diode terminals, measured under specified bias conditions

1.1.3.3.5

impedance at the intermediate frequency (of a mixer semiconductor diode)

the impedance measured at the output terminals of the mixer circuit when the device is driven by the local oscillator under specified conditions

1.1.3.3.6

radio frequency impedance

the input impedance, at radio frequency, of a diode measured under specified conditions

1.1.3.3.7

video impedance (of a detector diode)

the output impedance measured at a video frequency when the diode is operating under specified bias conditions

1.1.3.3.8

recovered charge

the total charge recovered from the diode after switching from a specified forward current condition to a specified reverse condition

NOTE This charge includes components due to both carrier storage and depletion layer capacitance.

1.1.3.3.9

detector voltage efficiency

the ratio of the d.c. load voltage to the peak sinusoidal input voltage under specified circuit conditions

1.1.3.3.10

detector power efficiency

the ratio of the change in d.c. power in the load resistance produced by the a.c. signal, to the available power from a sinusoidal voltage generator when the diode is operated under specified conditions

1.1.3.3.11

dynamic impedance

the quotient of the change in voltage and the corresponding change in current, under specified test conditions

1.1.3.4 Voltage reference, voltage regulator and clipper diodes

1.1.3.4.1

voltage-reference diode

a diode which develops across its terminals a reference voltage of specified accuracy when biased within a specified current range

1.1.3.4.2

voltage-regulator diode

a diode which develops across its terminals an essentially constant voltage throughout a specified current range

1.1.3.4.3

clipper diode

a bi-directional voltage regulator diode which develops across its terminals an essentially constant voltage throughout a specified current range for both directions of current flow

1.1.3.4.4

voltage-temperature coefficient

the change in voltage measured under specified conditions over a specified range of ambient or case temperature. It is expressed as percentage change per degree centigrade

1.1.3.4.5

breakdown voltage regulation

the change in breakdown voltage between two specified values of reverse current measured in the breakdown region of the voltage-current characteristic

1.1.3.5 Tunnel diodes

1.1.3.5.1

tunnel diode

a diode utilizing the tunnel effect

NOTE The tunnel effect gives rise to negative differential conductance in a certain range of the forward direction of the current-voltage characteristic.

1.1.3.5.2

unitunnel diode

a tunnel diode whose peak and valley point currents are approximately equal

1.1.3.5.3

tunnel effect (in a p-n transition region)

a process whereby conduction occurs through a potential barrier and in which electrons pass in either direction between the conduction band in the n-region and the valence band in the p-region

NOTE The tunnel effect, unlike the diffusion of charge carriers, involves electrons only and is for all purposes an instantaneous process.

1.1.3.5.4

negative differential conductance region

that part on the characteristic of a tunnel diode between the peak and valley points (see Figure 2)

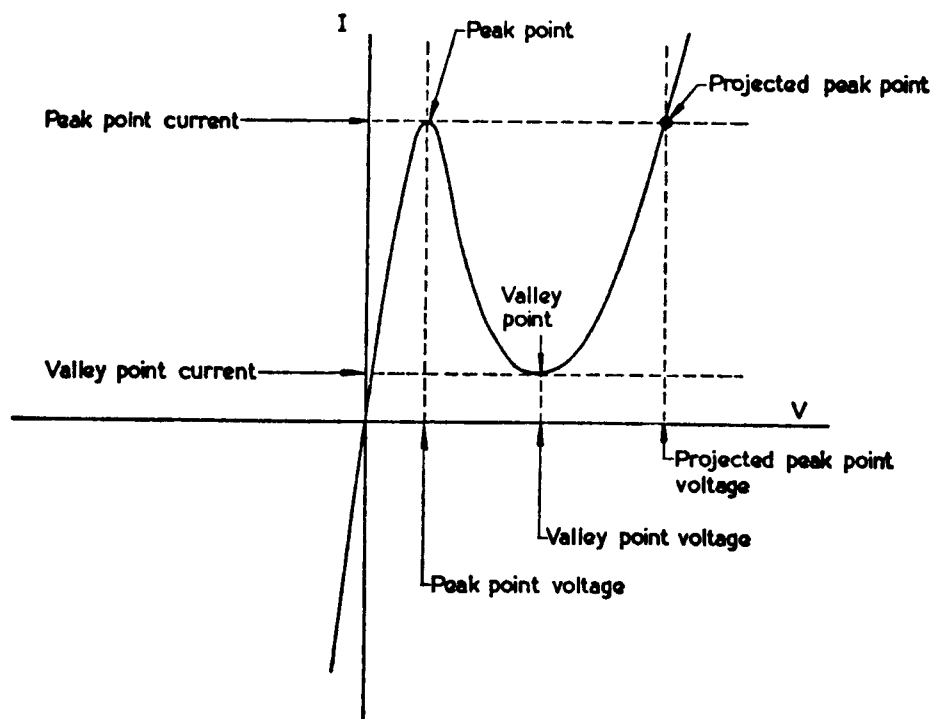


Figure 2 — Static current-voltage characteristic of a tunnel diode

1.1.3.5.5

peak point

the point on the characteristic of a tunnel diode corresponding to the lowest voltage in the forward direction for which the differential conductance is zero (see Figure 2)

1.1.3.5.6

valley point

the point on the characteristic of a tunnel diode corresponding to the lowest voltage greater than the peak point voltage for which the differential conductance is zero (see Figure 2)

1.1.3.5.7

projected peak point

the point on the characteristic of a tunnel diode where the current is equal to the peak point current, but where the voltage is greater than the valley point voltage (see Figure 2)

1.1.3.5.8

peak point current

the current value at the peak point

1.1.3.5.9

valley point current

the current value at the valley point

1.1.3.5.10

peak to valley point current ratio

the ratio of the peak point current to the valley point current

1.1.3.5.11

peak point voltage

the voltage value at the peak point

1.1.3.5.12**valley point voltage**

the voltage value at the valley point

1.1.3.5.13**projected peak point voltage**

the voltage value at the projected peak point

1.1.3.5.14**resistive cut-off frequency**

the frequency at which the real part of the tunnel diode admittance at its terminals is zero at the specified bias point

1.1.3.5.15**self resonant frequency**

the frequency at which the reactive part of the diode admittance at its terminals is zero at the specified bias point

NOTE The self resonant frequency is given by the formula:

$$f_r = \frac{1}{2\pi} \sqrt{\frac{1}{L_s(C' + C_s)} - \left(\frac{g'}{C'}\right)^2}$$

where C_s = stray (parallel) capacitance,

C' = diode capacitance,

g' = modulus of the diode negative differential conductance,

L_s = total series equivalent inductance.

1.1.3.5.16**case capacitance**

the residual capacitance between the device terminals when the p-n junction is not internally connected

1.1.3.5.17**series inductance**

the total effective internal series inductance under specified conditions

1.1.3.6**variable capacitance diode**

a diode, the terminal capacitance of which varies in a defined manner as an inverse function of voltage when biased in the reverse direction

1.1.3.7 Microwave diodes

The following terms and definitions apply only to microwave diodes:

1.1.3.7.1**microwave diode**

a diode designed for operation at frequencies of one gigahertz and above

1.1.3.7.2**cut-off frequency**

the frequency at which the reactive component of the diode impedance is equal to the resistive component when the diode is operating under specified bias and test mount conditions

1.1.3.7.3**overall noise factor**

the ratio of **1.1.3.7.1** the available signal-to-noise power ratio at the input to **1.1.3.7.2** the available signal-to-noise power ratio at the output of a network comprising the diode, test mount, and specified amplifier

1.1.3.7.4**noise ratio (Noise temperature ratio)**

the ratio of **1.1.3.7.1** the available noise power output generated by a diode within a given band of frequencies when the diode is operating under specified conditions to **1.1.3.7.2** the available thermal noise power generated within the same band of frequencies by a resistor at a reference temperature of 293 K

1.1.3.7.5**low frequency noise power (Flicker noise power)**

the low frequency sideband noise power generated by the diode when it is operating under specified conditions. This noise power is characterized approximately by a $\frac{1}{f}$ law, where f is the sideband displacement frequency

1.1.3.7.6**low frequency noise ratio (Flicker noise ratio)**

the ratio of **1.1.3.7.1** the low frequency noise power within a given band of frequencies when the diode is operating under given conditions to **1.1.3.7.2** a reference input power of 1 mW

NOTE This is sometimes expressed as the ratio of **1.1.3.7.1** the low frequency noise power within a given band of frequencies when the diode is operating under given conditions to **1.1.3.7.2** the available thermal noise power generated within the same band of frequencies by a resistor at a reference temperature of 293 K.

1.1.3.7.7**tangential sensitivity (of a diode used as a video detector in combination with a linear amplifier and a display system)**

that pulse power which gives a display amplitude equal to that given by the combined noise power of the diode and amplifier

1.1.3.7.8**voltage sensitivity**

the voltage per unit input power developed across a specified load resistor connected in parallel with the diode

1.1.3.7.9**current sensitivity**

the rectified short-circuit current per unit input power

1.1.3.7.10**figure of merit (of a diode used as a video detector)**

the product of the short-circuit current sensitivity and the square root of the small-signal dynamic impedance at zero bias

1.1.3.7.11**spike**

an electrical impulse of duration less than the thermal time constant of the diode

1.1.3.7.12**burnout**

the overload capability of a microwave diode

1.1.3.7.13**pulse**

a brief variation of a quantity above or below a stated datum level; this variation is characterized by a rise and a decay and has a finite duration

1.1.3.7.14**R.F. power pulse**

a pulse in which the varying quantity is the r.f. power

1.1.3.7.15

average pulse amplitude (of a nominally flat topped pulse)

the value of the pulse determined by the height of the mid-point of a straight line through the average of the variations on the top of the pulse measured at the mid point of the pulse

NOTE 1 In the case of a pulse whose duration is of 1 μ s or more it is usual to ignore overshoots having a duration of less than 10 % of the pulse duration.

NOTE 2 In the case of a distorted pulse it may be necessary to correct the amplitude as defined to obtain agreement with the measurement of the average of the appropriate pulse quantity throughout the pulse duration.

1.1.3.7.16

pulse duration

the time interval between the instants at which the value of the pulse quantity equals a specified fraction of the pulse amplitude

1.1.3.7.17

pulse repetition frequency

the average number of pulses in unit time when this is independent of the interval of time over which it is measured

1.1.3.7.18

pulse repetition period

the reciprocal of pulse repetition frequency

1.1.3.8 Rectifier diodes

1.1.3.8.1

rectifier diode

a diode designed for rectification and including its associated mounting and cooling attachments, if integral with it

1.1.3.8.2

repetitive peak forward current

the peak value of the forward current, including all repetitive transient currents

NOTE It is related to the mean forward current by a factor which depends upon the circuit and upon the waveform of the supply voltage.

1.1.3.8.3

overload forward current

a forward current of substantially the same wave-shape as the normal forward current and having a greater value than the specified normal forward current

NOTE The normal forward current is the current which passes through the device under steady state conditions.

1.1.3.8.4

surge (non-repetitive) forward current

a forward current pulse of short time duration and of specified wave-shape

1.1.3.8.5

surge current rating

the maximum current pulse which can be carried by the semiconductor diode for the specified length of time, repetition frequency, waveform and temperature

1.1.3.9 Thyristors

These terms and definitions, whilst not identical to those agreed by IEC/TC 47 are nevertheless compatible with them.

1.1.3.9.1

thyristor

a bistable semiconductor device comprising three or more junctions which can be made conductive at any instant when the anode (or principal) voltage is positive

NOTE The term "thyristor" may be used either as a generic term or as an abbreviation for "reverse blocking triode thyristor".

1.1.3.9.2**reverse blocking thyristor**

a thyristor which, for negative anode voltage, cannot be made conductive, i.e. it exhibits a reverse blocking state

1.1.3.9.3**diode thyristor**

a two electrode thyristor, commonly with two terminals

1.1.3.9.4**triode thyristor**

a three electrode thyristor, of which one electrode is the gate. Commonly it has three terminals

1.1.3.9.5**reverse conducting diode thyristor**

a diode thyristor which is inherently conductive when the anode voltage is negative

1.1.3.9.6**reverse conducting triode thyristor**

a triode thyristor which is inherently conductive when the anode voltage is negative

1.1.3.9.7**bi-directional triode thyristor (triac)**

a three terminal thyristor having substantially the same switching behaviour in the first and third quadrants of the principal characteristic

1.1.3.9.8**turn-off thyristor**

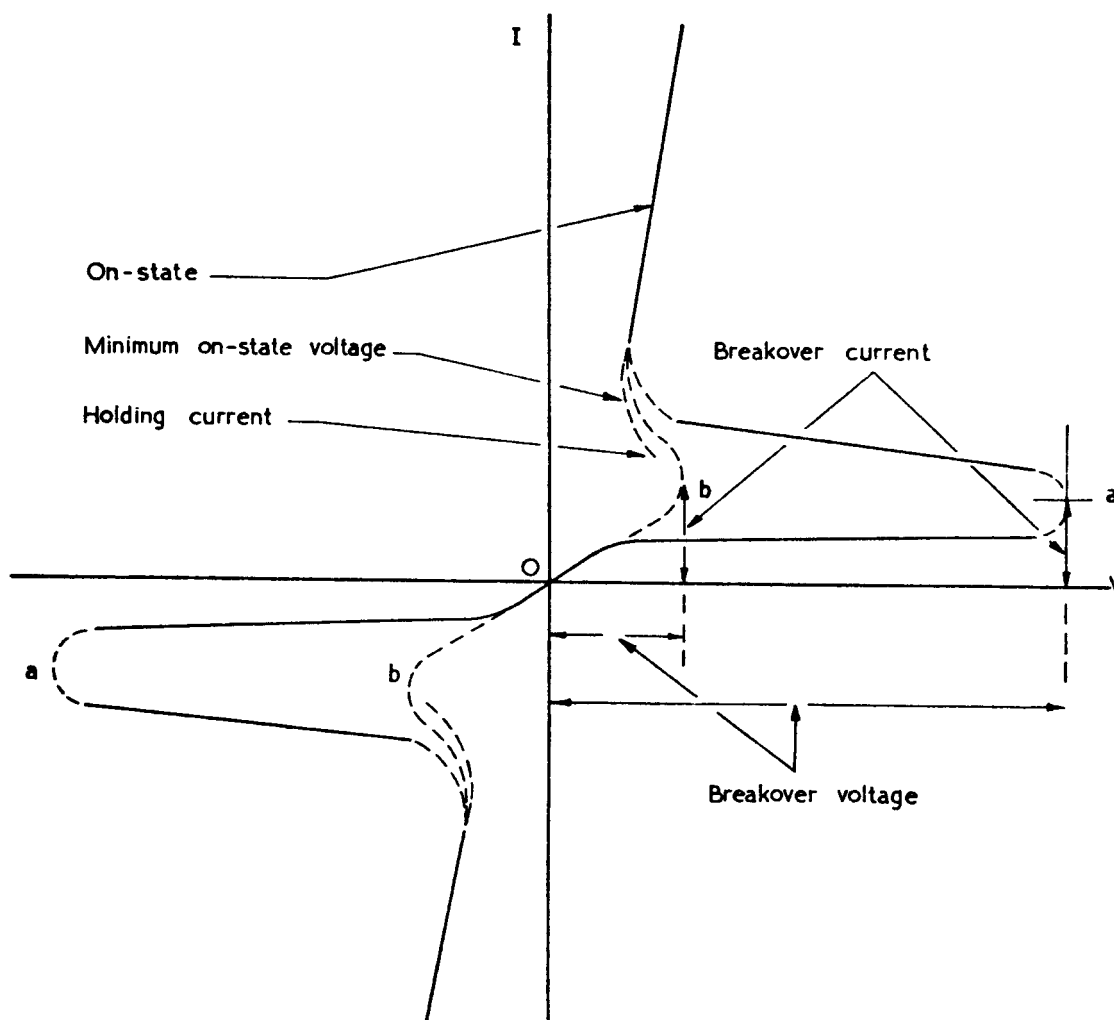
a thyristor which can be switched from the on-state to the off-state by applying an appropriate control signal to the gate

1.1.3.9.9**p-gate thyristor**

a thyristor in which the gate terminal is connected to the p-region nearest the cathode and which is normally switched to the on-state by applying a positive signal between gate and cathode terminals

1.1.3.9.10**n-gate thyristor**

a thyristor in which the gate terminal is connected to the n-region nearest the anode and which is normally switched to the on-state by applying a negative signal between gate and anode terminals



NOTE Curve (a) corresponds to zero gate current or to a diode thyristor.
Curve (b) is with gate current present.

Figure 3 — Voltage current characteristic for bi-directional diode (diac) and bi-directional triode thyristor (triac)

1.1.3.9.11

main terminal 1 (of a bi-directional thyristor)

the main terminal which is named "1" by the manufacturer

1.1.3.9.12

main terminal 2 (of a bi-directional thyristor)

the main terminal which is named "2" by the manufacturer

1.1.3.9.13

gate terminal

a terminal to or from which only control current flows

NOTE This control current is usually called the gate current.

1.1.3.9.14

principal current

the current which flows through the main terminals of a bi-directional thyristor or through the anode and cathode terminals of a reverse blocking or a reverse conducting thyristor

1.1.3.9.15

principal voltage

the voltage between the main terminals of a bi-directional thyristor or between the anode and cathode terminals of a reverse blocking or a reverse conducting thyristor

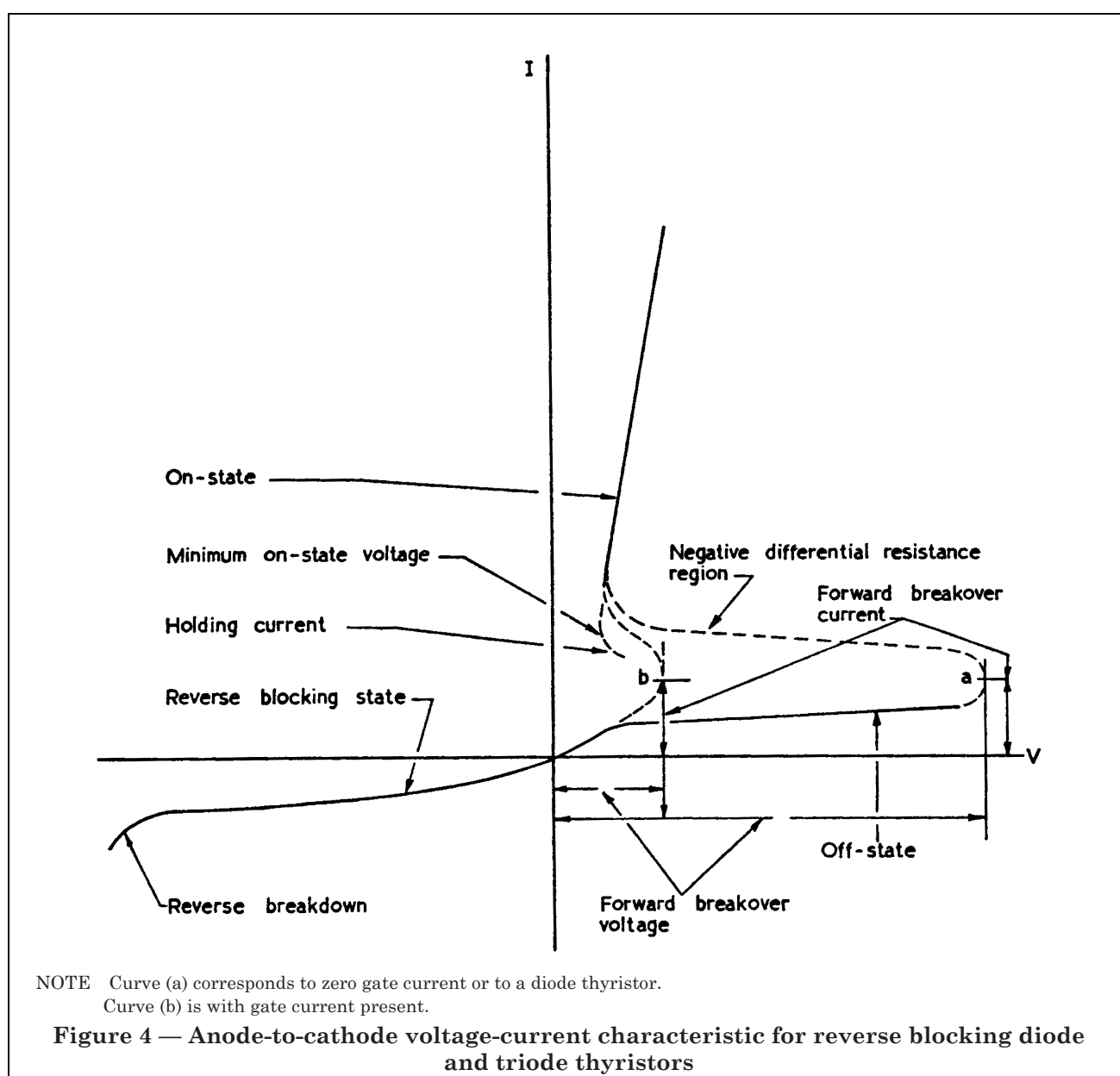
NOTE 1 In the case of bi-directional thyristor the principal voltage is called positive when the main terminal 1 is positive with respect to main terminal 2.

NOTE 2 In the case of a reverse blocking or a reverse conducting thyristor, the principal voltage is called positive when the anode is positive with respect to the cathode and negative when the anode is negative with respect to the cathode

1.1.3.9.16

principal (voltage-current) characteristic

a function, usually represented graphically, relating the principal voltage to the principal current, with the gate current, where applicable, as a parameter (see Figure 3 for bi-directional thyristors)



1.1.3.9.17

anode (to cathode voltage current) characteristic

a function, usually represented graphically, relating the anode voltage to the principal current, with gate current, where applicable, as a parameter (see Figure 4)

NOTE Where no confusion is likely to occur the term can be abbreviated to “anode characteristic” or “characteristic”.

1.1.3.9.18

on-state

the condition of a thyristor corresponding to the low-resistance low-voltage portion of the principal characteristic

NOTE In the case of reverse conducting devices, this definition is applicable only for positive anode voltage.

1.1.3.9.19

on-state current

the principal current when the thyristor is in the on-state

1.1.3.9.20

holding current

the minimum principal current required to maintain the thyristor in the on-state

1.1.3.9.21

latching current

that minimum value which the principal current must have reached in order that the thyristor will remain in the on-state after the triggering signal is removed

1.1.3.9.22

continuous (direct) on-state current

the value of the constant on-state current

1.1.3.9.23

repetitive peak on-state current

the peak value of the on-state current including all repetitive transient currents

1.1.3.9.24

overload on-state current

an on-state current of substantially the same wave-shape as the normal on-state current but having a greater magnitude than the normal on-state current

NOTE The normal on-state current is the current which passes through the device under steady state conditions.

1.1.3.9.25

surge (non-repetitive) on-state current

an on-state current of short time duration and specified wave-shape

1.1.3.9.26

critical rate of rise of on-state current

the maximum value of the rate of rise of on-state current which a thyristor can withstand without deleterious effect

1.1.3.9.27

mean on-state current (of a reverse blocking thyristor)

the mean value of the on-state current averaged over a full cycle

1.1.3.9.28

R.M.S. on-state current (of a bi-directional thyristor)

the r.m.s. value of the on-state current for a full cycle

1.1.3.9.29

on-state voltage

the principal voltage when the thyristor is in the on-state

1.1.3.9.30**on-state threshold voltage**

the value of the voltage obtained at the intersection of the voltage axis and the straight line which represents approximately the characteristic of the thyristor in the on-state

1.1.3.9.31**on-state slope resistance**

the value of the resistance calculated from the slope of the straight line used when determining the on-state threshold voltage

1.1.3.9.32**off-state**

the condition of a thyristor corresponding to the portion of the principal characteristic between the origin and the breakover point or points

1.1.3.9.33**off-state current**

the principal current when the thyristor is in the off-state

1.1.3.9.34**off-state voltage**

the principal voltage when the thyristor is in the off-state

1.1.3.9.35**continuous (direct) off-state voltage**

the value of the constant voltage applied to the thyristor when it is in the off-state

1.1.3.9.36**crest working off-state voltage**

the highest instantaneous value of the off-state voltage which occurs across the thyristor, excluding all repetitive and non-repetitive transient voltages

1.1.3.9.37**repetitive peak off-state voltage**

the highest instantaneous value of the off-state voltage which occurs across the thyristor including all repetitive transient voltages but excluding all non-repetitive transient voltages

1.1.3.9.38**non-repetitive peak off-state voltage**

the highest instantaneous value of any non-repetitive transient off-state voltage which occurs across the thyristor

NOTE A repetitive voltage is usually a function of the circuit and increases the power dissipation of the device. A non-repetitive transient voltage is usually due to an external cause and it is assumed that its effect has completely disappeared before the next transient arrives.

1.1.3.9.39**critical rate of rise of off-state voltage**

the minimum value of the rate of rise of voltage which will cause switching from the off-state to the on-state under specified conditions

1.1.3.9.40**reverse blocking state**

the condition of a reverse blocking thyristor corresponding to the portion of the anode characteristic for reverse currents of lower magnitude than the current at the reverse breakdown voltage

1.1.3.9.41**reverse blocking current (of a reverse blocking thyristor)**

the reverse current when a reverse blocking thyristor is in the reverse blocking state

1.1.3.9.42

continuous (direct) reverse voltage

the value of the constant voltage applied to the thyristor when it is in the reverse blocking state

1.1.3.9.43

breakover point

the point on the principal characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value (see Figure 4)

1.1.3.9.44

negative differential resistance region

any portion of the principal characteristic within which the differential resistance is negative (see Figure 4)

1.1.3.9.45

breakover current

the principal current at the breakover point (see Figure 4)

1.1.3.9.46

breakover voltage

the principal voltage at the breakover point (see Figure 4)

1.1.3.9.47

reverse breakdown voltage (of a reverse blocking thyristor)

the reverse voltage at which the reverse current becomes greater than a specified value (see Figure 4)

1.1.3.9.48

forward gate current

the gate current corresponding to the forward gate voltage

1.1.3.9.49

peak forward gate current

the highest instantaneous value of forward gate current including all transient currents

1.1.3.9.50

reverse gate current

the gate current corresponding to the reverse gate voltage

1.1.3.9.51

gate trigger current

the lowest gate current required to switch a thyristor from the off-state to the on-state

1.1.3.9.52

gate non-trigger current

the highest gate current which will not cause the thyristor to switch from the off-state to the on-state

1.1.3.9.53

gate turn-off current

the lowest gate current required to switch a thyristor from the on-state to the off-state

NOTE Not all thyristors can be turned off by the gate.

1.1.3.9.54

gate voltage

the voltage between a gate terminal and a specified main terminal

1.1.3.9.55

forward gate voltage

the negative gate-to-anode voltage for n-gate thyristors. The positive gate-to-cathode voltage for p-gate thyristors

1.1.3.9.56**peak forward gate voltage**

the highest instantaneous value of forward gate voltage including all transient voltages

1.1.3.9.57**reverse gate voltage**

the positive gate-to-anode voltage for n-gate thyristors. The negative gate-to-cathode voltage for p-gate thyristors

1.1.3.9.58**peak reverse gate voltage**

the highest instantaneous value of reverse gate voltage including all transient voltages

1.1.3.9.59**gate trigger voltage**

the gate voltage required to produce the gate trigger current

1.1.3.9.60**gate non-trigger voltage**

the highest gate voltage which will not cause the thyristor to switch from the off-state to the on-state

1.1.3.9.61**gate turn-off voltage**

the gate voltage required to produce the gate turn-off current

NOTE Not all thyristors can be turned off by the gate.

1.1.3.9.62**gate controlled turn-on time**

the time interval during which the thyristor is switching from the off-state to the on-state as a result of the application of a gate trigger pulse (see Figure 5)

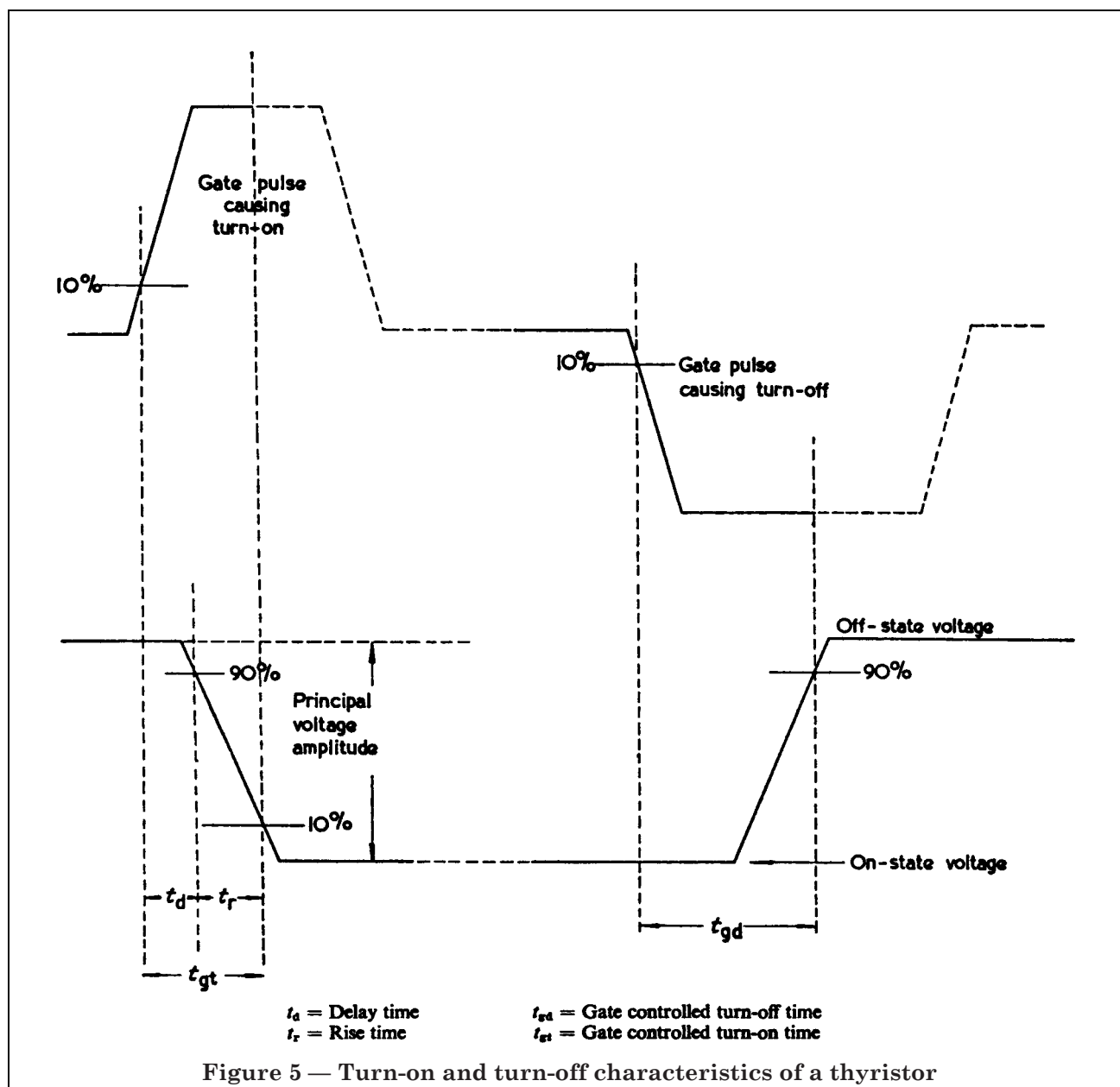
NOTE 1 The interval is usually measured from the 10 % point on the gate pulse to the instant at which the principal voltage has dropped to 10 % of its initial value.

NOTE 2 The turn-on time is the sum of the delay time and the rise time.

1.1.3.9.63**gate controlled rise time**

the time interval between the instant when the principal voltage has dropped from a specified value, near its initial value, and the instant when it reaches a specified low value, during the switching of a thyristor from the off-state to the on-state by a gate pulse (see Figure 5)

NOTE Where no confusion is likely to occur, the term can be abbreviated to "rise time".



1.1.3.9.64

gate controlled turn-off time

the time interval during which the thyristor is switching from the on-state to the off-state as a result of the application of a gate trigger pulse (see Figure 5)

NOTE The interval is usually measured from the 10 % point on the gate pulse, to the instant at which the principal voltage has increased to 90 % of the off-state voltage.

1.1.3.9.65

circuit commutated turn-off time (circuit commutated recovery time)

the time interval between the instant when the principal current has decreased to zero after external switching of the main circuits, and the instant when the thyristor is capable of supporting a specified principal voltage without turning on (see Figure 6)

1.1.3.10 Transistors

1.1.3.10.1 transistor

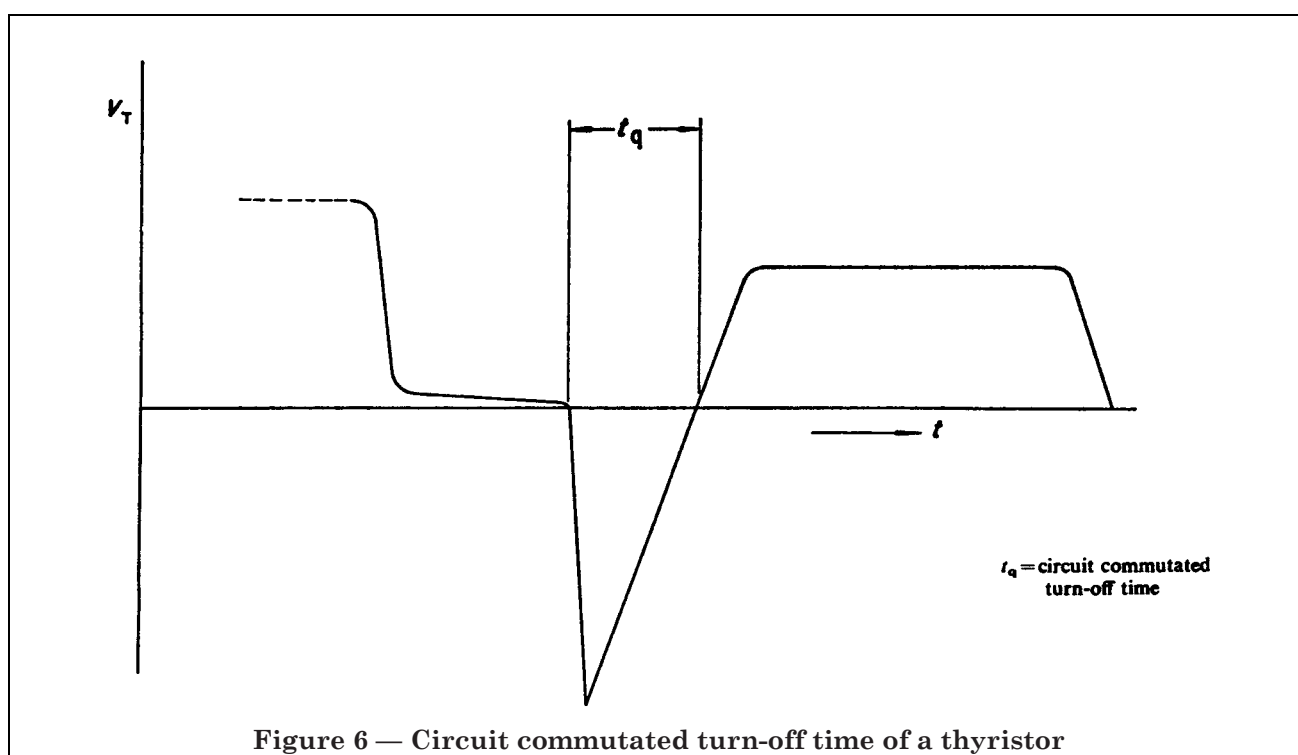
a semiconductor device capable of providing power amplification and having three or more terminals

1.1.3.10.2 bi-directional transistor

a transistor which has substantially the same electrical characteristics when the emitter and collector terminals are interchanged

1.1.3.10.3 photo-transistor

a transistor utilizing the photo-electric effect



1.1.3.10.4 emitter junction

a junction between the base and emitter regions normally biased in the forward direction, and through which the charge carriers flow from a region in which they are majority carriers to one in which they are minority carriers

1.1.3.10.5 collector junction

a junction between the base and collector regions normally biased in the reverse direction and through which the charge carriers flow from a region in which they are minority carriers to one in which they are majority carriers

1.1.3.10.6 base region

a region between the emitter and collector junctions of a transistor into which minority carriers are injected

1.1.3.10.7

emitter region

that part of a transistor lying between the emitter junction and the emitter electrode from which carriers flow across the emitter junction

1.1.3.10.8

collector region

that part of a transistor lying between the collector junction and the collector electrode, and into which carriers flow from the collector junction

1.1.3.10.9

emitter terminal

the specified externally available point of connection to the emitter region

1.1.3.10.10

collector terminal

the specified externally available point of connection to the collector region

1.1.3.10.11

base terminal

the specified externally available point of connection to the base region

1.1.3.10.12

common base

a circuit configuration in which the base terminal is common to the input circuit and to the output circuit and in which the input terminal is the emitter terminal and the output terminal is the collector terminal

1.1.3.10.13

common emitter

a circuit configuration in which the emitter terminal is common to the input circuit and to the output circuit and in which the input terminal is the base terminal and the output terminal is the collector terminal

1.1.3.10.14

common collector

a circuit configuration in which the collector terminal is common to the input circuit and to the output circuit and in which the input terminal is the base terminal and the output terminal is the emitter terminal

1.1.3.10.15

inverse direction of operation

a mode of operating a transistor in which the nominal collector region acts as an emitter and in which the net flow of minority carriers is from the nominal collector region to the base region

1.1.3.10.16

inverse common base

a circuit configuration in which the base terminal is common to the input circuit and to the output circuit and in which the input terminal is the collector terminal and the output terminal is the emitter terminal

1.1.3.10.17

inverse common emitter

a circuit configuration in which the emitter terminal is common to the input circuit and to the output circuit and in which the input terminal is the collector terminal and the output terminal is the base terminal

1.1.3.10.18

inverse common collector

a circuit configuration in which the collector terminal is common to the input circuit and to the output circuit and in which the input terminal is the emitter terminal and the output terminal is the base terminal

1.1.3.10.19

emitter cut-off current

the reverse current of the base-emitter junction when the collector is open circuited, the reverse voltage being specified

1.1.3.10.20**collector cut-off current**

the reverse current of the base-collector junction when the emitter is open circuited, the reverse voltage being specified

1.1.3.10.21**static input voltage**

the continuous (direct) voltage at the input terminals under specified bias and termination conditions

1.1.3.10.22**saturation voltage** (of a transistor)

the residual voltage between collector and emitter terminals under specified conditions of base current and collector current, the collector current being limited by the external circuit

1.1.3.10.23**punch-through voltage**

the value of the collector-base voltage above which the open-circuit emitter-base voltage increases almost linearly with increasing collector base voltage

NOTE At this voltage, the collector depletion layer extends through the base to the emitter depletion layer.

1.1.3.10.24**input capacitance**

the capacitance measured across the input terminals with specified output conditions

1.1.3.10.25**output capacitance**

the capacitance measured across the output terminals with specified input conditions

1.1.3.10.26**emitter depletion layer capacitance**

the part of the capacitance across an emitter-base junction that is associated with its depletion layer

NOTE The emitter depletion layer capacitance is a function of the total potential drop across the depletion layer.

1.1.3.10.27**collector depletion layer capacitance**

the part of the capacitance across a collector-base junction that is associated with its depletion layer

NOTE The collector depletion layer capacitance is a function of the total potential drop across the depletion layer.

1.1.3.10.28**small-signal open-circuit output admittance**

under small-signal conditions, the quotient of the alternating component of the output current to the alternating component of the voltage applied to the output terminals, with the input open-circuited to alternating current

1.1.3.10.29**small-signal short-circuit forward transfer admittance**

under small-signal conditions, the quotient of the alternating component of the output current to the alternating component of the input voltage, with the output short-circuited to alternating current

1.1.3.10.30**small-signal short-circuit input admittance**

under small-signal conditions, the quotient of the alternating component of the input current to the alternating component of the input voltage, with the output short-circuited to alternating current

1.1.3.10.31**small-signal short-circuit output admittance**

under small-signal conditions, the quotient of the alternating component of the output current to the alternating component of the output voltage, with the input short-circuited to alternating current

1.1.3.10.32**small-signal short-circuit reverse-transfer admittance**

under small-signal conditions, the quotient of the alternating component of the input current to the alternating component of the output voltage, with the input short-circuited to alternating current

1.1.3.10.33**extrinsic base resistance** (of a transistor)

the resistance between the base terminal and the internal inaccessible base point in an equivalent circuit

1.1.3.10.34**emitter series resistance**

the resistance between the emitter terminal and the internal inaccessible emitter point in an equivalent circuit

1.1.3.10.35**collector series resistance**

the resistance between the collector terminal and the internal inaccessible collector point in an equivalent circuit

1.1.3.10.36**saturation resistance** (of a transistor)

the resistance between collector and emitter terminals under specified conditions of base current and collector current, when the collector current is limited by the external circuit

1.1.3.10.37**static value of the short-circuit forward current transfer ratio**

the ratio between the continuous (direct) output current and the continuous (direct) input current, the output voltage being held constant

1.1.3.10.38**small-signal short-circuit forward current transfer ratio**

the ratio between the alternating output current and the small sinusoidal input current producing it under small-signal conditions, the output being short-circuited to alternating current

1.1.3.10.39**inherent (large-signal) forward current transfer ratio**

the difference between the continuous (direct) collector current and the collector base cut-off current divided by the sum of the continuous (direct) base current and the collector-base cut-off current at a specified constant value of the collector-emitter voltage

1.1.3.10.40**transient forward current transfer ratio near saturation**

the ratio of the collector current suddenly demanded from a transistor and the minimum base current necessary to hold it near saturation

1.1.3.10.41**small-signal open-circuit reverse voltage transfer ratio (feedback voltage ratio)**

the ratio of the alternating voltage appearing at the input terminals, when they are open-circuited to alternating current, to the alternating voltage applied to the output terminals, under small-signal conditions

1.1.3.10.42**collector-current multiplication factor**

the ratio of enhanced current flow in the collector as the result of the flow of holes or electrons respectively from an n-type or p-type base region into the collector, to the current carried by these minority carriers, the collector voltage being held constant

NOTE For junction transistors the collector-current multiplication factor is nearly equal to unity.

1.1.3.10.43**base transmission factor** (of a transistor)

the ratio of current carried by minority carriers arriving at the collector junction to that leaving the emitter junction

NOTE The base transmission factor is in general complex, in that it contains the effect of transit times of the minority carriers on the phase of the current arriving at the collector with respect to that leaving the emitter.

1.1.3.10.44**frequency of unity current transfer ratio**

the frequency at which the modulus of the common-emitter small-signal short-circuited forward current transfer ratio h_{fe} has decreased to unity

1.1.3.10.45**transition frequency**

the product of the modulus of the common-emitter small-signal short circuit forward current transfer ratio $|h_{fe}|$ and the frequency of measurement, this frequency being so chosen that $|h_{fe}|$ is decreasing at a slope of approximately 6 dB/octave

1.1.3.10.46**maximum frequency of oscillation**

the maximum frequency at which a transistor can be made to oscillate under specified conditions

NOTE This approximates to the frequency at which the maximum available power gain has decreased to unity.

1.1.3.10.47**delay time** (of a switching transistor)

the time interval between the application at the input terminals of a pulse which is switching the transistor from a non-conducting to a conducting state, and the appearance at the output terminals of the pulse induced by the charge carriers

NOTE The time is usually measured between points corresponding to 10 % of the amplitude of the applied pulse and of the output pulse, respectively (see Figure 7).

1.1.3.10.48**rise time** (of a switching transistor)

the time interval between the instants at which the magnitude of the pulse at the output terminals reaches specified lower and upper limits respectively when the transistor being switched from its non-conducting to its conducting state

NOTE The lower and upper limits are usually 10 % and 90 % respectively, of the amplitude of the output pulse (see Figure 7).

1.1.3.10.49**carrier storage time** (of a switching transistor)

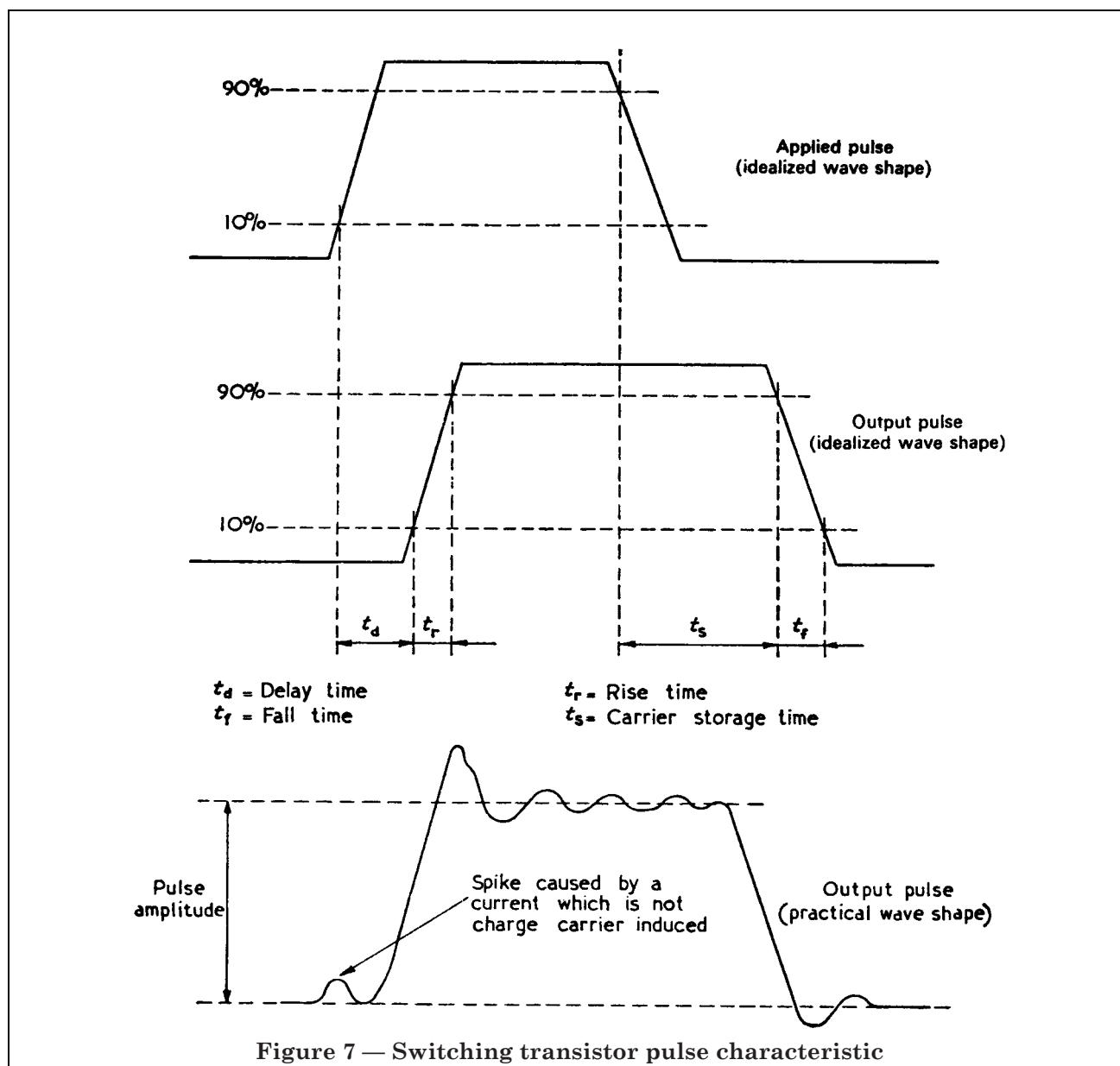
the time interval between the beginning of the fall of the pulse applied to the input terminals and the beginning of the fall of the pulse generated by charge carriers at the output terminals

NOTE The time is generally measured between the 90 % values of the two pulse amplitudes (see Figure 7).

1.1.3.10.50**fall time** (of a switching transistor)

the time interval between the instants at which the magnitude of the pulse at the output terminals reaches specified upper and lower limits respectively when the transistor is being switched from its conducting to its non-conducting state

NOTE The upper and lower limits are usually 90 % and 10 % respectively of the amplitude of the output pulse (see Figure 7).



1.1.3.10.51

collector time coefficient (of a switching transistor)

the quotient of the majority carrier charge introduced via the base electrode of a transistor and the resulting increase in collector current, the collector-emitter voltage being held constant and the emitter-base voltage being initially zero

NOTE The charge is introduced in a time which is short compared with $h_{FE}/2\pi f_1$ where h_{FE} is the static forward current transfer ratio and f_1 is the cut-off frequency.

1.1.3.10.52

saturation-time coefficient

the quotient of the excess majority charge that must be removed from the base electrode of a transistor to bring it out of saturation and the excess base current

NOTE The excess base current and excess majority charge are those which exist with respect to the condition when the collector current becomes limited by the external circuit.

1.1.3.10.53**early voltage**

the point on the graph of collector current versus collector to emitter voltage where the line of the output characteristic, extrapolated backwards, cuts the voltage axis

1.1.3.11 Field effect transistors**1.1.3.11.1****field-effect transistor**

a transistor in which the current flowing through a conducting channel is controlled by an electric field from a voltage applied between the gate and source terminals

1.1.3.11.2**junction-gate field-effect transistor**

a field-effect transistor having one or more gate regions which form p-n junction(s) with the channel

1.1.3.11.3**insulated-gate field-effect transistor**

a field-effect transistor having one or more gate electrodes which are electrically insulated from the channel

1.1.3.11.4**metal-oxide semiconductor field-effect transistor**

an insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material

1.1.3.11.5**n-Channel field-effect transistor**

a field-effect transistor which has an n-type conduction channel

1.1.3.11.6**p-Channel field-effect transistor**

a field-effect transistor which has a p-type conduction channel

1.1.3.11.7**depletion type field-effect transistor**

a field-effect transistor having appreciable channel conductivity for zero gate-source voltage; the channel conductivity may be increased or decreased according to the polarity of the applied gate-source voltage

1.1.3.11.8**enhancement type field-effect transistor**

a field-effect transistor having substantially zero channel conductivity for zero gate-source voltage; the channel conductivity may be increased by the application of a gate-source voltage of appropriate polarity

1.1.3.11.9**triode field-effect transistor**

a field-effect transistor having a gate region, a source region and a drain region

NOTE Where no confusion is possible the term may be abbreviated to "field-effect triode".

1.1.3.11.10**tetrode field-effect transistor**

a field-effect transistor having two independent gate regions, a source region and a drain region

NOTE Where no confusion is possible the term may be abbreviated to "field-effect tetrode".

1.1.3.11.11**source (emitter) region of a field-effect transistor**

a region from which majority carriers flow into the channel

1.1.3.11.12**drain (collector) region of a field-effect transistor**

a region into which majority carriers flow from the channel

1.1.3.11.13

gate region of a field-effect transistor

a region associated with the gate electrode in which the electric field due to the control voltage is effective

1.1.3.11.14

depletion mode operation

the operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value decreases the magnitude of the drain current

1.1.3.11.15

enhancement mode operation

the operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value increases the magnitude of the drain current

1.1.3.11.16

threshold voltage (of an enhancement type field-effect transistor)

the gate-source voltage at which the magnitude of the drain current reaches a specified low value

1.1.3.11.17

cut-off voltage (of a depletion type field-effect transistor)

the gate-source voltage at which the magnitude of the drain current reaches a specified low value

1.1.3.11.18

gate-to-source leakage current

the current flowing through gate and source terminals at specified drain circuit conditions

1.1.3.11.19

input capacitance

the capacitance between gate and source terminals at specified bias and frequency conditions with the drain a.c. short-circuited to the source

1.1.3.11.20

gate resistance

the d.c. resistance between gate and source terminals at specified gate voltage with drain short-circuited to the source

1.1.3.11.21

channel

a thin semiconductor layer between the source region and the drain region, whose conductance is controlled by the gate voltage

1.1.3.11.22

bulk (substrate)

the base material into, or upon which, the field effect transistor is built, exclusive of the package. If made from a semiconductor material, the bulk normally forms a parallel junction-gate with the channel

1.1.3.12

Switching diodes

a diode which exhibits a fast transition from a high resistance state to a low resistance state and vice versa, depending on the d.c. bias voltage/current applied to the diode.

1.1.4

Letter symbols, signs and abbreviations

For the purposes of this standard the abbreviations and letter symbols given in BS 3363 and IEC publication 148 apply.

1.1.5

Graphical symbols

For the purposes of this standard the graphical symbols given in BS 3939 and IEC publication 117 apply.

1.1.6 Marking of the part and package

The following symbols or codes shall be marked on the device in the following order of preference as space permits. All the symbols and codes, except the terminal marking shall also appear on the primary pack, e.g. carton, box, plastics envelope, etc., used as initial protection or wrapping for delivery:

- 1) Terminal identification (see 1.1.6.1).
- 2) Manufacturer's type designation or colour band identification (see 1.1.6.2).
- 3) Factory identification code or manufacturer's name or trade mark and where applicable, the country of origin.
- 4) Date code (see 1.1.6.4).
- 5) British Standard detail specification number.
- 6) BS 9000 symbol (under consideration).

1.1.6.1 Terminal identification. The terminals of semiconductor devices shall be identified in one of the following ways:

- 1) In accordance with the specified outline or base drawing.
- 2) In accordance with one of the following methods, as appropriate.
- 3) As given in the detail specification.

1.1.6.1.1 Diodes and rectifiers. The terminals of all two-terminal diodes and rectifiers shall be clearly indicated by one or more of the following:

- 1) The rectifier arrow graphical symbol pointing towards the cathode.
- 2) A colour code as follows:
 - a) *Diodes and rectifiers in SO-45, BS 3934 (A20, IEC 191-2) and smaller outlines.* The cathode terminal or the part of the body of the device adjacent to the cathode terminal shall be marked by a contrasting colour band.

Where colour band identification (1.1.6.2) is used the cathode end shall be identified by the use of a double width band for the first digit. If there is a possibility of the cathode identification being confused with a colour band identification (1.1.6.2) then the latter shall be omitted.

b) *Diodes and rectifiers in outlines larger than SO-45, BS 3934 (A20, IEC 191-2).* If the terminals of devices in these outlines are identified by a colour code then the cathode terminal shall be indicated with red.

1.1.6.1.2 Transistors. When so specified, transistor terminals shall be identified by the following colour code:

Collector terminal	Red
Emitter terminal	Blue
Base terminal	Yellow
Fourth terminal if present	See below

If the fourth lead is connected to the emitter, the base or the collector, then it should be coded by the appropriate colour for that electrode.

If the fourth lead is connected to anything other than the emitter, the base or the collector, for example if it is connected to a shield, then it should be left uncoded.

When it is appropriate to identify only one terminal the collector shall be marked.

1.1.6.1.3 Thyristors. The detail specification shall identify the terminal numbering.

When any thyristor terminal is identified by colour coding the following colours shall be used:

Cathode terminal(s)	Red
Anode terminal(s)	Blue or black
Gate terminal	Yellow

1.1.6.2 Colour band identification for manufacturer's type number. When specified, the colour code identification for manufacturer's type number shall be as specified in the table opposite. The numbering sequence shall be from left to right, the left being signified by either a wider band of colour or a placement of the colour group towards the left hand edge of the body. Two-digit numbers shall be preceded by a zero.

Colour code for identification number

Colour	Identification number
	First, second, third and fourth digits
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Purple (Violet)	7
Grey	8
White	9

1.1.6.3 Factory identification code, or manufacturer's name or trade-mark. Where the certificate of conformity enables traceability to a manufacturer's factory, the manufacturer's name or trade-mark is sufficient. In all other cases the factory identification code shall be used and shall be in accordance with BS 9002.

1.1.6.4 Date code. The date code should be in accordance with Clause 22 of BS 9000.

1.1.7 Eligibility for qualification approval

The primary stage of processing, in accordance with 14.2 of BS 9000, is for bipolar devices, the first process which changes the monocrystalline semiconductor material from being either wholly p-type or wholly n-type. The primary stage for MOS and Schottky barrier devices is the first oxidation of the substrate. The primary stage for bulk effect devices is the first process which changes the monocrystalline semiconductor material to give the required doping profile.

NOTE This enables an approved manufacturer to use raw materials and piece-parts other than from an approved source, but restricts the use of raw semiconductor material (e.g. germanium, silicon, gallium arsenide) whether in bulk, slice or chip form (with or without an epitaxial layer of the same type) to material of wholly one type (i.e. wholly n-type or wholly p-type), or to raw polycrystalline material.

The primary stage and, in addition, any subsequent stage(s) up to and including the finished product may be carried out by a manufacturer approved within the CECC system in accordance with Clause 14 of BS 9000-1.

For the purpose of subclause i) of Clause 14 of BS 9000-1, plating processes on fully encapsulated devices may be sub-contracted.

The use of subclause ii) of Clause 14 of BS 9000-1 is restricted to the primary stage (diffusion) or to the assembly of the device.

1.1.8 Structurally similar devices

1.1.8.1 Devices from the same production line. In accordance with 19.1 of BS 9000, devices produced concurrently through final seal by the same fabrication technique, using the same types of machine and apparatus and having the same device design but differing only electrically, may be grouped together for the purpose of obtaining samples for the tests detailed below.

Such device types should preferably be included on the same detail specification but in any case the claim for grouping shall be declared in the qualification approval test report. With this proviso, the grouped testing described in 1.1.8.1.1 to 1.1.8.1.4 may be used.

1.1.8.1.1 Electrical tests in Groups A and/or C and/or D (excluding endurance tests). Where devices which are made on the same production line and have the same device design and assembly techniques are selected into sub-lots of types having different characteristic limits, each sub-lot shall be sampled (with sample size appropriate to the size of the sub-lot) for those tests having different limits for the different types.

For those electrical tests in Groups A and/or C and/or D having common electrical characteristic limits and test conditions for all the types, the manufacturer may take either:

- 1) a single sample (of a size appropriate to the total lot size) comprising equal or proportionate quantities of all types to assess the lot, or
- 2) a single sample (of a size appropriate to the total lot size) comprising equal or proportionate quantities from each of the three types having high, medium and low values of the reference characteristic — to assess the lot, or
- 3) a single sample (of a size appropriate to the total lot size) of any one type to assess the lot if it can be demonstrated to the satisfaction of the supervising inspectorate that the characteristic(s) being tested are not significantly dependent on the selection.

NOTE The procedure for demonstrating the validity of method 3) to the supervising inspectorate is to carry out tests for the common electrical characteristic on a sample from each of the sub-lots, and show there is no significant difference in the distribution of these characteristics between the sub-lots, by the use of a statistical test, e.g. the “t” test.

The sample taken from each sub-lot shall be 50 unless a smaller number is agreed with the supervising inspectorate. This demonstration shall be carried out at the qualification approval stage and thereafter at Group D intervals unless otherwise agreed with the supervising inspectorate.

If there is a significant difference, the type selected for the common electrical characteristics shall be that which gives the greatest risk of failure.

1.1.8.1.2 *Environmental tests in Groups B, C and D.* For the following tests when specified:

Vibration swept frequency
Acceleration and shock

the results of a sample (with size appropriate to the total lot size) of any one type can be used to assess the lot containing other types made on the same production line and having the same device design and using the same assembly techniques.

1.1.8.1.3 *Endurance tests, excluding voltage reference or voltage regulator diodes.* For the following tests, when specified:

Electrical endurance test (Groups B, C and D)
Dry heat storage
Cold test for storage

the results of a sample (with size appropriate to the total lot size) of any one type can be used to assess the lot containing other types made on the same production line and having the same device design and using the same assembly techniques but of different rating (e.g. voltage, current or temperature) providing:

- 1) the type tested and lower rated types together comprise not less than 60 % of the total lot size, and
- 2) that the following additional tests shall be performed for the highest rated type with sample sizes appropriate to the average total lot size during the Group C or Group D period, as appropriate.

Endurance test for 160 hours, inspection level S-4 AQL 1.5 % Group C.

High temperature storage for 1 000 hours, inspection level I AQL 2.5 %, Group D.

Low temperature storage for 1 000 hours, inspection level S-4 AQL 4.0 %, Group D.

1.1.8.1.4 *Endurance tests for voltage reference and voltage regulator diodes.* For the following tests, when specified:

Electrical endurance test (Groups B, C and D)
Dry heat storage
Cold test for storage

the results of a sample (with size appropriate to the total lot size) of the majority type within each lot can be used to assess the lot containing other types made on the same production line and having the same device design and using the same assembly techniques but of different rating (e.g. voltage, current or temperature).

1.1.8.2 Devices having a common encapsulation and mounting method. Devices which, although they may differ electrically are manufactured using a common encapsulation and are intended for mounting by the same method may be grouped together for the purposes of obtaining samples for certain tests. (One example of devices within this category would be those encapsulated in an SO-3 style can with a special associated base.)

For the following tests (when specified):

- Visual examination
- Polarity inspection
- Dimensions
- Solderability or
- Weldability
- Rapid change of temperature and damp heat, cyclic
- Lead fatigue (or fixed lug torque)

the results of a sample (with size appropriate to the total lot size) of any one type of device can be used to assess the lot containing other types which are made using the same encapsulation and essentially similar assembly techniques.

1.1.9 Delayed delivery

Devices held in store for a period exceeding two years following the date code shall be re-examined for all Group A, subgroup 2 and Group B, subgroup 2a requirements prior to release.

1.1.10 Supplementary procedure for qualification approval

1.1.10.1 The procedure given in BS 9000 shall be applied except that for the purpose of qualification approval in Group D, an AQL of 6.5 % shall be applied for subgroup D1 and an AQL of 4.0 % shall be applied for subgroups D2 and D3 (see 2.2.4).

No AQL value is appropriate for subgroup D4.

1.1.10.2 For production lot sizes below 280 specimens, the following table supersedes the sample requirements of Clause 13 of BS 9000. The samples may be drawn from one production lot. When using the table, a second sample, as shown, shall be taken when the quantity of defective devices exceeds the acceptance quantity but is less than the reject quantity.

Group	Lot size	Sample size	Accept	Reject	Second sample	Total sample	Accept	Reject
A	1–7	100 % (see Note 1)	0	1				
	8–280	5	0	2	3	8	1	2
B	1–7	100 % (see Note 1)	0	1				
	8–280	5	0	2	3	8	1	2
C1 and C2	1–7	100 % (see Note 1)	0	1				
	8–280	5	1	2				
C3	1–7	2 (see Notes 1 and 3)	0	1				
	8–280	2	0	2	2	4	1	2
C4	1–7	2 (see Notes 1 and 3)	0	1				
	8–280	2	0	1				
C5	1–7	100 % (see Note 1)	0	1				
	8–280	5	0	2	3	8	1	2
D1 and D2	1–7	100 % (see Note 1)	0	1				
	8–280	5	0	2	3	8	1	2
D3 and D4	1–7	2 (see Note 3)	see Note 2					
	8–280	2	see Note 2					

NOTE 1 Qualification approval depends on at least two devices being tested for each subgroup.

NOTE 2 See 1.1.10.1.

NOTE 3 For ease of operation of this table, 100 % testing may be used for lot sizes of 1–7 devices.

1.1.11 Certified test records

The procedure given in Section 6 of BS 9000 and 2.3 of this standard shall be applied.

1.1.12 Standard ratings and characteristics

Preferred nominal values and limits of voltages for voltage reference diodes in a 5 % range are as given in the following table.

Lower limit	Nominal	Upper limit	Lower limit	Nominal	Upper limit
2.5	2.7	2.9	8.5	9.1	9.6
2.8	3.0	3.2	9.4	10.0	10.6
3.1	3.3	3.5	10.4	11.0	11.6
3.4	3.6	3.8	11.4	12.0	12.7
3.7	3.9	4.1	12.4	13.0	14.1
4.0	4.3	4.6	13.8	15.0	15.6
4.4	4.7	5.0	15.3	16.0	17.1
4.8	5.1	5.4	16.8	18.0	19.1
5.2	5.6	6.0	18.8	20.0	21.2
5.8	6.2	6.6	20.8	22.0	23.3
6.4	6.8	7.2	22.7	24.0	25.9
7.0	7.5	7.9	25.1	27.0	28.9
7.7	8.2	8.7			

The nominal and limit values in the above table (except the limits 2.5 V and 2.9 V), multiplied by 10, will be preferred nominal and limit values in the 5 % series for higher voltages.

1.1.13 Unchecked parameters

The supplementary data given in detail specifications, in accordance with the requirements of the appropriate rules document (BS 9301 *et seq.*), shall not be the subject of inspection.

1.1.14 Procedure to be followed in the event of failure at Group C or D inspection

- 1) Group C. The procedure given in 20.16 of BS 9000 shall be applied.
- 2) Group D. Normally, the "Rules for preparation of detail specifications" do not include in Group D, tests which are used for release purposes.

Where such tests are included in Group D of the detail specification for the purpose of acceptance testing, the procedure given in 20.16 of BS 9000 shall be applied (see 1.1.10.1 for AQL values).

1.1.15 Supplementary procedure for reduced inspection

1.1.15.1 General. Either of the two special reduced inspection procedures detailed in 1.1.15.2 or 1.1.15.3 may be applied to any of the subgroups of Group B which meet the required conditions.

1.1.15.2 Group B tests under Group C conditions. This special procedure allows a manufacturer to carry out the appropriate Group B tests at normal inspection under Group C conditions at intervals of 3 months instead of on a lot by lot basis.

It may be applied under the following conditions.

- 1) That the requirements for the change from normal to reduced inspection as given in 8.3.3 of BS 6001 have been met and in addition that the limit number given in Table VIII of BS 6001 is greater than zero.
- 2) That the small lots sampling procedures as given in 17.4.3 of BS 9000 are not in operation.
- 3) That there have been zero defect/defectives in the sample from ten successive lots submitted to Group B testing.

A single defect/defective in this Group C sample shall cause reversion to the Group B lot by lot inspection until such time as the conditions for special reduced inspection have again been satisfied. In the event of such a Group C failure, the Group B lot by lot inspection may continue under reduced inspection as defined in BS 6001 provided that the conditions given in 8.3.3 and Table VIII of BS 6001 are still satisfied, otherwise reversion to inspection as specified in Clause 8 of BS 6001 shall apply.

1.1.15.3 Group B tests under skip-lot conditions. This special procedure allows a manufacturer to carry out the appropriate Group B tests at normal inspection on every fourth lot, i.e. skipping three lots, instead of on a lot by lot basis.

It may be applied under the following conditions.

- 1) That ten successive lots have been accepted on normal inspection.
- 2) That the maximum time interval between tests shall not exceed 3 months.
- 3) That the lot size used for determining the test sample shall not be smaller than that which would have been used for any of the proceeding skipped lots.

Rejection of a lot under this procedure shall cause reversion to the Group B lot by lot inspection until such time as the conditions for reduced inspection have again been satisfied.

1.1.16 Supplementary procedure for general application category devices

For the purpose of this specification, the general application category as defined in Clause 5 of BS 9000 has been subdivided in 2.1 of this specification into two categories named “P” and “Q”.

Manufacturers may, at their discretion, supply devices which have met the P category specification requirements against orders for the corresponding Q category specification.

1.2 Test procedures

The test and measurement methods and procedures given in this section shall be applied when required by the detail specification and in accordance with the inspection requirements of BS 9000 and tests Ab and Ad of BS 2011-2.1A:1977 Test A.

1.2.1 Measurement conditions

Unless otherwise specified, all tests shall be carried out under standard atmospheric conditions for testing as specified in Clause 5 of BS 2011-1.1:1980 General.

1.2.2 Visual inspection

(NOTE In all those “rules for the preparation of detail specifications” published prior to January 1977, where a reference to “1.2.2 Visual inspection” is made in Group A, the reference should be understood to mean 1.2.2.1).

1.2.2.1 External inspection. Unless otherwise specified, external inspection shall be performed under normal factory lighting conditions and under normal visual conditions and shall include the following items.

- 1) Correctness of marking.
- 2) Correctness of terminal identification.
- 3) Correct encapsulation.
- 4) Unbroken body.

1.2.2.2 Pre-encapsulation visual inspection. The inspection shall be performed, before the device is encapsulated, on 100 % of the product. Inspection shall be performed at a minimum magnification of $30\times$ at a suitable angle from the perpendicular to the die surface with the device under suitable illumination. When a die has a side of less than 0.5 mm the magnification shall be not less than $50\times$ and the die shall be viewed perpendicularly to its surface with the device under illumination normal to the surface of the die. For the examination of surface detail of microwave devices a minimum magnification of $100\times$ shall be used.

1.2.2.2.1 Inspection for foreign material. Unattached foreign material shall be removed prior to inspection.

In the case of a die, foreign particles shall be considered to be attached when they cannot be removed by a jet of dry nitrogen at a pressure of 138 kN/m^2 (20 psi gauge) applied for a minimum of 3 s from a distance of 50 mm maximum.

Devices shall be rejected if attached opaque particles on the die appear to bridge:

- a) adjacent unpassivated metallizations;
- b) any unpassivated metallizations to the header, bond wire or unpassivated edge of the die.

In the case of a header, foreign particles shall be considered to be attached when they cannot be removed by nominal tweezer pressure.

Devices shall be rejected if attached particles appear to bridge the header to post, die or bond wire.

1.2.2.2.2 Inspection for header and can defects. Devices shall be rejected if the internal part of the header, including the posts, or the interior of the can exhibit damage, corrosion, contamination or flaked plating.

Devices shall be rejected if contamination exists on the glass seal internal or external to the package between the header and the terminal or if there is evidence of corrosion on any part of the package.

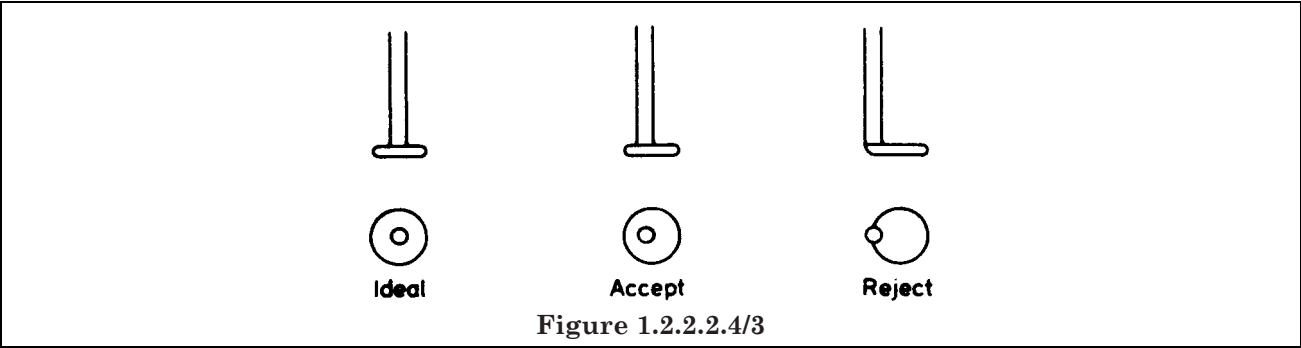
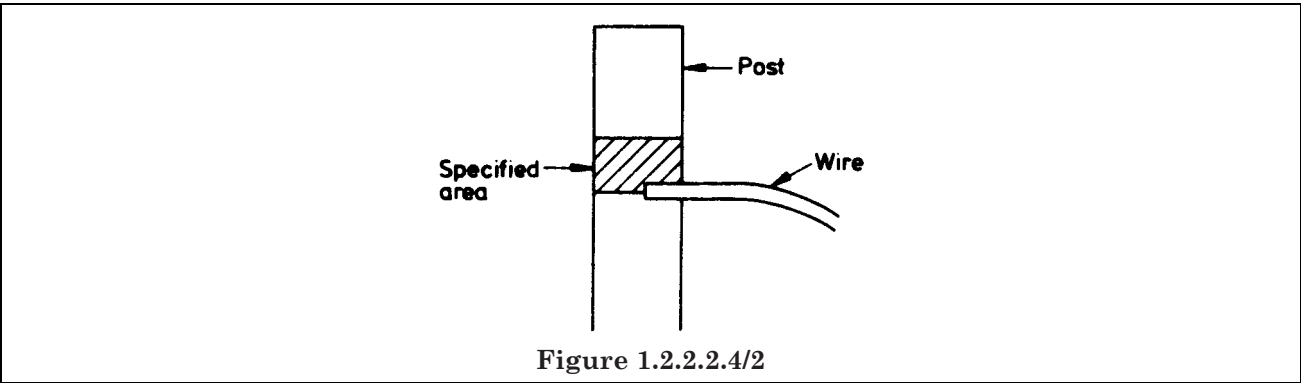
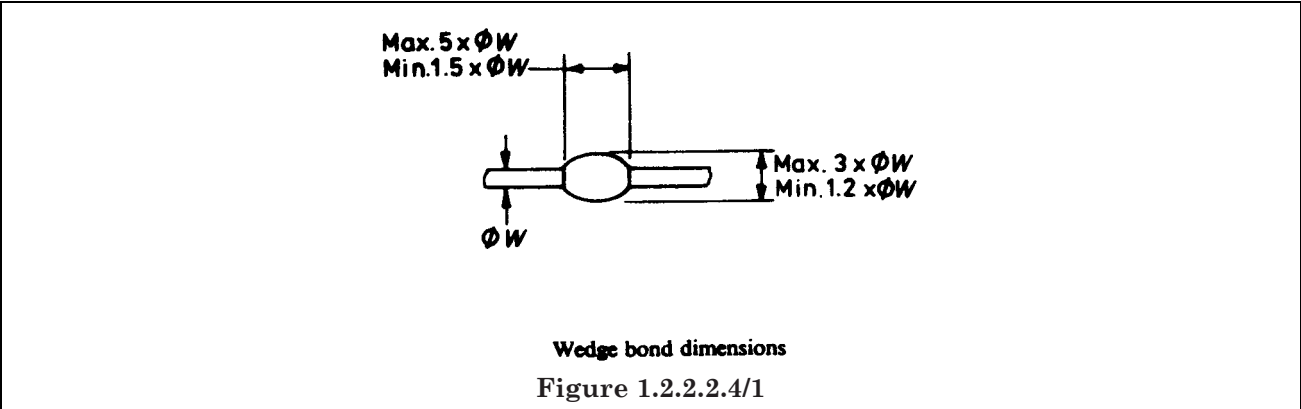
1.2.2.2.3 Inspection for die mounting. The device shall be rejected if it exhibits any of the following faults.

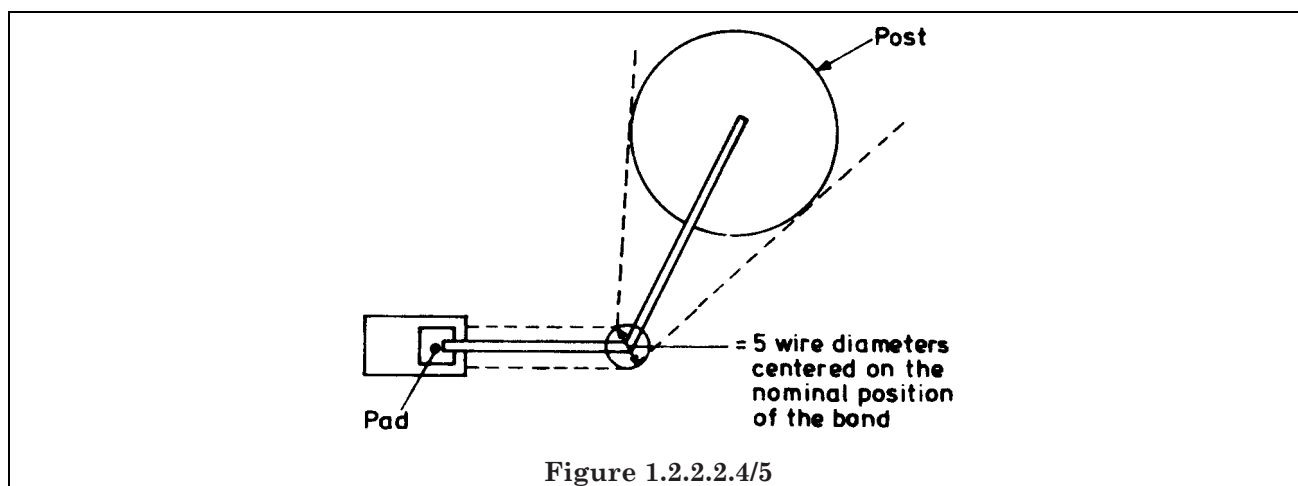
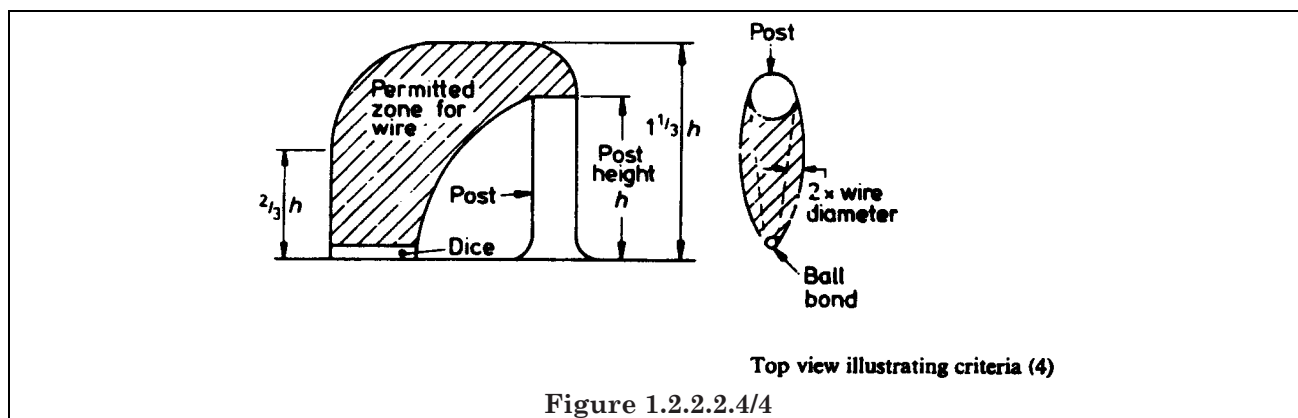
- a) The die geometry and dimensions do not correspond to the relevant assembly drawing.
- b) The die is misorientated by more than the amount permitted by the relevant assembly drawing.
- c) The die is not within the area indicated on the relevant assembly drawing.
- d) The die shows excessive skew or tilt with respect to the die bonding area as indicated on the relevant assembly drawing.
- e) Where mounted on top of a post, the die extends outside the area of the post.
- f) The die to header melt or epoxy mounting material is not visible around an estimated 75 % of the device periphery.
- g) The eutectic material on the glass-metal seal reduces the exposed glass surface distance from header to post by more than an estimated 25 %.
- h) Die mounting material build-up which touches the top surface of the device or extends vertically above it.

1.2.2.2.4 Inspection of bonds and internal lead wires. Devices shall be rejected if they exhibit any of the following faults.

- a) The bond configuration does not conform to the relevant assembly drawing.
- b) Nicks, cuts, crimps, scoring or thinning of the bonding wire (including those at the “heel” of a wedge bond) that reduce the specified wire diameter by more than an estimated 25 %.
- c) Less than an estimated 50 %, or in the case of microwave devices 75 %, of a bond wire covers the metallizing within the designed pad area.
- d) A ball bond with a diameter less than an estimated 2 and more than an estimated 5 wire diameters across or a wedge or other bond with a width less than an estimated 1.2 times or more than an estimated 3 times the wire diameter, or with a length less than an estimated 1.5 times or more than an estimated 5 times the wire diameter. (See Figure 1.2.2.2.4/1)
- e) Wire tails which extend over, or are capable of extending over or make contact with, any metallization not covered by passivation and not connected to the wire, or if wire tails exceed two wire diameters in length at the pad or four wire diameters in length at the post or 50 or 100 μm in length, whichever is the greater.
- f) Side welds have less than an estimated 50 % of the wire-post weld situated on the specified bonding area. (See Figure 1.2.2.2.4/2)
- g) The spacing of a bond from the edge of a post is less than an estimated 2 wire diameters or 50 μm , whichever is the least.
- h) There is no visible gap between the bonds.
- i) There is no visible gap between the bond and the adjacent metallization.
- j) Any ball bond where the location of the wire leaving the ball bond is not completely within the boundaries of the ball bond when viewed from above. (See Figure 1.2.2.2.4/3)
- k) A second bond is made on top of another in an attempt to repair the first.
- l) There is excessive loop or sag in any wire such that it is closer than 100 μm to another wire, the post, the die or any portion of the package. This does not apply to bonds attached to the same pad.
- m) The wire from a ball bond does not leave the die vertically without kinking or otherwise departing from a smooth line and does not begin to curve towards the post before reaching two-thirds of the post height. (See Figure 1.2.2.2.4/4)
- n) The wire from the ball bond on the die rises to more than one and one-third of the post height or 300 μm , whichever is the greater. The requirements of excessive loop or sag must still be met. (See Figure 1.2.2.2.4/4)

- o) The wire is taut between die and post.
- p) The wire is laterally displaced by more than two wire diameters outside the area bounded by the tangent planes common to die bond and post. (See Figure 1.2.2.2.4/4)
- q) The wire from a wedge bond leaves the bond plane vertically or otherwise than in a smooth curve.
- r) For preformed wire used where wedge bonds are formed simultaneously, the wire is not contained within the envelope defined by the tangents of the post edge to points two wire diameters from either side of the specified position of the formed bend and from the outer edges of the pad area to two points wire diameters from either side of the specified position of the formed bend. (See Figure 1.2.2.2.4/5.)





1.2.2.2.5 Inspection of bond strength. The bond strength shall be tested on a sampling basis with Inspection level S-2, AQL 2.5 %, these figures referring to the number of bonds to be tested.

The test shall be in accordance with 1.2.6.16 of BS 9300.

1.2.2.2.6 Inspection of scribing and die defects. Devices shall be rejected if they have cracks which touch the die edge at two points (i.e. an incomplete chip-out) unless the silicon bounded by the crack is removed and the resulting die satisfies the chip and crack criteria as follows.

- a) Devices having a guard ring and field relief electrode shall be rejected if:
 - 1) a chip-out reaches the inner oxide step formed by the guard ring diffusion, or
 - 2) a crack extends within the outer periphery of the guard ring diffusion.
- b) Devices having a guard ring only shall be rejected if:
 - 1) a chip-out reduces the guard ring annulus width by more than an estimated 50 %.
 - 2) a crack points towards or extends to the outer oxide step formed by the guard ring diffusion.
- c) Devices not possessing either a guard ring or a field relief electrode shall be rejected if:
 - 1) any crack exceeds an estimated 125 μm (0.005 in) in length or approaches closer than an estimated 5 μm (0.0002 in) to any active metallization, bonding pad or other active portion of the device;
 - 2) any crack penetrates the outer boundary of the oxide by more than an estimated length of 25 μm (0.001 in) and points towards the active metallization or circuit area;
 - 3) a chip-out extends to within an estimated 12 μm (0.0005 in) of a bonding pad or active portion of the device; or
 - 4) a die exhibits any crack or chip-out in the active circuit area.
- d) Microwave devices shall be rejected if:
 - 1) the chip-out extends to within an estimated 12 μm (0.0005 in) of a bonding pad;

2) any crack exceeds an estimated 125 μm (0.005 in) in length or approaches closer than an estimated 12 μm (0.0005 in) to any bonding pad, active metallization or other active portion of the device;

3) a die exhibits any crack or chip-out in the active circuit area.

e) Mesa construction and other power devices shall be rejected if chipped or cracked as shown in Figure 1.2.2.2.7.

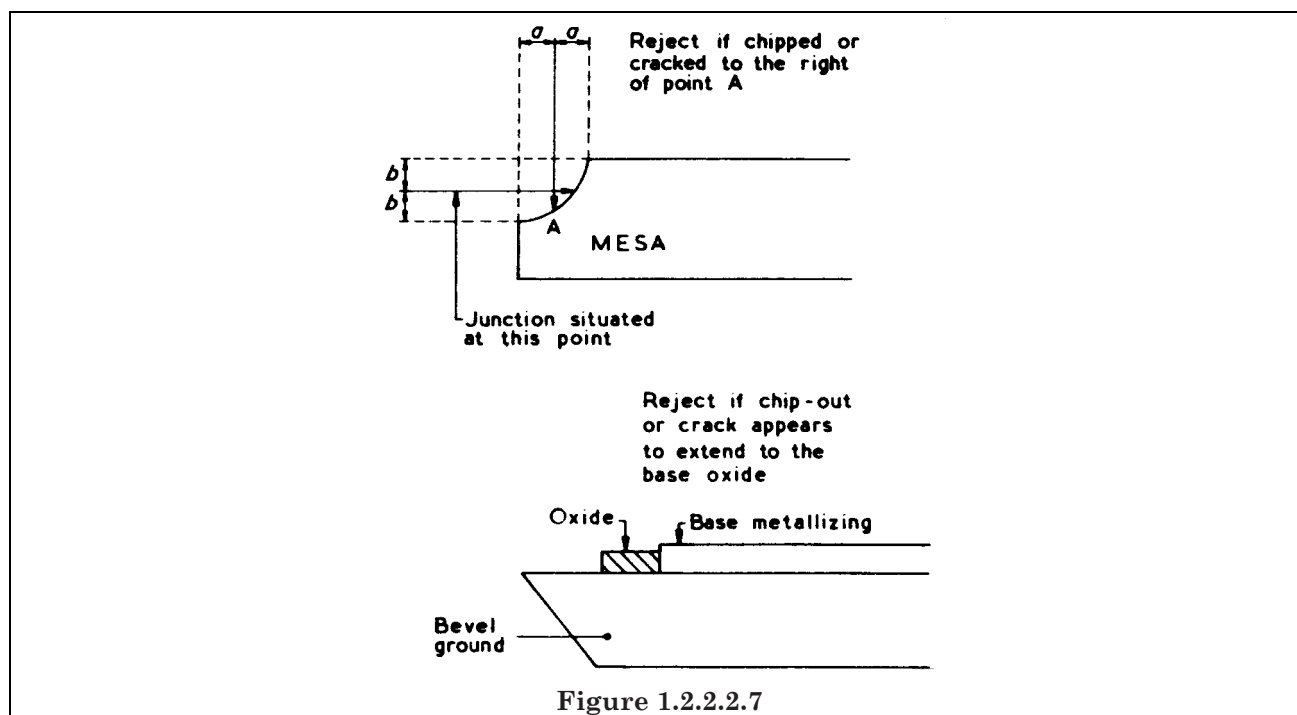


Figure 1.2.2.2.7

1.2.2.2.7 Inspection of metallization and photolithographic defects. Any tearing defect in the metallization that exposes the underlying material is defined as a scratch.

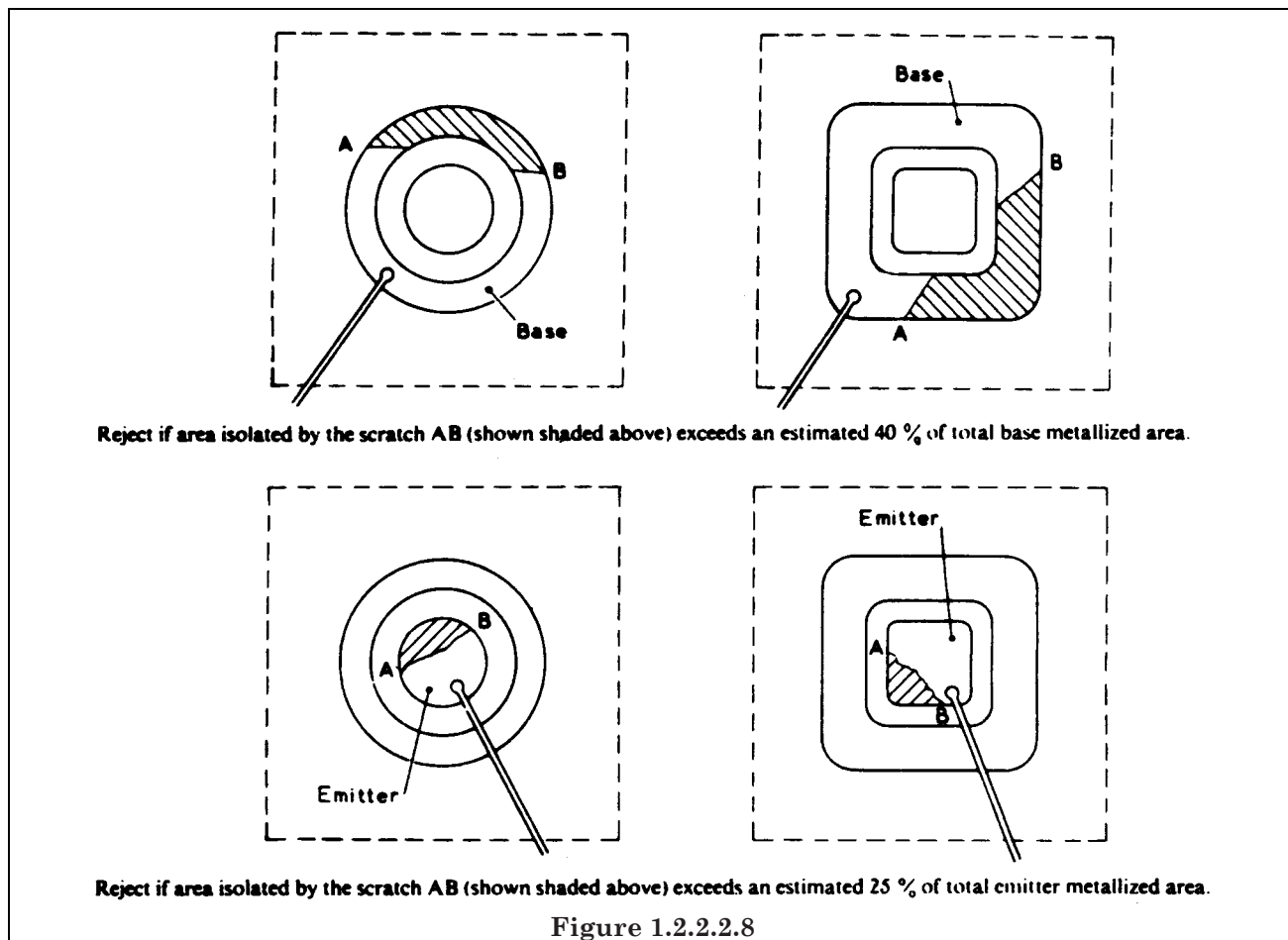
Devices shall be rejected if:

- metallization on a bonding pad does not cover more than 50 %, or, in the case of microwave devices, more than 80 % of the designed contact area;
- there is any evidence of metallization lifting, peeling or blistering;
- the oxide or alternative passivation is not visible between adjacent metallized areas;
- any active junction is not completely covered by oxide or alternative passivation;
- on non-interdigitated structures: a scratch isolates more than an estimated 25 % of the emitter and/or more than an estimated 40 % of the base metallized contact areas from the bond (see Figure 1.2.2.2.8);
- on interdigitated structures:
 - a scratch or photolithographic defect reduces the width of any metallizing “finger” by more than an estimated 50 % or, in the case of microwave devices, by more than an estimated 25 % or, in the case of a field-effect transistor gate, by more than an estimated 75 % of its original design width.
 - a scratch isolates more than an estimated 50 % or, in the case of microwave devices, 25 % of the bond area from the metallized interconnecting pattern;
 - the metallizing does not cover at least an estimated half or, in the case of microwave devices, three-quarters of the designed “finger” contact area.

1.2.2.2.8 Inspection of post protective coating. Devices that have been covered with silastic or other protective coating shall be rejected if:

- the device is not completely covered with protecting coating;
- there is evidence of bubbles or holes in the protective coating;

- c) there is evidence of coating on the can weld ring;
- d) the protective coating appears to be abnormal.



1.2.3 Dimensioning and gauging procedures

These tests shall be made in accordance with the specified drawing. The dimensions, which shall be checked as part of the Group B and C inspection requirements, are given in Table 1.2.3 or when appropriate in 1.2.3 of BS 9400 and are indicated by the standardized letter references in IEC publication 191-1 and BS 3934.

Table 1.2.3 — Inspections

Configuration of devices	Group B	Group C
1) Wire mounted double ended e.g. SO-6 (BSI) A1A (IEC) or e.g. SO-16 (BSI) A2 (IEC)	ϕD , G ϕD , A	All ^a All ^a
2) Wire mounted single ended e.g. SO-3 (BSI) C4 (IEC) with base SB3-3A (BSI) B4A (IEC)	ϕD , A	All ^a
3) Stud mounted lug ended e.g. SO-13 (BSI) A4U (IEC) or e.g. SO-28 (BSI) PA7 (IEC)	ϕD J	All ^a
4) Stud mounted flying lead e.g. SO-30A (BSI) A12U (IEC)	ϕD , O_2	All ^a
5) Flat base mounted e.g. SO-38 (BSI) or e.g. SO-5A (BSI) C14A (IEC) with base SB2-2 (BSI) B18 (IEC)	ϕD , O , ϕB U_1 , U_2 , Q , A	All ^a All ^a
6) Co-axial microwave e.g. SO-26 (BSI) A18 (IEC)	ϕD_1 , ϕD_2 , ϕB J , Q , A	All ^a

^a All dimensions included in the BS 3934 drawing called up in the detail specification or the drawing included in the detail specification prepared in accordance with BS 3934 except those already covered in Group B.

1.2.4 Electrical test procedures

1.2.4.1 General. This section gives information of a general nature applying to electrical measurement techniques and general precautions to be applied during measurements.

The measuring methods given in this standard are presented so as to prescribe their required principles of operation and therefore do not necessarily define detailed techniques for their practical application. Where tolerances associated with conditions of measurement are provided they shall be used as guidance for the maximum deviations from absolute circuit values that are permissible in practical measuring systems.

1.2.4.1.1 Alternative test methods. The measurement and conditions specified are not the only methods which can be used but the supervising inspector must be satisfied that other methods including pulse methods and/or conditions of measurements employed will give results compatible with the methods and/or conditions specified in this standard and the relevant detail specification. By “compatible” is meant that the value of the characteristic established by such other method will fall within the specified limits when measured by the specified method.

1.2.4.1.2 Polarity. The polarity of the sources shown in the subsequent circuits are applicable to p-n-p type transistors, to p-n-p-n type thyristors and to n-channel field-effect transistors. The circuits can be adapted for other polarity type devices by reversing the polarities of the appropriate sources and meters.

1.2.4.1.3 Ratings. The test conditions for all measurements should be such that the maximum ratings of the device are not exceeded.

Circuits shall include means of limiting maximum instantaneous currents and applied voltages, for example, by the addition of catching diodes where necessary. It is recommended that devices should not be inserted into or removed from a circuit while it is energized.

1.2.4.1.4 Equilibrium conditions. All electrical tests shall be conducted under equilibrium conditions unless otherwise specified or unless the measurement is being carried out under pulsed conditions. When test conditions cause significant change with time of the characteristic being measured, means of compensation for such effects will be specified; for example, the length of time that the device shall be maintained at test conditions before making a measurement.

1.2.4.1.5 Temperature. Unless otherwise specified, all measurements shall be made at an ambient or reference point temperature of 25 ± 2 °C. Measurements may be carried out at temperatures other than 25 °C provided the supervising inspector is satisfied that the device will be in accordance with all the provisions of the detail specification when tested at 25 °C.

When a low ambient temperature is specified, the method described in BS 2011-2.1A:1977 Tests Ab or Ad shall be used.

When a high ambient temperature is specified, the method described in BS 2011-2.1B:1977 Tests Bb or Bd shall be used.

When a high case or reference point temperature is specified, the device under test shall be mounted, by its normal fixing, to a copper or similar high conductivity metal block. The block shall have a mass of at least ten times that of the device under test and shall be maintained at the temperature as specified in the detail specification.

Sufficient time for the part to reach temperature equilibrium shall elapse before the measurements commence.

1.2.4.1.6 Meters. For any device carrying large currents, separate current carrying and voltage measuring contacts should be used. When this is not possible, corrections may have to be made to the measured values of interterminal voltages.

1.2.4.1.7 Measurement circuit requirements and precautions

1) *Open-circuit.* A circuit shall be considered open-circuited if a two-to-one decrease in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of measurement. The values of high resistances (whether of circuit components or meters) specified in the circuits, should be so high that a two-to-one decrease in their value will not affect the desired accuracy of the measurement.

2) *Short-circuit.* A circuit shall be considered short-circuited if a two-to-one increase in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. Capacitors used to couple or by-pass the test signal should present effective short-circuits at the test frequency. In certain of the high frequency measurements, where r.f. decoupling is important the necessary components and/or mounting conditions of the device shall be as specified.