

**Detail specification for
silicon voltage
regulator diodes —
400 mW, 2.7
to 33 V (5 %),
hermetically sealed,
glass encapsulation —
General application
category Q**

UDC 621.382.2:621.316.722

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, pages 1 to 9 and a back cover.

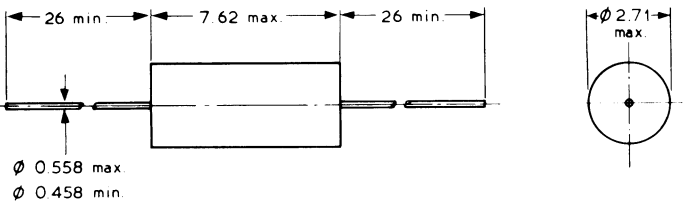
This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Amendments issued since publication

Amd. No.	Date	Comments

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Electrical Components of Assessed Quality: Detail Specification	
Outline and dimension (Third angle projection) All dimensions are in millimetres For detail dimensions see BS 3934 SO-6 	VOLTAGE REGULATOR DIODE
	GENERAL APPLICATION CATEGORY Q
	MANUFACTURER'S TYPE NUMBER AS SHOWN IN BS 9002
	400 mW, 2.7 TO 33 V (5 %) SILICON VOLTAGE REGULATOR DIODE HERMETICALLY SEALED GLASS ENCAPSULATION

1 Limiting conditions of use (not for inspection purposes)

Absolute maximum values

Power rating

P_{tot} Reverse power dissipation

400 mW

For derating curve of reverse power dissipation against T_{amb}

see Figure 1

Thermal ratings

T_{amb} Operating temperature range

– 55 °C to 150 °C

T_{stg} Storage temperature range

– 55 °C to 150 °C

2 Characteristics (not for inspection purposes) (at 25 °C unless otherwise stated)

V_{Z1} Working voltage at

see Table 1, cols. 1, 2, 3

I_{Z1} as Table 1, col. 4

V_{Z2} Minimum working voltage at

see Table 1, col. 13

I_{Z2} as Table 1, col. 11

I_{R5} Maximum reverse current at

see Table 1, col. 9

V_R as Table 1 col. 8

I_{R6} Maximum reverse current at $T_{\text{amb}} = 100$ °C and

see Table 1, col. 10

V_R as Table 1, col. 8

r_{Z1} Maximum differential resistance at

see Table 1, col. 5

I_{Z1} as Table 1, col. 4

r_{Z2} Maximum differential resistance at

see Table 1, col. 12

I_{Z2} as Table 1, col. 11

S_Z Temperature coefficient of V_{Z1}
over temperature range $T_{\text{amb}} = 25$ °C
to $T_{\text{amb}} = 60$ °C and at I_{Z1} as Table 1, col. 4

see Table 1, cols. 6, 7