

**Detail specification for
low power silicon n-p-n
switching
transistors — 20 V,
planar epitaxial,
ambient rated,
hermetic
encapsulation — Full
plus additional
assessment level**

UDC 621.316.5:621.318.57.621.382.3

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, pages 1 to 6 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Amendments issued since publication

Amd. No.	Date of issue	Comments
3317	October 1980	Indicated by a sideline in the margin

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