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Specification for

**Integrated electronic
circuits and
micro-assemblies of
assessed quality
(capability approval
procedures): generic
data and methods of
test**

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Contents

	Page
Co-operating organizations	Inside front cover
0 Introduction	1
Section 1. Principles and mandatory requirements	
1.1 General matters	5
1.1.1 Scope	5
1.1.2 Related documents	5
1.1.3 Terminology	5
1.1.3.1 General terms	5
1.1.3.2 Integrated circuits and their functions	8
1.1.3.3 General descriptive terms	8
1.1.3.4 Terms for the characteristics of digital circuits	9
1.1.3.5 Terms for the characteristics of analogue circuits	10
1.1.4 Letter symbols, signs and abbreviations	12
1.1.4.1 Digital circuits	12
1.1.5 Graphical symbols	13
1.1.6 Marking of the component and package	13
1.1.6.1 Terminal identification	13
1.1.6.2 Customer's type number (or colour code)	13
1.1.6.3 Factory identification code or manufacturer's name or trade mark	13
1.1.6.4 Date code	13
1.1.6.5 <i>Text deleted</i>	
1.1.6.6 Detail specification number	13
1.1.6.7 Colour code identification for type number	13
1.1.6.8 Tolerance identification	13
1.1.7 Eligibility for release	14
1.1.7.1 Film and hybrid integrated circuits, micro-assemblies, micro-modules and microwave integrated circuits	14
1.1.7.2 Monolithic and multichip semiconductor circuits	14
1.1.7.3 Use of non-approved sub-contractors	14
1.1.8 Structural similarity	15
1.1.9 Delayed delivery	15
1.1.10 Supplementary procedure for qualification approval	15
1.1.11 Certified test records	15
1.1.12 Standard ratings and characteristics	15
1.1.12.1 Supply terminal voltages	15
1.1.12.2 Test temperatures	15
1.1.12.3 Preferred temperature ranges	15
1.1.13 Unchecked parameters	15
1.1.14 Procedure to be followed in the event of failure at groups C and D inspection	15
1.1.15 Ordering information	16
1.1.16 Release prior to completion of group B tests	16
1.1.17 Supplementary procedure for reduced inspection	16
1.1.18 Supplementary procedure for general application category components	16
1.1.19 Rework	16
1.1.20 Sampling procedures	16

	Page
1.2 Test procedures	17
1.2.1 Standard conditions for testing	17
1.2.1.1 General	17
1.2.1.2 Safety aspects	17
1.2.1.3 Drying	18
1.2.2 External visual inspection	18
1.2.3 Dimensioning and gauging procedures	19
1.2.4 Electrical test procedures	19
1.2.4.1 General	19
1.2.4.2 Measurement methods	20
1.2.5 Mechanical test procedures	21
1.2.5.1 Direction of acceleration/force	21
1.2.6 Environmental test procedures	21
1.2.6.1 Cold	21
1.2.6.2 Dry heat	21
1.2.6.3 High temperature storage	21
1.2.6.4 Damp heat, steady state	22
1.2.6.5 Damp heat, cyclic	22
1.2.6.6 Shock	23
1.2.6.7 Bump	23
1.2.6.8 Vibration (sinusoidal)	24
1.2.6.8.1 <i>Text deleted</i>	
1.2.6.8.2 <i>Text deleted</i>	
1.2.6.9 Acceleration	24
1.2.6.10 Mould growth	25
1.2.6.11 Corrosion	25
1.2.6.12 Low air pressure	25
1.2.6.13 Rapid change of temperature	25
1.2.6.14 Sealing	27
1.2.6.14.1 Fine leak detection	27
1.2.6.14.2 Gross leak detection	29
1.2.6.14.3 <i>Text deleted</i>	
1.2.6.14.4 <i>Text deleted</i>	
1.2.6.15 Soldering	30
1.2.6.15.1 Solderability	31
1.2.6.15.2 Resistance to solder heat	31
1.2.6.15.3 De-wetting	31
1.2.6.15.4 Ageing	32
1.2.6.16 Robustness of terminations	32
1.2.6.16.1 Tensile test	32
1.2.6.16.2 Bending test	32
1.2.6.16.3 Bending (row of terminations)	32
1.2.6.16.4 Push test	32
1.2.6.16.5 Torque	33
1.2.6.17 Flammability	33
1.2.6.17.1 Internal	33
1.2.6.17.2 External	33
1.2.6.17.3 <i>Text deleted</i>	

	Page
1.2.6.18 Immersion in cleaning solvents	34
1.2.6.18.1 Resistance to contaminating fluids	34
1.2.6.19 Rapid change of temperature, two-bath method	34
1.2.6.20 <i>Text deleted</i>	
1.2.6.21 Damp heat steady state with bias	34
1.2.6.22 Thermal intermittance test	36
1.2.7 Electrical endurance test procedures	37
1.2.7.1 General	37
1.2.7.2 Test conditions	37
1.2.7.2.1 Steady-state, reverse bias	37
1.2.7.2.2 Steady-state, power	38
1.2.7.2.3 Power and reverse bias	38
1.2.7.2.4 Parallel excitation	38
1.2.7.2.5 Ring oscillator	38
1.2.7.2.6 Sequential HIGH-LOW state operation	39
1.2.7.3 Specified conditions	39
1.2.8 Accelerated test procedures	39
1.2.8.1 Thermally accelerated test for thick film resistive elements and associated conductors	39
1.2.8.2 Damp heat accelerated test for long term changes in resistance and interconductor leakage	40
1.2.9 Screening test procedures	41
1.2.9.0 Introduction	41
1.2.9.1 Screening requirements	41
1.2.9.1.1 General	41
1.2.9.1.2 Screening test and inspection	41
1.2.9.1.3 Detail specification inspection requirements	42
1.2.9.2 Burn-in screen	42
1.2.9.2.1 Specified conditions	43
1.2.9.2.2 Accelerated burn-in	43
1.2.10 Internal visual inspection	43
1.2.10.0 Introduction	43
1.2.10.1 Pre-assembly inspection	45
1.2.10.1.1 Hybrid and passive film circuits	45
1.2.10.1.2 Semiconductor dice	54
1.2.10.2 Post-assembly inspection	54
1.2.10.2.1 Mounting of substrate	54
1.2.10.2.2 Mounting of added components	55
1.2.10.2.3 Wire bonding	61
1.2.10.2.4 Internal lead wires	64
1.2.10.2.5 Package conditions	64
1.2.10.2.6 Controlled environment	65
1.2.11 Measurement of conductor adhesion to substrate	65
1.2.11.1 Pull test	65
1.2.11.2 Peel test	65
1.3 Capability approval and maintenance procedures	66
1.3.1 Capability assessment	66
1.3.2 Description of capability: Capability manual	70

		Page
1.3.3	Programme for initial capability approval and extensions	71
1.3.4	Performance of capability approval programme	76
1.3.5	Abstract of description of capability	76
1.3.6	Maintenance of capability approval	76
1.3.6.1	Small production lots	77
1.3.6.2	Capability qualifying circuits	77
1.3.6.3	Inspection requirements for maintenance of capability	77
1.3.7	Capability approval report	78
1.3.8	Review, suspension and withdrawal of capability approval	78
1.3.8.1	Review of approval	78
<i>Text deleted</i>		
1.4	Inspection to the customers's detail specification	78
Section 2. Guidance on the preparation of customers' detail specifications		
2.1	Basic information	79
2.1.1	Originator of the detail specification	79
2.1.2	Numbering of the detail specification	79
2.1.3	Description of the circuit and its intended application	80
2.1.4	Outline drawing and dimensions	80
2.1.5	Limiting conditions of use (ratings)	80
2.1.6	Required conditions of use and associated characteristics	80
2.1.7	Related documents	81
2.1.8	Additional information	81
2.1.9	Ordering instructions	81
2.2	Quality conformance inspection requirements	81
2.2.1	Screening requirements	81
2.2.2	Post-sealing test requirements	81
2.2.3	Electrical endurance tests	81
2.2.4	Electrical performance tests	82
2.2.5	Environmental tests	82
2.3	Certified test records	82
2.4	Authentication	82
Section 3. Manufacturer's guidance to customers		
3.1	Introduction	83
3.2	Circuit technology	83
3.3	Materials, construction and packages	83
3.4	Policy and information on design data and layout rules	84
3.4.1	Circuit elements	84
3.4.1.1	Resistors	84
3.4.1.2	Capacitors	85
3.4.1.3	Diodes	85
3.4.1.4	Transistors	85
3.4.2	Substrates for film circuits	87
3.4.3	Interconnection tracks and bonding pads	87
3.4.4	Circuit layout	87
3.4.5	Art work	88
3.4.6	Mask and screen preparation	88
3.4.7	Substrate preparation	88
3.5	Quality conformance inspection schedules	89

	Page
3.5.1 Pre-assembly inspection	89
3.5.2 Post-assembly inspection	89
3.5.3 Post-sealing inspection (environmental)	89
3.5.4 Electrical endurance inspection	89
3.5.5 Electrical performance inspection	89
3.6 Screening options	89
3.7 Add-on components	89
3.8 Capability qualifying circuits	89
3.9 Guidance on the ratings and characteristics which the customer should specify	90
Appendix A Guide to the writing of a customer's detail specification for a hybrid circuit	91
Figure 1 — Scheme for custom-built integrated circuits	2
Figure 2 — Event sequence for custom-built integrated circuits	4
Figure 1.2.6.22/1	37
Figure 1.2.7.2/1 — Steady state	38
Figure 1.2.7.2/2 — Parallel excitation	38
Figure 1.2.7.2/3 — Ring oscillator	39
Figure 1.2.10.1/1 — Scratch criteria	46
Figure 1.2.10.1/2 — Scratch criteria: composite metallization conductors only	47
Figure 1.2.10.1/3 — Void criteria	48
Figure 1.2.10.1/4 — Bonding pad areas	50
Figure 1.2.10.1/5 — Thin film resistor contact area	52
Figure 1.2.10.1/6 — Trimming requirements for thin and thick film resistors	53
Figure 1.2.10.1/7 — Trimming requirements for thin and thick film resistors (serpentine trim)	53
Figure 1.2.10.2/1	56
Figure 1.2.10.2/2	57
Figure 1.2.10.2/3	57
Figure 1.2.10.2/4	57
Figure 1.2.10.2/5	58
Figure 1.2.10.2/6	59
Figure 1.2.10.2/7	59
Figure 1.2.10.2/8	59
Figure 1.2.10.2/9	60
Figure 1.2.10.2/10	60
Figure 1.2.10.2/11	60
Figure 1.2.10.2/12 — Tailless or crescent bonds	63
Figure 1.2.11/1 — Conductor adhesion to substrate: peel test	66
Figure 1.3.2/1 — Skeleton flow chart	72
Table 1 — Colour code for identification number	14
Table 1.2.9/1 — Screening levels, test and inspection	42
Table 1.3.1/1 — Minimum test schedules	68
Table 1.3.1/2 — Sampling plans (category A)	69
Table 1.3.1/3 — Sampling plans (category B)	69
Table 1.3.3/1 — Blank CQC specification	73
Table 1.3.3/1 — CQC inspection requirements	74
Table 1.3.6/1 — Sampling requirements for small production lots	77

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to vi, pages 1 to 95 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

0 Introduction

This British Standard is the generic specification for capability approved integrated circuits in the system of standards for electronic components of assessed quality. It calls for the use of substances and/or test procedures that may be injurious to health if adequate precautions are not taken. It refers only to technical suitability and in no way absolves either the supplier or the user from statutory obligations relating to health, safety and fire hazards at any stage of manufacture or use. It follows a somewhat different pattern from other standards in the BS 9000 series since, owing to the wide diversity of customer requirements in terms of circuit functions, complexity and numbers of circuits of any one type to be supplied, the classical BS 9000 approach to detail specifications and qualification approval procedures for each type of circuit is no longer always practical.

The procedures for the procurement of integrated circuits of standardized specification within the BS 9000 system are contained in BS 9400, which specifies a system for the release of approved circuits to detail specifications written in accordance with the requirements of Part 2 of that document and the appropriate rules document in the series BS 9401 et seq. Qualification approval of each type of circuit for each manufacturer is obtained by demonstration of the conformity of the product to the detail specification and such approvals are published in PD 9002.

Very many of the processes in the manufacture of integrated circuits on a particular production line are common, although the resulting circuits may have widely differing electrical functions and characteristics. Many of the on-line quality control inspections for these common processes use standard test procedures such as those specified in the groups B, C and D inspection tables of detail specifications prepared in accordance with the requirements of BS 9000-1. Thus, provided that the customer can be assured that these inspections are being applied to declared common processes, it is no longer necessary to specify nor repeat them for each individual type of integrated circuit.

In this British Standard, the concept of qualification approval of each type of circuit is replaced by the concept of the “capability approval” of a manufacturer, i.e. the demonstration of the ability of a manufacturer to supply circuits of assessed quality in accordance with approved design rules, manufacturing processes and quality control procedures. Essentially, “capability approval” is analogous to a manufacturer receiving qualification approval for a series of several structurally similar components.

The required capability approval procedures are given in subsection 1.3 of this standard. They require an approved capability manual to be prepared by each manufacturer for each technology offered. Guides recommending the minimum contents of a capability manual for each different technology will be made available by the National Supervising Inspectorate (NSI).

This standard may be used in place of BS 9400 whenever its use is mutually agreed between manufacturer and customer (e.g. when only relatively small numbers of circuits are involved). However, catalogue items may also be released under BS 9450 capability approval procedures (see 15.11 of BS 9000-1).

Figure 1 shows a representation of the salient features of the BS 9000 system as adapted and extended to cover the situation where the customer is the initial activator in the requirements for integrated circuits which he requires for his equipment or system applications. This modified system starts with the same basic requirements as stated in BS 9000-1 for the initial approval of the manufacturer but in place of qualification approval the manufacturer obtains capability approval. For capability approval as indicated in Figure 1 full use is made of the on-line certification and approval of common processes such as those covered by groups B, C and D inspection so that any products made under such disciplines do not require further assessment of these features. The assessment of circuits produced for customer requirements then resolve into the quality conformance inspection of the electrical characteristics and performance, such as those covered by group A inspection.

The group A inspections which are specific to type must be dependent on customer requirements and he has the initial responsibility for specifying them in terms of their electrical functions and characteristics. In addition, he has the responsibility for specifying the environmental and other inspections with inspection levels and post-test end-point requirements which are necessary for his particular application.

Figure 1 shows a more detailed breakdown of the various sections of this specification and the various stages in the approval of the manufacturer’s capability and the guidance to be given to customers in the preparation of their detail specifications.

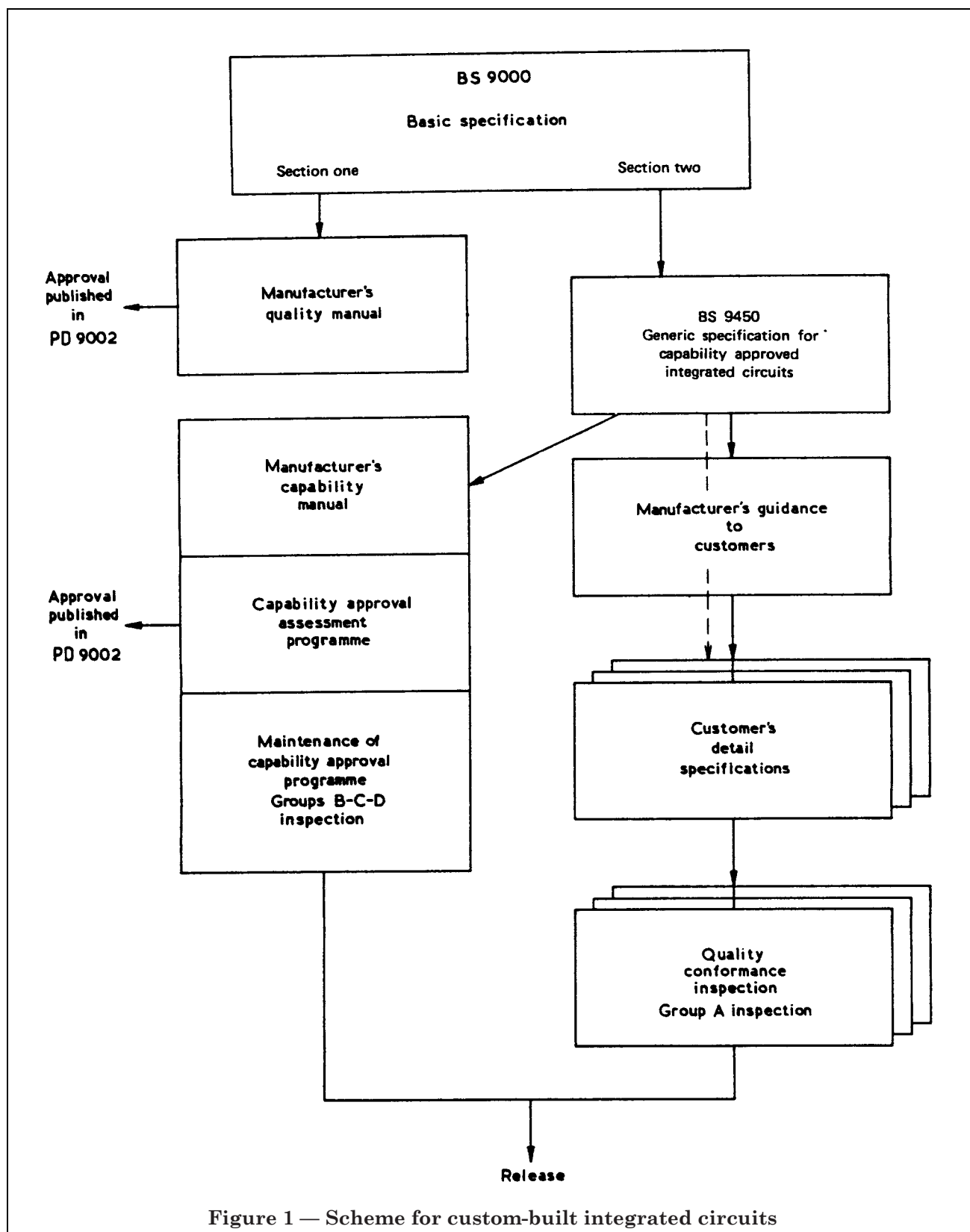


Figure 1 — Scheme for custom-built integrated circuits

Figure 2 shows the event sequence for the procurement and release of custom-built integrated circuits and the degree of involvement of BSI, the manufacturer, the supervising inspectorate and the customer.

A brief summary of the principal sections, subsections and clauses of this standard dealing with custom-built integrated circuits is as follows:

Section 1. Principles and mandatory requirements

1.1 General matters. Taken from BS 9400 with additions.

1.2 Test procedures. Referenced from BS 9400 with additions.

These are in conformity with BS 9400, but amended or extended to cover the requirements of capability approval, particularly for the film and hybrid technologies.

1.3 Capability approval and maintenance procedures

This subsection is additional to the principles given in BS 9000-1 and is in accordance with the general principles of section 3 of BS 9000-1. The additional information is given in the following clauses of this standard:

1.3.1 Capability assessment

1.3.2 Description of capability: Capability manual

1.3.3 Programme for initial capability approval and extensions

1.3.4 Performance of capability approval programme

1.3.5 Abstract of description of capability

1.3.6 Maintenance of capability approval

1.3.7 Capability approval report

1.3.8 Review, suspension and withdrawal of capability approval

1.4 Inspection to the customer's detail specification

Section 2. Guidance on the preparation of customers' detail specifications

This follows the same principles as those given in BS 9400 but modified to reflect the customers' initiation of specifications.

Section 3. Manufacturer's guidance to customers

This section is additional to the principles given in BS 9000-1 and states the minimum requirements necessary for the guidance of customers in the preparation of their enquiries and the preparation of their specifications. Although these requirements are not mandatory, it is essential that the data included by the manufacturer shall conform with the specifications and other information contained in his approved capability manual.

This guidance will inform the customer of the range of technologies, circuit design rules, methods of connection and packaging, inspection facilities etc., which a manufacturer is able to offer, in order to assist a customer to assess the suitability of a particular capability to a particular application requirement.

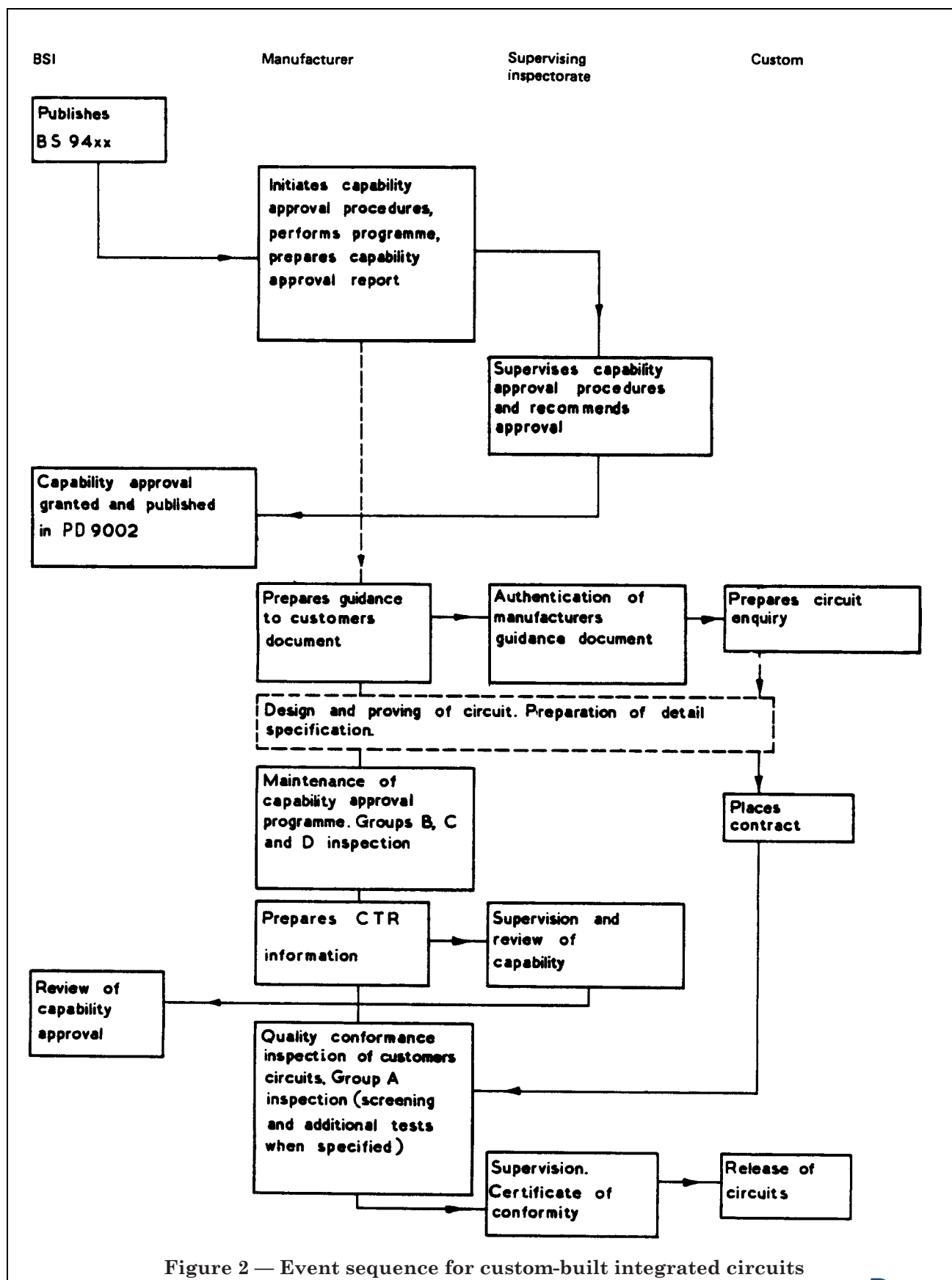


Figure 2 — Event sequence for custom-built integrated circuits

Section 1. Principles and mandatory requirements

1.1 General matters

1.1.1 Scope

This standard forms part of the BS 9000 series and should be read in conjunction with BS 9400 and with those standards referenced therein.

It specifies the approval procedure for integrated circuits as defined in **1.1.3** which are specifically ordered, designed, produced, tested and supplied to customer procurement requirements under the disciplines declared within the manufacturer's capability approval. In addition to the terms, definitions, symbols, test methods and other material already published in BS 9400 it gives supplementary information and requirements necessary to implement fully such detail specifications and procurement documents when prepared by customers within this system.

The requirements of this standard diverge from those of BS 9000 in that best use is made of on-line qualification of common processes and procedures of inspection of structurally similar features so that no further qualification approval of individual types of integrated circuits is necessary.

The manufacturer is required to declare to the supervising inspectorate his technology and the extent of his product capability and the means of assessing his ability to meet his declared capability both initially and on a continuous basis.

Schedules of standard tests and inspections are given herein to be selected and declared by the manufacturer as appropriate for his technology and range of products.

This standard also includes, in section 2 and section 3, two guidance documents, namely:

- a. General guidance to the customer on the preparation of detail specifications.
- b. Guidance to the manufacturer on the preparation of his guidance to the customer for the preparation of detail specifications.

In accordance with **6.5** of BS 9000-1, where any omissions, conflicts, ambiguities or inconsistencies occur, documents shall rank in the following order of authority:

- 1) The agreed customer/manufacturer detail specification prepared in accordance with section 2.
- 2) This standard.
- 3) BS 9400 and other applicable generic specifications, e.g. BS 9300 etc.
- 4) BS 9000 and other standards to which reference is made.

1.1.2 Related documents

The following standards, additional to those already given in BS 9400, are referred to in the text of this document.

(To be compiled as and when required).

1.1.3 Terminology

For the purposes of this British Standard, the following terms and definitions, together with those given in **1.2.10.0.2**, apply. Additional terms may be found in BS 204, BS 9300 and in BS 9400.

1.1.3.1 General terms

1.1.3.1.1

microelectronics

the concept of the construction and use of highly miniaturized electronic circuits

1.1.3.1.2

microcircuit

a microelectronic device having a high equivalent circuit-element and/or component density, which is considered as a single unit

NOTE A microcircuit may be a micro-assembly or an integrated (micro) circuit.

1.1.3.1.3

integrated (micro) circuit

a microcircuit in which a number of circuit elements are inseparably associated and electrically interconnected such that for the purposes of specification and testing and commerce and maintenance, it is considered indivisible

NOTE 1 For this definition, a circuit element does not have an envelope nor external connection and is neither specified nor sold as a separate item.

NOTE 2 Where no misunderstanding is possible, the term integrated microcircuit may be abbreviated to integrated circuit and will be so used throughout this standard.

NOTE 3 Further qualifying terms may be used to describe the technique used in the manufacture of a specific integrated circuit.

Examples of the use of qualifying terms:

Semiconductor monolithic integrated circuit (see 1.1.3.1.8)

Thick film integrated circuit (see 1.1.3.1.10)

Semiconductor multi-chip integrated circuit (see 1.1.3.1.13)

Film hybrid integrated circuit (see 1.1.3.1.20)

Thin film integrated circuit (see 1.1.3.1.9)

1.1.3.1.4

micro-assembly

a microcircuit consisting of various components and/or integrated circuits which are constructed separately and which can be tested before being assembled and packaged

NOTE 1 For this definition a component has external connections and possibly an envelope as well and can be specified and sold as a separate item.

NOTE 2 Further qualifying terms may be used to describe the form of the components and/or the assembly technique used in the construction of the specified micro-assembly. Examples of the use of the qualifying terms:

Semiconductor multi-chip micro-assembly.

Discrete component micro-assembly.

1.1.3.1.5

custom-built integrated circuits

integrated micro-circuits and micro-assemblies (as defined in 1.1.3.1.3 and 1.1.3.1.4) and micro-modules (as defined in 1.1.3.1.6) which are produced to customer requirements and which are designed, manufactured, tested and released in accordance with the procedures given in this standard

1.1.3.1.6

micro-module

a micro-circuit in which a number of components and/or integrated circuits are inseparably associated and electrically interconnected such that for the purposes of specification and testing and commerce and maintenance, it is considered indivisible

NOTE Where no misunderstanding is possible the prefix “micro” may be omitted from microcircuit, integrated microcircuit, micro-assembly and micro-module and has in general been so omitted throughout this standard.

1.1.3.1.7

capability qualifying circuits (or components). (CQCs)

circuits (or components) which are used for the demonstration of capability and the subsequent maintenance of capability in accordance with 1.3 of this specification

NOTE It will normally be necessary to use a range of CQCs to cover any one capability approval.

1.1.3.1.8

monolithic

a qualifying term for the technology of devices made out of a single piece of material

1.1.3.1.9

thin-film

a qualifying term for the technology wherein circuit elements are formed by vacuum deposition, e.g. by evaporation, sublimation, sputtering or by related techniques

1.1.3.1.10

thick-film

a qualifying term for the technology wherein circuit elements are formed by screen printing or by other related techniques

1.1.3.1.11

die

a unit of monolithic semiconductor material containing an active device or circuit

1.1.3.1.12

chip

an unencapsulated circuit or circuit element. (Alternative name for “die”)

1.1.3.1.13**multi-chip**

a qualifying term for the technology wherein an integrated circuit is realized by the use of two or more active or passive chips mounted on a substrate

1.1.3.1.14**flip-chip**

a qualifying term for chips or dice which can be mounted face downwards on a conductor pattern

1.1.3.1.15**beam-lead**

a qualifying term for chips or dice having extended integral solid terminations which can be directly bonded to a substrate or header without the need for intermediary wires

1.1.3.1.16**passive substrate**

a substrate without active elements whose functions are predominantly mechanical and thermal. It can be constructed from insulating, conductive or semi-conductive material

1.1.3.1.17**active substrate**

a substrate with active elements and, in some cases, passive elements. It may be used to support other externally deposited or connected elements

1.1.3.1.18**integral substrate package**

a package wherein the substrate forms an integral part of the package

1.1.3.1.19**included substrate package**

a package wherein the substrate is mounted within the package and is connected to the terminations

1.1.3.1.20**film hybrid**

a qualifying term for an integrated structure in which a circuit is formed by combination of one or more substrate technologies, with or without integral component elements, or by the combination of any one of these with discrete components

1.1.3.1.21**carrier**

a structure in which an incomplete integrated circuit or part of a circuit may be retained for ease of transportation, assembly and/or testing

1.1.3.1.22**passive element**

an element primarily contributing resistance, capacitance or inductance or a combination of these to a circuit function. Passive elements may be realised on or in passive or active substrates. Examples are resistors, capacitors, inductors, filters

1.1.3.1.23**active element**

an element primarily contributing electrical rectification or gain to a circuit function. Active elements may also be used to contribute resistance and capacitance to a circuit function, or to convert externally applied energy from one form to another

examples are diodes, transistors, semiconductor integrated circuits, light-sensing and light-emitting semiconductor devices

1.1.3.1.24**surface acoustic wave device (SAW)**

a device employing acoustic waves localized close to the surface of a piezo-electric substrate

1.1.3.2 Terms related to integrated circuits and their functions

1.1.3.2.1

digital circuit

a circuit which operates with digital signals at the input(s) and output(s) and which is characterized by the inter-relationships between the states of the digital signals at the input and output terminals.

See also 1.1.3.3.1

1.1.3.2.2

analogue integrated circuit

a circuit for which a continuous relationship (either linear or non-linear) exists between its input and output signals

1.1.3.2.3

attenuator

a network designated for insertion in a line, or between other networks, to introduce a loss without introducing distortion and normally without introducing impedance change

1.1.3.2.4

amplifier

a device in which an input signal controls a local source of power in such a way as to produce an output which bears some desired relationship to and is generally greater than, the input signal

1.1.3.2.5

differential amplifier

an amplifier whose output signal(s) correspond(s) to the instantaneous algebraic difference between two input signals

1.1.3.2.6

summing amplifier

an amplifier whose output signal(s) correspond(s) to the instantaneous algebraic sum of two or more input signals

1.1.3.2.7

filter

a circuit which delivers an output signal having a determined frequency-dependent relationship to the input signal

1.1.3.2.8

modulator

a circuit which delivers an output signal in which some characteristics of one input signal have been impressed upon some characteristics of another input signal

1.1.3.2.9

demodulator

a circuit which performs a function inverse to that of a modulator

1.1.3.2.10

delay network

a line or network specifically designed to introduce a desired delay in the transmission of a signal

1.1.3.2.11

frequency multiplier/divider

a circuit which delivers an output signal, the frequencies of which have determined integral multiple or submultiples of those of the input signal

1.1.3.3 General descriptive terms

1.1.3.3.1

digital signal

a physical quantity which may take one of a given number of discrete values (states)

NOTE In practice each discrete value falls within a range between defined limits.

1.1.3.3.2**worst case conditions (for a single characteristic)**

the values of the applied conditions which individually are chosen from within a specified range and together produce the most unfavourable value for a considered characteristic

NOTE The worst case conditions for different characteristics may be different.

1.1.3.3.3**limiting conditions of use (absolute limiting ratings)**

the values of electrical, thermal, mechanical or environmental quantities assigned by the manufacturer which establish a limiting capability or a limiting condition beyond which damage to the integrated circuit may occur

1.1.3.3.4**recommended conditions of use**

the values of electrical, thermal, mechanical or environmental quantities within which correct operation should be achieved

1.1.3.4 terms for the characteristics of digital circuits

the following terms may be qualified by additional adjectives such as expander, trigger, preset, clear, etc.

1.1.3.4.1**HIGH state input minimum voltage**

the minimum input voltage in the HIGH state applied to one or more inputs which ensures correct operation of the digital circuit

1.1.3.4.2**LOW state input maximum voltage**

the maximum input voltage in the LOW state applied to one or more inputs which ensures correct operation of the digital circuit

1.1.3.4.3**LOW state output maximum voltage**

the maximum voltage of the output in the LOW state for specified output current

1.1.3.4.4**HIGH state output minimum voltage**

the minimum voltage of the output in the HIGH state for specified output current

1.1.3.4.5**HIGH state static voltage noise margin**

the difference between the HIGH state output minimum voltage and the HIGH state input minimum voltage

1.1.3.4.6**LOW state static voltage noise margin**

the difference between the LOW state input maximum voltage and the LOW state output maximum voltage

1.1.3.4.7**static voltage noise margin**

the smaller of the HIGH state and the LOW state static voltage noise margins

1.1.3.4.8**HIGH state input current**

the current measured at an input terminal when a specified HIGH state voltage is applied to that input

1.1.3.4.9**LOW state input current**

the current measured at an input terminal when a specified LOW state voltage is applied to that input

1.1.3.4.10

HIGH state output current

the forced current measured at the output terminal which will guarantee a specified HIGH state output voltage

1.1.3.4.11

LOW state output current

the forced current measured at the output terminal which will guarantee a specified LOW state output voltage

1.1.3.4.12

input loading factor (of a bipolar circuit)

a factor which indicates the ratio of the input current of a specified input terminal to the input current of a particular integrated circuit which is chosen as a reference load

1.1.3.4.13

output loading capability (of a bipolar device)

a factor which indicates the ratio of the maximum output current of a specified output terminal to the input current of a particular integrated circuit which is chosen as a reference load

NOTE The reference load is chosen so that the input loading factor and the output loading capability become whole (integral) numbers.

1.1.3.4.14

HIGH to LOW state output delay time

the time interval between specified reference points on the input and on the output waveforms when the output is going to the LOW state

1.1.3.4.15

HIGH to LOW state transition time

the time interval between specified reference points on the output waveform when the output is going to the LOW state

1.1.3.4.16

HIGH to LOW state propagation time

the time interval between specified reference points on the input and on the output waveforms when the output is going to the LOW state and when the device is driven and loaded by like devices

1.1.3.4.17

LOW to HIGH state output delay time

the time interval between specified reference points on the input and on the output waveforms when the output is going to the HIGH state

1.1.3.4.18

LOW to HIGH state transition time

the time interval between specified reference points on the output waveform when the output is going to the HIGH state

1.1.3.4.19

LOW to HIGH state propagation time

the time interval between specified reference points on the input and on the output waveforms when the output is going to the HIGH state and when the device is driven and loaded by like devices

1.1.3.5 Terms for the characteristics of analogue circuits

1.1.3.5.1

input off-set voltage

the continuous (direct) voltage required to be applied between the input terminals of a differential amplifier for specified input and output loading circuits to cause the output voltage to attain a specified level, usually zero

NOTE When the amplifier has two symmetrical outputs the specified voltage refers to the difference in voltage between these outputs.

1.1.3.5.2**input off-set current**

the continuous (direct) current which has a value equal to the difference in the currents flowing in the two input terminals which will cause the output voltage to attain a specified level, usually zero, under stated operating conditions, in particular the input and output loading circuits

NOTE When the amplifier has two symmetrical outputs, the specified voltage refers to the difference in voltage between these outputs.

1.1.3.5.3**input bias current**

a) *(of a differential amplifier)*. The average of the two input currents when the output voltage is at a specified level, usually zero.

b) *(of a single input amplifier)*. The input current when the output voltage is at a specified level, usually zero.

1.1.3.5.4**common-mode voltage amplification (of a differential input linear amplifier)**

the ratio of the change in magnitude of the output voltage to the change in magnitude of the input voltage applied equally and in phase to each input terminal under specified conditions

1.1.3.5.5**differential-mode voltage amplification (of a differential input linear amplifier)**

the ratio of the change in magnitude of the output voltage to the change in the magnitude of the differential input voltage under specified conditions

1.1.3.5.6**common-mode rejection ratio (of a differential input linear amplifier)**

the ratio of the differential-mode voltage amplification to the common-mode voltage amplification each under the same specified conditions

NOTE In practical cases, the common-mode rejection ratio can be derived from a measurement of common-mode amplification that uses a higher value of input signal than that used for measuring the differential-mode amplification. This usually gives a figure equal to, or worse than, that given by the theoretical situation of equal input signals. If this ratio is not that obtained under small-signal conditions, the conditions should be stated in detail.

1.1.3.5.7**(equivalent) input drift**

the change in the input d.c. voltage or d.c. current (but with reversed sign) necessary to compensate for a change in output d.c. voltage or d.c. current, caused by a specified change of supply voltage, or time or temperature or other environmental conditions

1.1.3.5.8**temperature coefficient of input off-set voltage**

the ratio of the change of input off-set voltage to the change of operating temperature causing it, other conditions remaining constant

1.1.3.5.9**temperature coefficient of input off-set current**

the ratio of the change of input off-set voltage to the change of operating temperature causing it, other conditions remaining constant

1.1.3.5.10**common-mode input voltage range**

the range of voltage between the input terminals strapped together and the reference or earth terminal which, if exceeded, may cause the amplifier to cease to function within specification

1.1.3.5.11**differential-mode input voltage range**

the range of voltage between the input terminals which, if exceeded, may cause the amplifier to cease to function within specification

1.1.3.5.12**output voltage range**

the maximum peak-to-peak output voltage which can be obtained with specified amplitude distortion when the quiescent d.c. output voltage is set to a specified reference level

1.1.3.5.13**noise**

the unwanted output signal generated by the circuit, not coherent with the input signal. For linear circuits this is normally referred to the input as an equivalent input signal under specified conditions

1.1.3.5.14**input terminal impedance**

the impedance between any input terminal and the reference terminal with other input terminals isolated, or with specified connections, and under specified conditions

1.1.3.5.15**signal input impedance**

the impedance between the signal terminals at a specified frequency under specified conditions

1.1.3.5.16**common-mode input impedance**

the impedance between the signal terminals connected together by a capacitor having a small impedance at the test frequency and the reference terminal, under specified conditions

1.1.4 Letter symbols, signs and abbreviations

The letter symbols, signs and abbreviations shall be in accordance with the principles given in BS 3363 (see also IEC Publication 148).

In addition, for the purpose of integrated circuit specifications, the following letter symbols shall be used.

1.1.4.1 Digital circuits

a) The subscript sequence for voltage and current symbols is as follows:

First subscript: Terminal identification
 Second subscript: HIGH or LOW state
 Third subscript: Further qualification if required

	Voltages		Currents	
	Input	Output	Input	Output
HIGH state	V_{IH}	V_{OH}	I_{IH}	I_{OH}
LOW state	V_{IL}	V_{OL}	I_{IL}	I_{OL}

Particular values of the above quantities may be denoted by further subscripts (1), (2), etc.

Limiting values of the above quantities may be qualified by the addition of subscripts “min” and “max”.

b) The subscript sequence for time symbols is as follows:

First subscript: Type of time interval.
 Second and third subscripts: Change of state of output.
 The subscript P is used for propagation time.
 The subscript D is used for delay time.
 The subscript T is used for transition time.

Example:

t_{PLH} denotes, LOW to HIGH state output propagation time.

t_{PHL} denotes, HIGH to LOW state output propagation time.

Limiting values of the above quantities may be qualified by addition of subscripts “min” and “max”.

NOTE The standard symbol for pulse duration, t_p , may be qualified by the addition of subscript words, e.g. clock, count, etc.

c) The following abbreviations are in common use:

DTL: Diode transistor logic.

RTL: Resistor transistor logic.

TTL: Transistor transistor logic.

ECL: Emitter coupled logic.

1.1.5 Graphical symbols

The graphical symbols to be used on all integrated circuit specifications shall be in accordance with BS 3939 and 1.1.5 of BS 9400.

1.1.6 Marking of the component and package

The following symbols or codes shall be marked on the device in the following order of preference as space permits:

a) Terminal identification (see 1.1.6.1).

b) Customer's type number or drawing number and, where applicable, issue. Alternatively, a colour code may be used (see 1.1.6.2 and 1.1.6.7).

c) Tolerance identification (see 1.1.6.8).

d) Factory identification code or manufacturer's name or trade mark (see 1.1.6.3).

e) Date code (see 1.1.6.4).

f) British Standard detail specification number.

All the symbols and codes, except the terminal markings and colour band identification if used, shall also appear on the primary package, e.g. carton, box, plastics envelope, etc., used as initial protection or wrapping for delivery. Where colour band identification is used on the device the manufacturer's type number shall appear on the primary package.

1.1.6.1 Terminal identification. The terminals or leads of integrated circuits shall be marked or identified in accordance with the specified outline as given in the detail specification.

1.1.6.2 Customer's type number (or colour code). The marking of the customer's type number shall be in accordance with that given in the detail specification.

1.1.6.3 Factory identification code or manufacturer's name or trade mark. Where the certificate of conformity enables traceability to a manufacturer's factory, the manufacturer's name or trade mark is sufficient. In all other cases the factory identification code shall be used and shall be in accordance with PD 9002.

1.1.6.4 Date code. The date code should be in accordance with clause 22 of BS 9000-1.

Text deleted

1.1.6.6 Detail specification number. Each detail specification shall carry a distinguishing number made up of the number of this specification and a unique number (e.g. the customer's reference/drawing number) identifying the item to the agreed customer's specification (see also section 2 of this standard).

1.1.6.7 Colour code identification for type number. When specified in the detail specification, the colour code identification for type number shall be as specified in Table 1. The number sequence shall be from left to right, the left being signified by either a wider band of colour or a placement of the colour group towards the left hand edge of the body. Two digit numbers shall be preceded by a zero.

1.1.6.8 Tolerance identification (where applicable). When specified in the detail specification, the component tolerance shall be printed on the device package, e.g. by the use of letter codes in accordance with BS 1852.

Table 1 — Colour code for identification number

Colour	Identification number
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Purple (Violet)	7
Grey	8
White	9

1.1.7 Eligibility for release

Integrated electronic circuits and micro-assemblies shall be eligible for submission for capability approval and release to BS 9450 if the procurement of materials and components and all stages of manufacture and test are undertaken at any BS 9450 approved manufacturing facility (except as allowed in 1.1.7.3).

1.1.7.1 Film and hybrid integrated circuits, micro-assemblies, micro-modules and microwave integrated circuits. This also applies to part completed film and hybrid circuits supplied for subsequent processing.

1.1.7.1.1 Acceptable primary stages of manufacture are either:

- The production of the first conductive layer as an additive process to a substrate (e.g. conductive inks applied to an alumina or porcelain-on steel or similar base); or
- The production of the first conductive pattern as a subtractive process to a suitably prepared substrate (e.g. removal of conductive material from a copper clad epoxide glass fabric, or similar, base).

Organic printed boards with mounted or deposited components shall only be released under BS 9450 if no one dimension exceeds 110 mm. Unpopulated organic printed boards may not be released under BS 9450.

1.1.7.1.2 All stages of manufacture, up to and including the finished product, are not limited by size or complexity (other than by the constraints given in 1.1.7.1.1) but shall be restricted to practices and procedures covered by this specification and declarations within the approved manufacturer's capability manual.

1.1.7.2 Monolithic and multichip semiconductor circuits

1.1.7.2.1 Acceptable primary stages of manufacture are:

- For bipolar integral circuits, the first process which changes the mono-crystalline semiconductor material from being either wholly p-type or wholly n-type.
- For MOS circuits, the first oxidation of the semiconductor material.
- For integrated circuits incorporating bulk effect devices, the first process which changes the mono-crystalline semiconductor to give the required doping profile.

1.1.7.2.2 All stages of manufacture, up to and including the finished product, are not limited by size or complexity but shall be restricted to practices and procedures covered by this specification and declarations within the approved manufacturer's capability manual.

1.1.7.3 Use of non-approved subcontractors. Should an approved manufacturer wish to subcontract operations corresponding to the primary stage of processing or any subsequent stages to an unapproved manufacturer, he shall meet the requirements of 14.3.2 of BS 9000-1 and, additionally, ensure the conditions given in a) to e) are met.

- The subcontracted operation shall comply with 1.1.7.1.1 and 1.1.7.2.2 as follows:
 - The subcontracted manufacture may be either the preparation of the substrate prior to discrete component assembly/diffusion processes [as in 1.1.7.1.1 a) and 1.1.7.2 above], or the subsequent assembly of the device.
 - If the primary stage of manufacture conforms to 1.1.7.1.1 b) above, then the substrate must be released under BS 9760 or supplied under equivalent disciplines agreed with the NSI.

b) The supervising inspectorate shall be satisfied that the chief inspector of the certifying manufacturer has been provided with the full quality assurance and inspection documentation from the non-approved facility, and that he had the responsibility for inspection of the work and the inspection arrangements there. Such documentation shall include the inspection records for each sample of the product which undergoes inspection.

c) The chief inspector shall be provided with the production line process charts, the defined inspection points, the inspection requirements at each stage and the quality control requirements, together with the procedures for the transfer of the parts from the place of manufacture to the certifying manufacturer. The supervising inspectorate shall be informed and have access to this documentation and be able to verify the application of these requirements.

d) Any changes in inspection requirements and manufacturing procedures shall be reported back to the approved manufacturer's chief inspector who is certifying the components. These changes shall be declared on the document accompanying the transferred parts. The significant changes shall be reported by the approved manufacturer's chief inspector to the supervising inspectorate.

e) The approved manufacturer shall perform the acceptance tests required by the detail specification for the component he is certifying. He can perform the acceptance tests in a non-approved facility provided that this facility is supervised by the supervising inspectorate. Acceptance tests can be sub-contracted to approved test laboratories.

1.1.8 Structural similarity

The concept of structural similarity is not required when capability approval is used, as the relevant requirements are covered in the manufacturer's capability approval.

1.1.9 Delayed delivery

Released lots that have been in store for more than 3 years shall undergo and satisfy group A and group B tests before delivery. No further re-testing is needed for lots delivered within 3 years of a re-test.

1.1.10 Supplementary procedure for qualification approval

Not applicable.

1.1.11 Certified test records

The information to be present in certified test records shall be as stated in Table 1.3.3/1 of this standard. Manufacturers are free, but not obliged, to give additional CTR information beyond that required in Table 1.3.3/1, but where this additional information is derived from sources other than acceptance procedures this shall be stated.

1.1.12 Standard ratings and characteristics

The values for ratings and characteristics shall be chosen from the list given below. If additional items are included in a detail specification, the values and conditions under which they apply shall be stated. Any interdependence of ratings and characteristics and any limiting conditions of use shall be stated.

1.1.12.1 Supply terminal voltages. Preferred nominal values 3.0 V, 4.0 V, 5.0 V, 9.0 V, 12 V, 24 V, 30 V and 48 V. Preferred tolerances, 5 %, 10 % and 20 %. The tolerances above and below the normal value need not necessarily be the same.

1.1.12.2 Test temperatures. – 55 °C, – 40 °C, – 25 °C, 0 °C, + 25 °C, + 70 °C, + 85 °C, + 100 °C, + 125 °C and + 150 °C.

1.1.12.3 Preferred temperature ranges

- a) – 55 °C to + 125 °C.
- b) 0 °C to + 70 °C.
- c) – 40 °C to + 100 °C.

1.1.13 Unchecked parameters

Not applicable.

1.1.14 Procedure to be followed in the event of failure at groups C and D inspection

The procedure given in 20.11 of BS 9000-1:1981 shall be applied.

1.1.15 Ordering information

Not applicable.

1.1.16 Release prior to completion of group B tests

Not applicable

1.1.17 Supplementary procedure for reduced inspection

The procedure in 17.4 of BS 9000-1:1981 shall be applied.

1.1.18 Supplementary procedure for general application category components

Not applicable.

1.1.19 Rework

Rework shall only be permitted within the procedures declared in the manufacturer's approved capability manual. Such procedures must demonstrate, to the satisfaction of the supervising inspectorate, that the subsequent reliability of the integrated circuit as supplied to the customer is not thereby impaired.

A customer may prohibit rework on circuits to be supplied for a particular contract.

Reworked packages which have been resealed shall be subjected to and pass the "Rapid change of temperature test" 1.2.6.13, or the "Sealing, fine and gross leak tests", 1.2.6.14.1 and 1.2.6.14.2.

Where circuits have been directly embedded in hard plastic encapsulants, e.g. by moulding, casting, or dipping using epoxy or silicone resins, no rework shall be permitted.

Replacement of defective add-on components and/or defective wire bonds shall be permitted within the following limits, unless otherwise restricted in the manufacturer's approved capability manual.

- a) Scratched, open or discontinuous metallization paths or conductor patterns or semiconductor material shall not be repaired.

Film conductors may be repaired by the attachment of conducting links provided that the number and type of joints so made comply with the requirements of the manufacturer's approved capability manual.

- b) Not more than one attempt shall be permitted to reconnect a wire or component termination at any pad or post. No reconnections shall be permitted directly over an area where the metallization of the intended bond area has been lifted.

- c) On a semiconductor die, no ball bond on top of another shall be permitted.

- d) Encapsulated components which have been removed from a defective substrate may be re-used on another substrate provided they satisfactorily fulfil the requirements of the approved electrical and physical tests prior to re-use. Such components shall not be re-used more than once.

In the case of hermetically sealed components which have been removed, all glass-to-metal seals shall be inspected for cracks before re-use.

- e) If a component which has been soldered is removed, not more than two solder reflow cycles shall be applied to the conductor or pad involved, whether or not a replacement component is to be re-connected.

- f) Semiconductor dice which have been bonded shall not be removed and re-bonded. However dice which have been attached to headers or substrates may be detached and re-used provided it is demonstrated that the method of attachment allows this to be done without impairing the subsequent reliability of the complete integrated circuit.

1.1.20 Sampling procedures

At the discretion of the manufacturer and with the agreement of the NSI, the manufacturer may use either LTPDs (see ISO 2859) or AQLs. To ensure acceptable correlation between AQL and LTPD sampling plans, the maximum acceptance number should not be greater than four. The equivalent sampling plans are given in the table below.

AQL	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.5	6.5
LTPD	0.7	1.0	2.0	3	5	7	10	20	30	50

1.2 Test procedures

The test and measurement methods and procedures given in 1.2.1 to 1.2.11 inclusive of this section shall be applied as follows:

- a) When they are required to verify facilities or assessment tests included as part of a manufacturer's capability assessment programme, or
- b) when they are required to perform tests or measurements contained in a customer's detail specification.

A manufacturer is free to specify those tests which he offers as part of his declared production capability, and which will be specified in his capability manual.

Tests and measurement procedures shall be applied in accordance with the inspection requirements of BS 9000.

1.2.1 Standard conditions for testing

1.2.1.1 General. Unless otherwise stated, all tests shall be made under standard atmospheric conditions for testing, as specified in BS 2011 (IEC 68).

Before the measurements are made, the integrated circuit shall be stored at the measuring temperature for a time sufficient to allow the entire circuit to reach this temperature. The recovery period specified after conditioning is sufficient for this purpose.

When measurements are made at a temperature other than that specified, the ambient temperature during the measurement shall be recorded and the results shall be corrected, where necessary, to the specified temperature.

During measurements, the integrated circuit shall not be exposed to draughts or direct sun-rays, and shall be protected from unintentional radioactive and electromagnetic radiations.

1.2.1.1.1 Alternative test methods. The measurements and conditions specified are not the only methods which can be used but the supervising inspector shall be satisfied that other methods including pulse methods and/or conditions of measurements employed will give results compatible with the methods and/or conditions specified in this standard and the relevant detail specification. By "compatible" is meant that the value of the characteristic established by such other methods will fall within the specified limits when measured by the specified method and under the specified conditions.

1.2.1.2 Safety aspects. An employer is responsible, under the Health and Safety at Work Act 1974, for ensuring the health and safety of employees.

To minimize possible hazards which may arise from the carrying out of tests contained in this standard and related documents, the following precautions are recommended. These recommendations are not necessarily complete in their coverage and are given for guidance only.

1.2.1.2.1 Toxic vapour and poisonous residues. When performing the following listed tests from BS 9400 and BS 9450 care should be taken to ensure that any toxic vapours or poisonous residues which may be liberated, are not inhaled or directly handled by personnel working in, or adjacent to, the test area(s), and that they are disposed of in a safe manner.

1.2.6.1	Cold for non-heat dissipating specimen with sudden change of temperature	1.2.6.14	Sealing
1.2.6.2	Dry heat for non heat dissipating specimen with sudden change of temperature	1.2.6.15	Soldering
1.2.6.3	High temperature storage	1.2.6.16	Robustness of terminations
1.2.6.4	Damp heat, steady state	1.2.6.17	Flammability
1.2.6.5	Damp heat, cyclic	1.2.6.18	Immersion in cleaning solvents
1.2.6.6	Shock	1.2.6.19	Rapid change of temperature, two-bath method
1.2.6.7	Bump	<i>Text deleted</i>	
1.2.6.8	Vibration	1.2.6.21	Damp heat steady state with bias
1.2.6.9	Acceleration steady state	1.2.6.22	Thermal intermittance test
1.2.6.10	Mould growth	1.2.7	Electrical endurance test procedures
1.2.6.12	Low air pressure	1.2.8.2	Damp heat accelerated test for long term changes in resistance and interconductor leakage
1.2.6.13	Rapid change of temperature	1.2.9	Screening test procedures

1.2.1.2.2 Fire. Flammability tests should be carried out in a hooded fume cupboard (or other suitable container) lined with fire-resistant material(s) from which the gaseous products of combustion are extracted to a safe dispersal point.

1.2.1.2.3 Hot equipment. Heated equipment used for tests e.g. ovens, cycling chambers, solder baths, should be suitably protected to minimize the risk of accidental burns and incorporate devices to prevent overheating in the event of normal control system failure.

1.2.1.2.4 Radiation. The storage and handling of radioactive materials used for leak tests should comply with the relevant safety standards.

1.2.1.2.5 Mechanical. Pressurized or evacuated containers used for leak tests should be subject to regular inspection to minimize explosion/implosion risks and, where appropriate, tested in accordance with statutory regulations.

1.2.1.2.6 Electrical test methods (digital and analogue circuits). It is assumed that personnel carrying out any of the electrical tests described in 1.2.4 of this standard will be familiar with basic safety precautions to avoid hazards from electrical shock, which are inherent in any test involving the use of power supplies which may be driven from the a.c. mains. Care should be taken to avoid accidental contact with supply voltages which are not in the “low-voltage” category. Circuits can operate with supply voltages up to 100 V. The existence of this hazard can be verified from the conditions specified for the circuit under test.

Attention is drawn to the possibility of the following additional hazards arising, particularly under fault conditions, either within the circuit itself, or in the ancillary test equipment.

a) *Toxic vapours.* These might arise if a device overheats, and their effect would depend principally on the type of encapsulation used, and the chemicals used in passivation layers on the circuit or in the chip mounting.

b) *Explosions.* This hazard could exist if a device is severely overstressed under test, either thermally or electrically. For most measurements, adequate protection can be provided by the use of power supplies with current limiters set to a value specified appropriately for the circuit under test, but this protection may not be adequate for BS 9400 test method 3206. This explosion hazard is most likely to arise from use of BS 9400 test methods 2009, 2010, 2011 and 2014.

An explosion can also occur due to rapid expansion of entrapped moisture or other liquid under normal dissipation. This can result from prolonged storage or from performing certain of the sealing tests.

c) *Burns.* These can occur when handling hot or cold equipment used for high temperature and low temperature measurements. In particular, circuits tested at maximum power dissipation may achieve relatively high case or chip temperatures, which could result in burns to the fingers if the device is picked up immediately after the test is terminated. This problem could also be encountered if a fault develops within a device, resulting in abnormally high internal power dissipation. In addition, burns could occur if an operator's fingers are placed in an area where microwave radiations of even modest power are focussed.

d) *Probe hazards.* The possibility of skin injuries exists if probe testers are being used on circuit wafers or chips, and no protective clothing is worn.

While risks associated with any of the above hazards are relatively low, it is considered that they do exist, and could arise when applying any of the published test methods. They are not confined to the tests specifically mentioned.

1.2.1.3 Drying. When drying is required in the test procedure, the integrated circuit shall be conditioned before measurement is made, using either procedure 1, or procedure 2 as required by the detail specification.

Procedure 1: For 24 ± 4 h in an oven at a temperature of 55 ± 2 °C and at a relative humidity not exceeding 20 %.

Procedure 2: For 96 ± 4 h in an oven at a temperature of 100 ± 5 °C.

The integrated circuit shall be allowed to cool in a desiccator, using a suitable desiccant such as activated alumina or silica gel, and shall be kept therein from the time of removal from the oven to the beginning of the specified test.

1.2.2 External visual inspection

Unless otherwise specified, visual inspection shall be performed under approved factory lighting conditions and under normal visual conditions.

Inspection shall include the following items:

- a) Correctness of marking.
- b) Correctness of terminal identification.
- c) Correct encapsulation.
- d) Unbroken body.

1.2.3 Dimensioning and gauging procedures

This section covers the requirements for the dimensional inspection of integrated circuits to be used as and when required by the detail specification and in accordance with the general inspection requirements of BS 9000.

These tests shall be made in accordance with the specified drawing and as given below. The dimensions, which shall be checked as part of the group B, C and D inspection requirements, are indicated by the standardized letter references in IEC Publication 191-1 which are also used in the drawings in BS 3934.

Configuration of devices	Group B	Group C	Group D
a) Wire mounted single ended, e.g. SO-3 (BSI), C4 (IEC) with base SB8-1A (BSI), B7A (IEC)	ϕD A	ϕB_2 L	All ^a
b) Flat pack e.g. SO-92 type 1	H Number of leads Seated height (maximum)	$L_{(\min)}$ $b_{(\max)}$ e $Z_{(\max)}$	All ^a
c) In-line (body width does not overhang terminals) e.g. Dual-in-line, SO-87 type 1	$D_{(\max)}$ Seated height (maximum)	$b_{(\max)}$ $c_{(\max)}$ $L_{(\min)}$ Stand off height (minimum)	All ^a
d) In-line (body overhangs terminals)	$D_{(\max)}$ $Z_{(\max)}$ Package width (maximum) $Z_{1(\max)}$ Seated height (maximum)	$\phi b_{(\max)}$ $L_{(\min)}$ Stand off height (minimum)	All ^a
^a All dimensions included on the BS 3934 drawing called up in the specification or the drawing in the specification and prepared in accordance with BS 3934 except those already covered in groups B and C.			

1.2.4 Electrical test procedures

1.2.4.1 General. This clause gives information of a general nature applying to electrical measurement techniques and general precautions to be applied during measurements.

Text deleted

1.2.4.1.2 Limiting conditions of use. The test conditions for all measurements should be such that the limiting conditions of use of the device are not exceeded.

The precautions should include limits on maximum instantaneous currents and applied voltages. It is recommended that devices should not be inserted into, nor removed from, a test circuit while the latter is energized.

1.2.4.1.3 Equilibrium conditions. All electrical tests shall be conducted under equilibrium conditions unless otherwise specified or unless the measurement is being carried out under pulsed conditions. When test conditions cause significant change with time of the characteristic being measured, means of compensation for such effects will be specified; for example, the length of time that the device shall be maintained at test conditions before making a measurement.

1.2.4.1.4 Temperature. Unless otherwise specified, all electrical measurements shall be made at an ambient or reference point temperature or 25 ± 2 °C. Measurements may be carried out at temperatures other than 25 °C provided that the supervising inspector is satisfied that the device performance will be in accordance with all the provisions of the detail specification when tested at 25 °C.

The ambient temperature shall be measured as the air temperature below the integrated circuit in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

The reference point temperature for case rated integrated circuits intended for conduction cooling through a mounting base shall be measured in accordance with method 0001, given in BS 9400.

For circuits specified to be used under conditions other than ambient or conduction cooling, the temperature shall be measured as required by the detail specification.

For measurements at low and high temperatures the methods described in 1.2.6.1 and 1.2.6.2 respectively shall be applied except that the time of exposure shall be reduced to that sufficient to allow temperature equilibrium to be reached. Recovery conditions do not apply.

The temperatures shall be selected from those listed in 1.1.12.

1.2.4.1.5 Measurement circuit requirements and precautions

NOTE A load in 1.2.4.1.5.4 and 1.2.4.1.5.6 is chosen to represent the equivalent resistance of the test circuit and unit under test. For acceptance test purposes, the resistor value should represent the limiting conditions.

1.2.4.1.5.1 Open-circuit. An open-circuit shall be considered to exist if a two-to-one decrease in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of measurement. The values of high resistances (whether of circuit components or meters) specified in the circuits, should be so high that a two-to-one decrease in their value will not affect the desired accuracy of the measurement.

1.2.4.1.5.2 Short-circuit. A short-circuit shall be considered to exist if a two-to-one increase in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. Capacitors used to couple or by-pass the test signal should present effective short-circuits at the test frequency. In certain of the high frequency measurements, where r.f. decoupling is important, the necessary components and/or mounting conditions of the device shall be as specified.

1.2.4.1.5.3 Small-signal. A signal shall be considered small if a two-to-one change in its magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. Care should be taken that the measuring equipment does not introduce spurious oscillation or distortion likely to affect the required accuracy of measurement.

1.2.4.1.5.4 Constant current source. A current source shall be considered constant if a two-to-one increase of a load impedance (see note above) does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.

1.2.4.1.5.5 Current measuring device. The effective admittance of a current measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of the test.

1.2.4.1.5.6 Constant voltage source. A voltage source shall be considered constant if a two-to-one decrease of a load impedance (see note above) does not produce a change in the parameter being measured that is greater than the required accuracy of measurement.

1.2.4.1.5.7 Voltage measuring device. The effective impedance of a voltage measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of measurement.

1.2.4.1.6 Power supplies. The sources of direct currents and voltages should not have ripple contents large enough to affect the desired accuracy of measurement. Test or supply voltages or currents shall be within ± 1 % of the specified value.

1.2.4.1.7 Precision of measurements. The limits quoted in detail specifications are absolute. Tolerances on measurements shall be taken into account when determining the actual measurement limits.

1.2.4.1.8 Multiple integrated circuits. The detail specification will state the test requirements for each section of a multiple integrated circuit consisting of several functionally independent sections. All terminals associated solely with sections not under test shall be left open-circuit unless otherwise specified.

1.2.4.2 Measurement methods. Where applicable the measurement methods shall be selected from BS 9400 or other generic specifications in the BS 9000 series.

1.2.5 Mechanical test procedures

All the mechanical test procedures required for integrated circuits are included in 1.2.6.

1.2.5.1 Direction of acceleration/force. For devices with internal elements mounted with the major seating perpendicular to the Y axis, the Y_1 orientation shall be defined as that one in which the element tends to be removed from its mount.

1.2.6 Environmental test procedures

This clause covers the requirements for environmental tests to be used in accordance with the general requirements of BS 9000. The conditions given in each procedure are those from which the manufacturer chooses in order to establish his capability approval. Other conditions may be prescribed by a customer for particular applications. These conditions shall be included in the detail specification. They should be taken from those included in BS 2011.

Unless otherwise specified, all tests shall be performed under the standard atmospheric conditions for testing as specified in BS 2011.

When testing is performed by the device manufacturer more severe test conditions than those specified are permitted. In this case temperatures may be higher than those specified when the specified temperatures are 25 °C and above, and lower than those specified when the specified temperatures are below 25 °C. In all other cases the prescribed limits of test conditions shall be used.

Wherever possible, the tests given in the following subclauses are taken from BS 2011 or BS 6493-3. However, some tests are additional to those in BS 2011 or BS 6493-3 (e.g. rapid change of temperature) and in these cases the test procedures are given in full.

1.2.6.1 Test Aa: Cold for non-heat dissipating specimen with sudden change of temperature.

(This test is non-destructive). The sample shall be subjected to the procedure described in test Aa of BS 2011-2.1A:1977. The air in the chamber need not be agitated. Unless otherwise specified there shall be no upper limit requirements for the time of recovery or the relative humidity during the recovery period.

The following specified conditions will be given in the detail specification:

- a) Temperature of conditioning.
- b) Duration of conditioning.
- c) Association with other tests in a sequence.
- d) Electrical and mechanical tests to be made prior to conditioning and after recovery, as appropriate.

1.2.6.2 Test Ba: Dry heat for non-heat dissipating specimen with sudden change of temperature.

(This test is non-destructive.) The sample shall be subjected to the procedure described in test Ba of BS 2011-2.1B:1977.

NOTE The atmosphere should be of inert gas if the devices are for subsequent delivery or subject to solderability tests.

The air in the chamber need not be agitated and there shall be no requirement for relative humidity during the conditioning period.

The duration of the recovery period shall be not less than 1 h nor more than 6 h and there shall be no requirement for the control of relative humidity during that period.

The following specified conditions will be given in the detail specification:

- a) Temperature of conditioning.
- b) Duration of conditioning.
- c) Association with other tests in sequence.
- d) Electrical and mechanical tests to be made prior to conditioning and after recovery, as appropriate.

1.2.6.3 High temperature storage (This test is non-destructive.)

1.2.6.3.1 Purpose. The purpose of this test is to determine the effect on integrated circuits of storage at elevated temperatures without electrical stress applied. This method may also be used in a screening sequence or as a pre-conditioning treatment prior to the conduct of other tests. This test shall not be used to determine device failure rates for other than storage conditions.

1.2.6.3.2 Apparatus. The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature and suitable electrical equipment to make the specified end point measurements.

1.2.6.3.3 Procedure. The device shall be stored at the specified ambient condition for the specified time. End-point measurements shall be made at 0 h and after the specified duration of test $+72_{-0}^{\circ}$ h. End-point measurements shall be made at standard conditions and sample units shall be removed from the test ambient and allowed to reach standard conditions before final end-point measurements. Additional measurements may be made at intermediate points. It may be desirable to make end-point and, where applicable, intermediate measurements on a serialized device basis or on the basis of a histogram distribution by total sample in order to increase the sensitivity of the test to parameter degradation or the progression of specific failure mechanisms with time and temperature.

1.2.6.3.4 Test condition. The ambient test temperature shall be in accordance with one of the following test temperatures or as specified.

Test condition	Temperature
A	$70 \pm 5^{\circ}\text{C}$
B	$125 \pm 5^{\circ}\text{C}$
C	$150 \pm 5^{\circ}\text{C}$
D	$175 \pm 5^{\circ}\text{C}$
E	$200 \pm 5^{\circ}\text{C}$
F	$85 \pm 5^{\circ}\text{C}$
G	$100 \pm 5^{\circ}\text{C}$

1.2.6.3.5 Specified conditions. The following test conditions will be obtained from the detail specification:

- Device history, whether screened or unscreened.
- Test temperature.
- Test duration if other than 1 000 h.
- End-point measurements.
- Intermediate measurements if applicable.
- Device number or special data reporting requirements if applicable.

1.2.6.4 Test Ca: Damp heat, steady state. (This test is destructive.) The sample shall be subjected to the procedure described in test Ca of BS 2011-2.1Ca:1977.

Unless excluded by the detail specification, devices subjected to the test shall be checked for corrosion as follows:

- The marking shall remain legible.
- Where appropriate, the lead wires shall be subjected to one bending cycle as in **1.2.6.16.2** and fracture of a lead shall constitute a failure.

The following specified conditions will be given in the detail specification:

- The severity of test (4 days, 21 days or 56 days).
- Loading conditions.
- Electrical and mechanical tests to be made prior to conditioning and after recovery, as appropriate.

1.2.6.5 Test Db: Damp heat, cyclic. (This test is destructive.) The sample shall be subjected to the procedure described in test Db of BS 2011-2.1Db:1981.

There is no special pre-conditioning procedure.

There are no initial measurements.

The high temperature shall be $40 \pm 2^{\circ}\text{C}$ or $55 \pm 2^{\circ}\text{C}$ and the low temperature shall be $25 \pm 3^{\circ}\text{C}$.

The relative humidity during rise time shall be $> 95\%$ and $< 100\%$.

The relative humidity at high temperature shall be between 90% and 95% .

The relative humidity during the remaining period shall be $> 95\%$ and $< 100\%$.

The number of cycles shall be 6 or 28.

During conditioning there shall be no loading and no measurements.

Unless otherwise specified the sample shall remain under standard atmospheric conditions for recovery for not less than 1 h nor more than 2 h.

The values of the following test conditions shall be specified in the detail specification:

- a) High temperature.
- b) Number of cycles.
- c) Final measurements.

When the test is performed as a group B test the number of cycles shall be six.

When the test performed is a group C test the number of cycles shall be 28.

Unless excluded by the detail specification devices subjected to the 28-cycles test in group C inspection shall be checked for corrosion as follows:

- 1) The marking shall remain legible.
- 2) When appropriate, the lead wires shall be subjected to one bending cycle as described in **1.2.6.16.2** and the fracture of a lead shall constitute a failure.

1.2.6.6 Test Ea: Shock. This test is non-destructive unless otherwise stated in the detail specification. The test is in accordance with BS 2011-2.1Ea:1977, incorporating Amendments No. 1 and No. 2.

See also **1.2.5.1**.

The device shall be rigidly mounted by the body, with protection for the terminations, unless otherwise specified in the detail specification.

The half-sine pulse shape shall be used unless otherwise specified in the detail specification.

The severity shall be selected from the following table.

Condition	Peak acceleration		Pulse duration
	m/s ²	g _n	ms
1	294	30	18
2	490	50	11
3	981	100	6
4	4 900	500	1
5	14 700	1 500	0.5

Three successive shocks shall be applied in each direction of three mutually perpendicular axes so chosen that faults are most likely to be revealed (i.e. a total of 18 shocks), unless a larger number of shocks is specified in the detail specification.

Unless otherwise prescribed in the detail specification, the devices shall be non-operating during the test.

The detail specification shall prescribe:

- a) method of mounting, if not rigidly mounted by the body;
- b) pulse shape, if not half-sine;
- c) severity (condition 1, 2, 3, 4 or 5);
- d) number of shocks if more than three in each direction;
- e) operating conditions if the device is operating during the test;
- f) measurements and mechanical/visual checks before and after the test;
- g) whether the sealing test shall be performed as a final measurement.

1.2.6.7 Test Eb: Bump. (This test is non-destructive.) The sample shall be subjected to the procedure described in test Eb of BS 2011-2.1Eb:1977. See also **1.2.5.1**. The preferred severities are:

- a) 390 m/s² and a total of 4 000 ± 10 bumps.
- b) 390 m/s² and a total of 1 000 ± 10 bumps.
- c) 98 m/s² and a total of 1 000 ± 10 bumps.

The following specified conditions will be given in the detail specification:

- 1) Method of mounting.
- 2) Association with other tests in a sequence.
- 3) Electrical and mechanical tests to be made prior to and after conditioning, as appropriate.
- 4) Severity of test.

1.2.6.8 Test Fc: Vibration (sinusoidal). See also 1.2.5.1. (This test is destructive, since it is a vibration endurance test). This test is in accordance with BS 2011-2.1Fc:1983 Test Fc.

The device shall be rigidly mounted by the body, with protection for the terminations, unless otherwise specified in the detail specification.

NOTE The mounting of the device by its terminations introduces extra complications which affect the repeatability of the test, e.g. the provision or otherwise of plated-through holes on the printed circuit board.

The severity shall be selected from Appendix B of BS 2011-2.1Fc:1983, and shall preferably be as given in the table below.

Condition	Frequency range	Amplitude or acceleration	Number of sweep cycles in each axis
1	100 to 2 000 ^{Hz}	196 m/s ² (20g _n)	15
2	55 to 500	0.75 mm or 98 m/s ² (10g _n)	20
3	10 to 500	0.35 mm or 49 mm/s ² (5g _n)	10

Unless otherwise prescribed in the detail specification, the sample shall be divided into three subsamples and each of the subsamples shall be vibrated successively for the prescribed number of cycles in each of three mutually perpendicular axes. For this test, the three subsamples may be mounted on the three faces of a cubic mounting block, and vibrated simultaneously.

Unless otherwise prescribed in the detail specification, the devices shall be non-operating during the test.

The detail specification shall prescribe:

- method of mounting, if not rigidly mounted by the body;
- severity (condition 1, 2, 3 or other);
- vibration regime if other than that stated above;
- measurements and mechanical/visual checks before and after the test;
- whether the sealing test shall be performed as a final measurement.

1.2.6.9 Test Ga: Acceleration. (This test is non-destructive.) See also 1.2.5.1. The test is in accordance with BS 2011-2.1Ga:1984, with the following requirements.

The test shall be carried out using a centrifuge, unless otherwise specified in the detail specification. The device shall be restrained by the case or its normal mountings, and the terminations shall be secured.

The severity shall be selected from the following table.

Acceleration	
m/s ²	g _n
490	50
4900	500
1 9600	2 000
4 9000	5 000
9 8000	10 000
19 6000	20 000
29 4000	30 000

The acceleration shall be increased to the specified value in not less than 20 s, shall remain constant for at least 1 min and shall then be decreased to zero in not less than 20 s.

The detail specification shall prescribe:

- severity;
- direction of acceleration (this should be the most critical direction, e.g. that most likely to detach bonding wires from their pads);
- measurements and mechanical/visual checks before and after the test;
- whether the sealing test shall be performed as a final measurement.