

Specification for

**Integrated electronic circuits
and micro-assemblies of
assessed quality (capability
approval procedures):**

Generic data and methods of test

ICS 31.200

Committees responsible for this British Standard

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Foreword

This British Standard has been prepared by Subcommittee EPL/47. It is a revision of BS 9450 : 1975, which it supersedes. BS 9450 : 1975 is now only valid for approvals against lower level documents that are dependent upon it.

BS 9450 : 1998 contains revisions to the text of the previous edition, and introduces annexes containing requirements for the minimum content of a manufacturer's capability manual in respect of the various types of circuit covered by this specification.

In the light of the devolution of quality assessment of electronic components to documentation within the CECC and IECQ systems, both BS 9450 : 1975 and BS 9450 : 1998 are obsolescent (i.e. not recommended for use in new equipment design) and will be withdrawn when there are no approvals against the respective standards. BS 9450 : 1998 has a wider scope than its equivalent documents in these other systems, and the annexes may afford the basis of texts to be adopted by them.

Compliance with a British Standard does not of itself confer immunity from legal obligations

Summary of Pages

This document comprises a front cover, an inside front cover, pages i to vi, pages 1 to 144, an inside back cover and a back cover.

Introduction

This British Standard is the generic specification for capability approved integrated circuits in the system of standards for electronic components of assessed quality. It calls for the use of substances and/or test procedures that may be injurious to health if adequate precautions are not taken. It refers only to technical suitability and in no way absolves either the supplier or the user from statutory obligations relating to health, safety and fire hazards at any stage of manufacture or use. It follows a somewhat different pattern from other standards in the BS 9000 series since, owing to the wide diversity of customer requirements in terms of circuit functions, complexity and numbers of circuits of any one type to be supplied, the classical BS 9000 approach to detail specifications and qualification approval procedures for each type of circuit is no longer always practical.

The procedures for the procurement of integrated circuits of standardized specification within the BS 9000 system are contained in BS 9400, which specifies a system for the release of approved circuits in accordance with detail specifications. Qualification approval of each type of circuit for each manufacturer is obtained by demonstration of the conformity of the product to the detail specification, and such approvals are published in PD 9002.

Very many of the processes in the manufacture of integrated circuits on a particular production line are common, although the resulting circuits may have widely differing electrical functions and characteristics. Many of the on-line quality control inspections for these common processes use standard test procedures such as those specified in the groups B, C and D inspection tables of detail specifications prepared in accordance with BS 9000. Thus, provided that the customer can be assured that these inspections are being applied to declared common processes, it is no longer necessary to specify nor repeat them for each individual type of integrated circuit.

In this British Standard, the concept of qualification approval of each type of circuit is replaced by the concept of the 'capability approval' of a manufacturer, i.e. the demonstration of the ability of a manufacturer to supply circuits of assessed quality in accordance with approved design rules, manufacturing processes and quality control procedures. Essentially, 'capability approval' is analogous to a manufacturer receiving qualification approval for a series of several structurally similar components.

The required capability approval procedures are given in 1.3. They require an approved capability manual to be prepared by each manufacturer for each technology offered.

This standard may be used in place of BS 9400 whenever its use is mutually agreed between manufacturer and customer (e.g. when only relatively small numbers of circuits are involved). However, catalogue items may also be released under BS 9450 capability approval procedures.

Figure 1 shows a representation of the salient features of the BS 9000 system as adapted and extended to cover the situation where the customer is the initial activator in the requirements for integrated circuits which he requires for his equipment or system applications. This modified system starts with the same basic requirements for the initial approval of the manufacturer as given in BS 9000, but in place of qualification approval the manufacturer obtains capability approval. For capability approval, full use is made of the on-line certification and approval of common processes such as those covered by groups B, C and D inspection so that any products made under such disciplines do not require further assessment of these features. The assessment of circuits produced for customer requirements then resolve into the quality conformity inspection of the electrical characteristics and performance, such as those covered by group A inspection.

The group A inspections which are specific to type have to be dependent on the requirements of the customer who has the initial responsibility for specifying them in terms of their electrical functions and characteristics. The customer also has the responsibility for specifying the environmental and other inspections, with inspection levels and post-test end-point requirements, which are necessary for a particular application.

Figure 1 shows a more detailed breakdown of the various sections of this specification and the various stages in the approval of the manufacturer's capability and the guidance to be given to customers in the preparation of their detail specifications.

Figure 2 is a flow chart for the procurement and release of custom-built integrated circuits and shows the degree of involvement of BSI, the manufacturer, the supervising inspectorate and the customer.

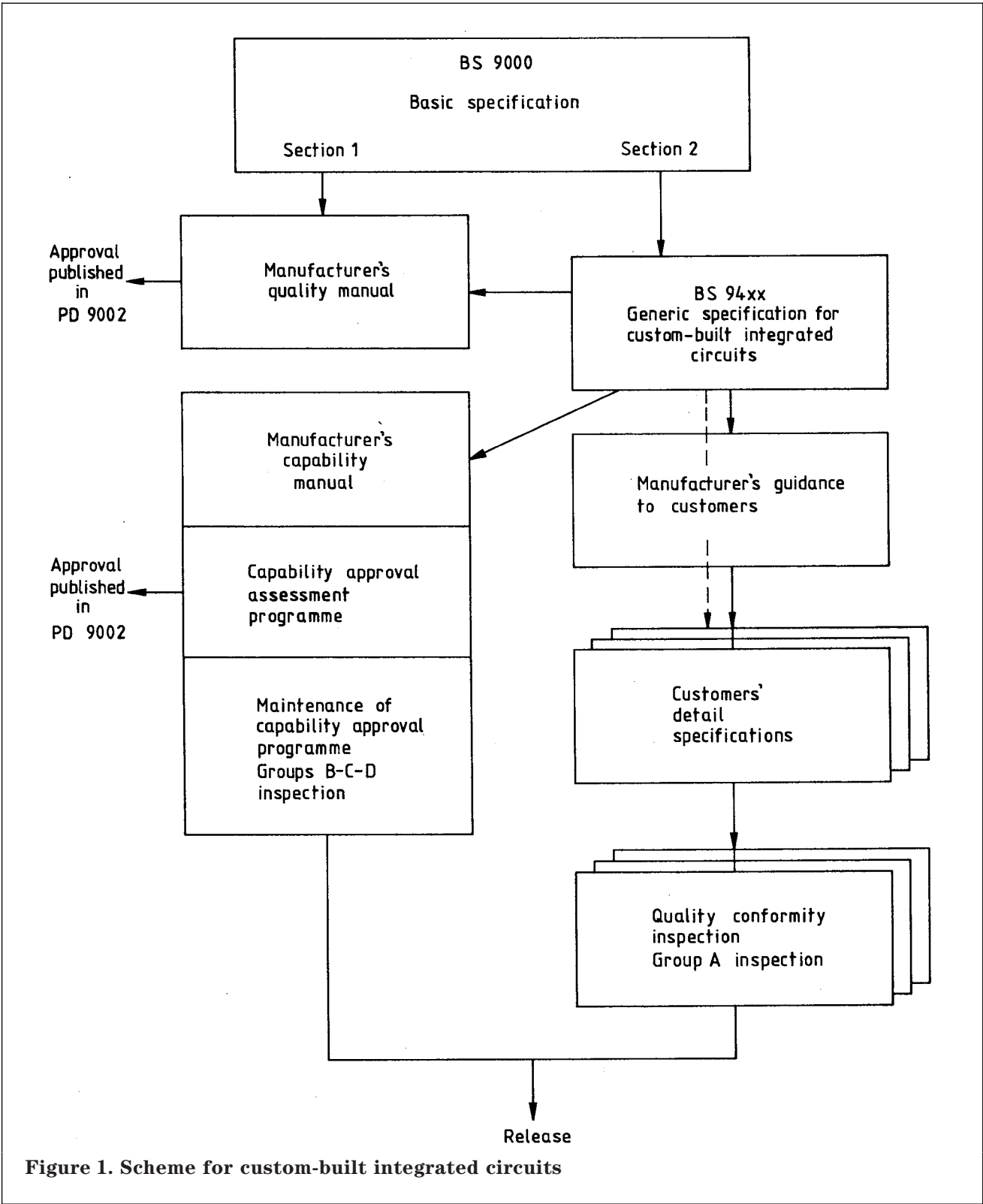
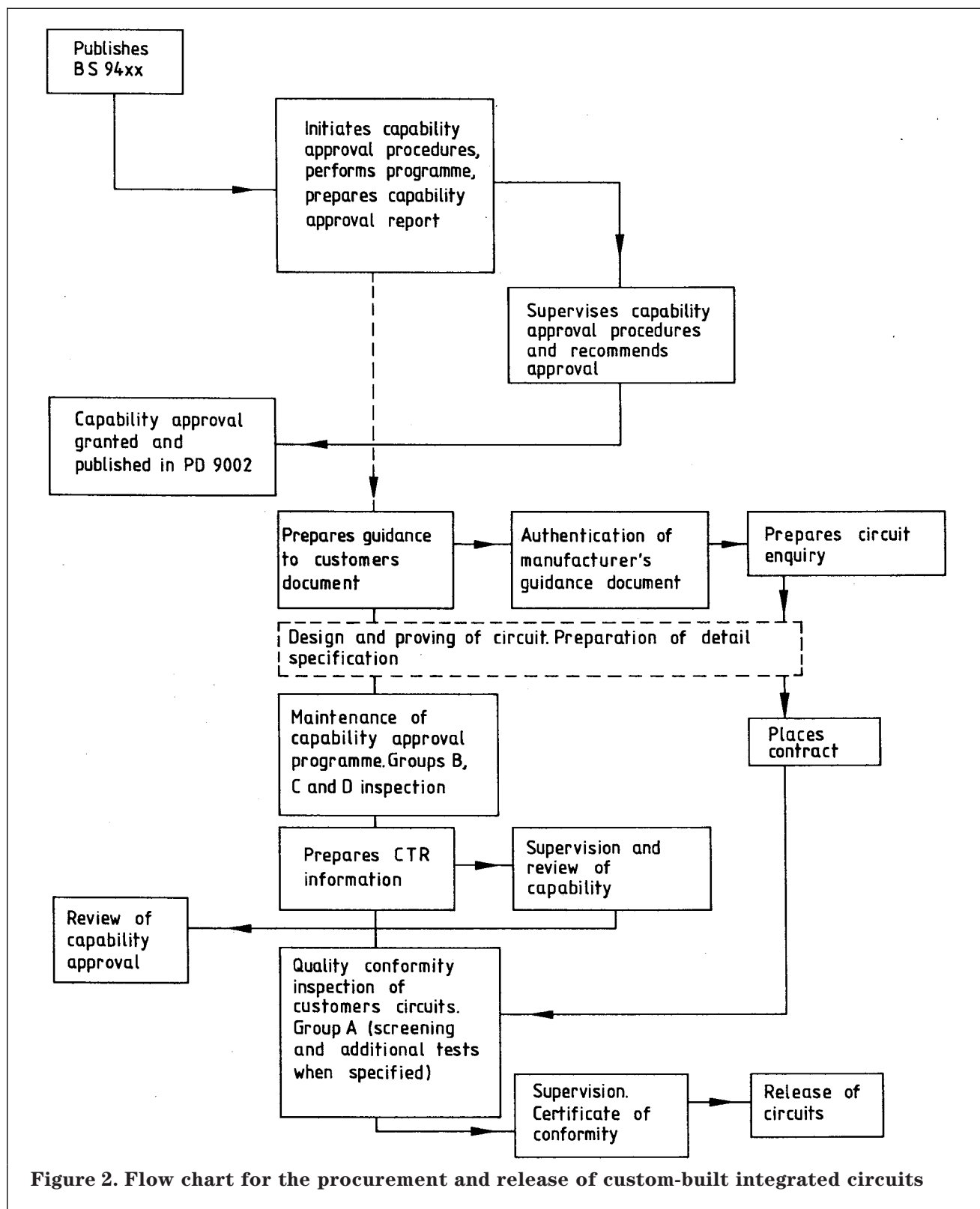


Figure 1. Scheme for custom-built integrated circuits



A brief summary of the principal elements of this standard is as follows:

Section 1. Principles and requirements

1.1 General matters

This material is taken from BS 9400, with additions.

1.2 Test procedures

These are derived from BS 9400, with additions. They conform to BS 9400, but are amended or extended to cover the requirements of capability approval, particularly for the film and hybrid technologies.

1.3 Capability approval and maintenance procedures

This material is additional to the principles given in BS 9000 : Part 1 and is in accordance with the general principles of section three of BS 9000 : Part 1 : 1989. Additional information is given in the following clauses of this standard:

- 1.3.2** Capability assessment
- 1.3.3** Description of capability : Capability manual
- 1.3.4** Programme for initial capability approval and extensions
- 1.3.5** Performance of capability approval programme
- 1.3.6** Abstract of description of capability
- 1.3.7** Maintenance of capability approval
- 1.3.8** Inspection requirements for maintenance of capability
- 1.3.9** Capability approval report
- 1.3.10** Review, suspension and withdrawal of capability approval
- 1.4** Inspection in accordance with the customer's detail specification

Section 2. Guidance on the preparation of customers' detail specifications

This section follows the same principles as those given in BS 9400 but they are modified to reflect the customers' initiation of specifications.

Section 3. Recommendations for manufacturer's guidance to customers

This section is supplementary to BS 9000 : Part 1 : 1989, and lists the minimum information necessary for the guidance of customers in the preparation of their enquiries and the preparation of their specifications. It is essential that the data included conforms to the specifications and other information contained in the manufacturer's approved capability manual.

The guidance listed in section 3 informs the customer of the range of technologies, circuit design rules, methods of connection and packaging, inspection facilities etc. which a manufacturer is able to offer, in order to assist a customer to assess the suitability of a particular capability to a particular application requirement.

Section 1. Principles and requirements

1.1 General matters

1.1.1 Scope

This standard forms part of the BS 9000 series and is to be read in conjunction with BS 9400 and with those standards referred to therein.

This standard specifies the approval procedure for integrated circuits, as defined in **1.1.3**, which are specifically ordered, designed, produced, tested and supplied to customer procurement requirements under the disciplines declared within the manufacturer's capability approval. In addition to the terms, definitions, symbols, test methods and other material already published in BS 9400, it gives supplementary information and requirements necessary to implement fully such detail specifications and procurement documents when prepared by customers using this system.

NOTE. The requirements of this standard diverge from those of BS 9400 in that best use is made of on-line qualification of common processes and procedures of inspection of structurally similar features, so that no further qualification approval of individual types of integrated circuit is necessary.

The manufacturer is required to declare to the supervising inspectorate his technology and the extent of his product capability and the means of assessing his ability to meet his declared capability, both initially and on a continuous basis.

Schedules of tests and inspections are given herein to be selected and declared by the manufacturer as appropriate for his technology and range of products.

This standard also includes, in section two and section three, two guidance documents, namely:

- a) general guidance to the customer on the preparation of detail specifications.
- b) manufacturer's guidance to customers on the preparation of detail specifications.

1.1.2 Normative references

This British Standard incorporates, by dated or undated reference, provisions from other publications. These normative references are made at the appropriate places in the text and the cited publications are listed on page 142. For dated references, only the edition cited applies; any subsequent amendments to, or revisions of the cited publication apply to this British Standard only when incorporated in the reference by amendment or revision. For undated references, the latest edition of the cited publication applies, together with any amendments.

1.1.3 Definitions

For the purposes of this British Standard, the definitions given in BS 4727, BS 9300 and in BS 9400 apply, together with the following.

1.1.3.1 General terms

1.1.3.1.1 microelectronics

The concept of the construction and use of highly miniaturized electronic circuits.

1.1.3.1.2 microcircuit

A single microelectronic device having a high density of circuit element and/or component equivalents.

NOTE. A microcircuit may be a micro-assembly or an integrated (micro) circuit.

1.1.3.1.3 integrated (micro) circuit

A microcircuit in which a number of circuit elements is inseparably associated and electrically interconnected such that for the purposes of specification and testing and commerce and maintenance, it is considered indivisible.

NOTE 1. For this definition, a circuit element is a constituent of a circuit that has neither an envelope nor external connection and is neither specified nor sold as a separate item.

NOTE 2. Where no misunderstanding is possible, the term integrated microcircuit may be abbreviated to integrated circuit, and is so used throughout this standard.

NOTE 3. Further qualifying terms may be used to describe the technique used in the manufacture of a specific integrated circuit. The following are examples of the use of qualifying terms:

- semiconductor monolithic integrated circuit (see **1.1.3.1.8**)
- semiconductor multi-chip integrated circuit (see **1.1.3.1.13**)
- thin film integrated circuit (see **1.1.3.1.9**)
- thick film integrated circuit (see **1.1.3.1.10**)
- film hybrid integrated circuit (see **1.1.3.1.20**)

1.1.3.1.4 micro-assembly

A microcircuit consisting of various components and/or integrated circuits which are constructed separately and which can be tested before being assembled and packaged.

NOTE 1. For this definition a component has external connections and possibly an envelope as well and can be specified and sold as a separate item.

NOTE 2. Further qualifying terms may be used to describe the form of the components and/or the assembly technique used in the construction of the specified micro-assembly. The following are examples of the use of the qualifying terms:

- semiconductor multi-chip micro-assembly.
- discrete component micro-assembly.

1.1.3.1.5 custom-built integrated circuits

Integrated micro-circuits and micro-assemblies (as defined in **1.1.3.1.3** and **1.1.3.1.4**) and micro-modules (as defined in **1.1.3.1.6**) which are produced to customer requirements and which are designed, manufactured, tested and released in accordance with the procedures given in this standard.

1.1.3.1.6 micro-module

A microcircuit in which a number of components and/or integrated circuits are inseparably associated and electrically interconnected such that for the purposes of specification and testing and commerce and maintenance, it is considered indivisible.

NOTE. Where no misunderstanding is possible the prefix 'micro' may be omitted from the terms 'microcircuit', 'integrated microcircuit', 'micro-assembly' and 'micro-module' and is in general so omitted throughout this standard.

1.1.3.1.7 capability qualifying circuits (or components) (CQCs)

Circuits (or components) which are used for the demonstration of capability and the subsequent maintenance of capability in accordance with 1.3 of this specification.

NOTE. It will normally be necessary to use a range of CQCs to cover any one capability approval.

1.1.3.1.8 monolithic

A qualifying term for the technology of devices made out of a single piece of material.

1.1.3.1.9 thin-film

A qualifying term for the technology whereby circuit elements are formed by vacuum deposition, e.g. by evaporation, sublimation, sputtering or by related techniques.

1.1.3.1.10 thick-film

A qualifying term for the technology whereby circuit elements are formed by screen printing or by other related techniques.

1.1.3.1.11 die

A unit of monolithic semiconductor material containing an active device or circuit.

1.1.3.1.12 chip

An unencapsulated circuit or circuit element (also used as an alternative name for 'die').

1.1.3.1.13 multi-chip

A qualifying term for the technology whereby an integrated circuit is realized by the use of two or more active or passive chips mounted on a substrate.

1.1.3.1.14 flip-chip

A qualifying term for chips or dies which can be mounted face downwards on a conductor pattern.

1.1.3.1.15 beam-lead

A qualifying term for chips or dies having extended integral solid terminations which can be directly bonded to a substrate or header without the need for intermediary wires.

1.1.3.1.16 passive substrate

A substrate, without active elements, the function of which is predominantly mechanical and thermal. It can be constructed from insulating, conductive or semi-conductive material.

1.1.3.1.17 active substrate

A substrate with active elements and, in some cases, passive elements. It may be used to support other externally deposited or connected elements.

1.1.3.1.18 integral substrate package

A package in which the substrate forms an integral part of the package.

1.1.3.1.19 included substrate package

A package in which the substrate is mounted within the package and is connected to the terminations.

1.1.3.1.20 film hybrid

A qualifying term for an integrated structure in which a circuit is formed by combination of one or more substrate technologies, with or without integral component elements, or by the combination of any one of these with discrete components.

1.1.3.1.21 carrier A structure in which an incomplete integrated circuit or part of a circuit may be retained for ease of transportation, assembly and/or testing.

1.1.3.1.22 passive element

An element primarily contributing resistance, capacitance or inductance, or a combination of these, to a circuit function. Passive elements may be realized on or in passive or active substrates.

Examples are resistors, capacitors, inductors, filters.

1.1.3.1.23 active element

An element primarily contributing electrical rectification or gain to a circuit function. Active elements may also be used to contribute resistance and capacitance to a circuit function, or to convert externally applied energy from one form to another.

Examples are diodes, transistors, semiconductor integrated circuits, light-sensing and light-emitting semiconductor devices.

1.1.3.1.24 surface acoustic wave device (SAW)

A device employing acoustic waves localized close to the surface of a piezo-electric substrate.

1.1.3.2 Terms related to integrated circuits and their functions**1.1.3.2.1 digital circuit**

A circuit which operates with digital signals at the input(s) and output(s) and which is characterized by the inter-relationships between the states of the digital signals at the input and output terminals.

See also 1.1.3.3.1.

1.1.3.2.2 analogue integrated circuit

A circuit for which a continuous relationship (either linear or non-linear) exists between its input and output signals.

1.1.3.2.3 attenuator

A network designated for insertion in a line, or between other networks, to introduce a loss without introducing distortion and normally without introducing impedance change.

1.1.3.2.4 amplifier

A device in which an input signal controls a local source of power in such a way as to produce an output which bears some desired relationship to and is generally greater than, the input signal.

1.1.3.2.5 differential amplifier

An amplifier the output signal(s) of which correspond(s) to the instantaneous algebraic difference between two input signals.

1.1.3.2.6 summing amplifier

An amplifier the output signal(s) of which correspond(s) to the instantaneous algebraic sum of two or more input signals.

1.1.3.2.7 filter

A circuit which delivers an output signal having a determined frequency-dependent relationship to the input signal.

1.1.3.2.8 modulator

A circuit which delivers an output signal in which some characteristics of one input signal have been impressed upon some characteristics of another input signal.

1.1.3.2.9 demodulator

A circuit which performs a function inverse to that of a modulator.

1.1.3.2.10 delay network

A line or network specifically designed to introduce a desired delay in the transmission of a signal.

1.1.3.2.11 frequency multiplier/divider

A circuit which delivers an output signal, the frequencies of which have determined integral multiples or submultiples of those of the input signal.

1.1.3.3 General descriptive terms**1.1.3.3.1 digital signal**

A physical quantity which may take one of a given number of discrete values (states).

NOTE. In practice each discrete value falls within a range between defined limits.

1.1.3.3.2 worst case conditions (for a single characteristic)

The values of the applied conditions which individually are chosen from within a specified range and together produce the most unfavourable value for a considered characteristic.

NOTE. The worst case conditions for different characteristics may be different.

1.1.3.3.3 limiting conditions of use (absolute limiting ratings)

The values of electrical, thermal, mechanical or environmental quantities assigned by the manufacturer which establish a limiting capability or a limiting condition beyond which damage to the integrated circuit may occur.

1.1.3.3.4 recommended conditions of use

The values of electrical, thermal, mechanical or environmental quantities within which correct operation should be achieved.

1.1.3.4 Terms for the characteristics of digital circuits

NOTE. The following terms may be qualified by additional adjectives such as expander, trigger, preset, clear, etc.

1.1.3.4.1 HIGH state input minimum voltage

The minimum input voltage in the HIGH state applied to one or more inputs which ensures correct operation of the digital circuit.

1.1.3.4.2 LOW state input maximum voltage

The maximum input voltage in the LOW state applied to one or more inputs which ensures correct operation of the digital circuit.

1.1.3.4.3 LOW state output maximum voltage

The maximum voltage of the output in the LOW state for specified output current.

1.1.3.4.4 HIGH state output minimum voltage

The minimum voltage of the output in the HIGH state for specified output current.

1.1.3.4.5 HIGH state static voltage noise margin

The difference between the HIGH state output minimum voltage and the HIGH state input minimum voltage.

1.1.3.4.6 LOW state static voltage noise margin

The difference between the LOW state input maximum voltage and the LOW state output maximum voltage.

1.1.3.4.7 static voltage noise margin

The smaller of the HIGH state and the LOW state static voltage noise margins.

1.1.3.4.8 HIGH state input current

The current measured at an input terminal when a specified HIGH state voltage is applied to that input.

1.1.3.4.9 LOW state input current

The current measured at an input terminal when a specified LOW state voltage is applied to that input.

1.1.3.4.10 HIGH state output current

The forced current measured at the output terminal which will guarantee a specified HIGH state output voltage.

1.1.3.4.11 LOW state output current

The forced current measured at the output terminal which will guarantee a specified LOW state output voltage.

1.1.3.4.12 input loading factor (of a bipolar circuit)

A factor which indicates the ratio of the input current of a specified input terminal to the input current of a particular integrated circuit which is chosen as a reference load.

1.1.3.4.13 output loading capability (of bipolar device)

A factor which indicates the ratio of the maximum output current of a specified output terminal to the input current of a particular integrated circuit which is chosen as a reference load.

NOTE. The reference load is chosen so that the input loading factor and the output loading capability become whole (integral) numbers.

1.1.3.4.14 HIGH to LOW state output delay time

The time interval between specified reference points on the input and on the output waveforms when the output is going to the LOW state.

1.1.3.4.15 HIGH to LOW state transition time

The time interval between specified reference points on the output waveform when the output is going to the LOW state.

1.1.3.4.16 HIGH to LOW state propagation time

The time interval between specified reference points on the input and on the output waveforms when the output is going to the LOW state and when the device is driven and loaded by like devices.

1.1.3.4.17 LOW to HIGH state output delay time

The time interval between specified reference points on the input and on the output waveforms when the output is going to the HIGH state.

1.1.3.4.18 LOW to HIGH state transition time

The time interval between specified reference points on the output waveform when the output is going to the HIGH state.

1.1.3.4.19 LOW to HIGH state propagation time

The time interval between specified reference points on the input and on the output waveforms when the output is going to the HIGH state and when the device is driven and loaded by like devices.

1.1.3.5 Terms for the characteristics of analogue circuits**1.1.3.5.1 input off-set voltage**

The continuous (direct) voltage required to be applied between the input terminals of a differential amplifier for specified input and output loading circuits to cause the output voltage to attain a specified level, usually zero.

NOTE. When the amplifier has two symmetrical outputs, the specified voltage refers to the difference in voltage between these outputs.

1.1.3.5.2 input off-set current

The continuous (direct) current which has a value equal to the difference in the currents flowing in the two input terminals which will cause the output voltage to attain a specified level, usually zero, under stated operating conditions, in particular the input and output loading circuits.

NOTE. When the amplifier has two symmetrical outputs, the specified voltage refers to the difference in voltage between these outputs.

1.1.3.5.3 input bias current

a) (of a differential amplifier). The average of the two input currents when the output voltage is at a specified level, usually zero.

b) (of a single input amplifier). The input current when the output voltage is at a specified level, usually zero.

1.1.3.5.4 common-mode voltage amplification (of a differential input linear amplifier)

The ratio of the change in magnitude of the output voltage to the change in magnitude of the input voltage applied equally and in phase to each input terminal under specified conditions.

1.1.3.5.5 differential-mode voltage amplification (of a differential input linear amplifier)

The ratio of the change in magnitude of the output voltage to the change in the magnitude of the differential input voltage under specified conditions.

1.1.3.5.6 common-mode rejection ratio (of a differential input linear amplifier)

The ratio of the differential-mode voltage amplification to the common-mode voltage amplification, each under the same specified conditions.

NOTE. In practical cases, the common-mode rejection ratio can be derived from a measurement of common-mode amplification that uses a higher value of input signal than that used for measuring the differential-mode amplification. This usually gives a figure equal to, or worse than, that given by the theoretical situation of equal input signals.

1.1.3.5.7 (equivalent) input drift

The change in the input d.c. voltage or d.c. current (but with reversed sign) necessary to compensate for a change in output d.c. voltage or d.c. current, caused by a specified change of supply voltage, or time or temperature or other environmental conditions.

1.1.3.5.8 temperature coefficient of input off-set voltage

The ratio of the change of input off-set voltage to the change of operating temperature causing it, other conditions remaining constant.

1.1.3.5.9 temperature coefficient of input off-set current

The ratio of the change of input off-set voltage to the change of operating temperature causing it, other conditions remaining constant.

1.1.3.5.10 common-mode input voltage range

The range of voltage between the input terminals, strapped together, and the reference or earth terminal which, if exceeded, may cause the amplifier to cease to function within its specification.

1.1.3.5.11 differential-mode input voltage range

The range of voltage between the input terminals which, if exceeded, may cause the amplifier to cease to function within its specification.

1.1.3.5.12 output voltage range

The maximum peak-to-peak output voltage which can be obtained with specified amplitude distortion when the quiescent d.c. output voltage is set to a specified reference level.

1.1.3.5.13 noise

The unwanted output signal generated by the circuit, not coherent with the input signal.

NOTE. For linear circuits this is normally referred to the input as an equivalent input signal under specified conditions.

1.1.3.5.14 input terminal impedance

The impedance between any input terminal and the reference terminal with other input terminals isolated, or with specified connections, and under specified conditions.

1.1.3.5.15 *signal input impedance*

The impedance between the signal terminals at a specified frequency under specified conditions.

1.1.3.5.16 *common-mode input impedance*

The impedance between the signal terminals, connected together by a capacitor having a small impedance at the test frequency, and the reference terminal, under specified conditions.

1.1.3.6 *Terms for internal visual inspection***1.1.3.6.1** *active area*

In SAW devices, the area which includes the interdigitated pattern carrying the acoustic wave.

1.1.3.6.2 *active circuit area*

All areas of functional circuit elements, operating metallization or any connected combinations thereof on the top or bottom surfaces of the substrate.

1.1.3.6.3 *active finger*

In SAW devices, a finger which extends into the overlap region with at least one adjacent finger of opposite polarity.

1.1.3.6.4 *busbar*

In SAW devices, a relatively broad strip of metallization on to which are connected fingers of the same polarity.

1.1.3.6.5 *composite metallization (for conductors)*

Two or more layers of metal or any other material used for interconnections that are not isolated from each other by a grown or deposited insulating material.

NOTE. The term 'underlying metal' refers to any layer below the top layer of metal.

1.1.3.6.6 *cosmetic scratch*

A shallow scratch which may extend completely across the metallization and which neither exposes or damages underlying layers, nor laterally displaces metallization beyond the edge of the conductor owing to mechanical deformation.

1.1.3.6.7 *dummy finger*

In SAW devices, a finger which terminates before overlapping with an adjacent finger of opposite polarity.

1.1.3.6.8 *edge metallization*

Metallization on a substrate that extends over an edge, e.g. for interlayer connection purposes or to connect metal on opposing faces.

1.1.3.6.9 *foreign material*

Any material not used in the manufacture of the microcircuit, or any in-built material that is displaced from its original or intended position within the microcircuit package.

NOTE. Conductive foreign material is defined as any substance that appears opaque under those conditions of lighting and magnification used in routine visual inspection.

1.1.3.6.10 *glassivation*

The top layer(s) of transparent insulating material that cover(s) the active area of a semiconductor die, including integral metallization, but not including bonding pads.

NOTE. 'Crazing' is the presence of minute cracks in the glassivation layer. Particles are considered to be embedded in the glassivation if there is evidence of colour fringing around them.

1.1.3.6.11 *protective coating*

A layer of insulating material applied over the circuit elements for the purpose of mechanical protection and prevention of contamination.

1.1.3.6.12 *insulating layer*

A layer used for electrical isolation of multilevel film, or to protect top level conductive and/or resistive material layers.

1.1.3.6.13 *kerf*

The slit or cut made by a material-removing instrument (such as a laser or abrasive trimmer).

1.1.3.6.14 *lead-in*

In SAW devices, a relatively broad strip of metallization which extends from the busbar and on to which a wire may be bonded.

1.1.3.6.15 *multilevel metallization (for conductors)*

Two or more layers of metal, or any other material used for interconnections, that are isolated from each other by a layer of intermediary insulation material.

1.1.3.6.16 *multilayer metallization (composite metallization)* Two or more layers of metal, or any other material used for inter-connections, that are not isolated from each other by a layer of intermediary insulation material.

1.1.3.6.17 *operating metallization (for conductors)*

All metal (or any other material) used for inter-connection, with the exception of the metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads and identification markings.

1.1.3.6.18 *passivation*

The silicon oxide, silicon nitride, or other insulating material that is grown or deposited directly on the die prior to the deposition of metal.

1.1.3.6.19 *rebonds*

A second bonding, either in the sense of:

- a) the replacement of an original bond wire between two substrate pads or between a substrate pad and a package;

NOTE. In this case the original wire has either been removed, leaving the welded portion of the bond attached to the pad or terminal, or it has failed to adhere at the first bonding attempt.
or of

- b) the clamping of the free end of a wire.

1.1.3.6.20 scratch

Any tearing defect in the surface of the metallization.

1.1.3.6.21 substrate

The supporting structural material into and/or upon which the passivation, metallization, and circuit elements are placed.

1.1.3.6.22 through-hole metallization

The metallization that electrically connects two or more layers of multilevel metallization via holes in intermediary isolation layers or in the substrate itself.

1.1.3.6.23 transducer

In SAW devices, an array of parallel metal fingers of alternating polarity separated by gaps of approximately the same width as the metal fingers.

1.1.3.6.24 void

Any defect in the metallization not caused by a scratch where underlying dielectric, passivation or substrate is visible.

1.1.4 Letter symbols, signs and abbreviations

1.1.4.1 The letter symbols, signs and abbreviations shall be in accordance with BS 3363.

In addition, for the purpose of digital integrated circuit specifications, the letter symbols given in 1.1.4.2 and 1.1.4.3 shall be used.

NOTE. The following abbreviations are in common use:
DTL : Diode transistor logic;
RTL : Resistor transistor logic;
TTL : Transistor transistor logic;
ECL : Emitter coupled logic.

1.1.4.2 Voltage and current symbols shall be as follows:

- first subscript: terminal identification
- second subscript: HIGH or LOW state
- third subscript: further qualification if required

This sequence is illustrated in table 1.

Table 1. Voltage and current symbols for digital integrated circuits				
State Output	Voltages		Currents	
	Input	Output	Input	Output
HIGH	V _{IH}	V _{OH}	I _{IH}	I _{OH}
LOW	V _{IL}	V _{OL}	I _{IH}	I _{OL}
NOTE. Particular values of these quantities may be denoted by further subscripts (1), (2), etc. Limiting values of these quantities may be qualified by the addition of subscripts 'min.' and 'max.'.				

1.1.4.3 The subscript sequence for time symbols is as follows:

- first subscript: type of time interval;
- second and third subscripts: change of state of output;
- P is used for propagation time;
- D is used for delay time;
- T is used for transition time.

Example:

- t_{PLH} denotes LOW to HIGH state output propagation time.
- t_{PHL} denotes HIGH to LOW state output propagation time.
- Limiting values of the above quantities may be qualified by addition of subscripts 'min' and 'max'.
- NOTE. The standard symbol for pulse duration, t_p , may be qualified by the addition of subscript words, e.g. clock, count, etc.

1.1.5 Graphical symbols

The graphical symbols to be used on all integrated circuit specifications shall be in accordance with BS 3939 and 1.1.5 of BS 9400.

1.1.6 Marking of the component and package

1.1.6.1 General

The following symbols or codes shall be marked on the device in the following order of preference as space permits:

- a) terminal identification (see 1.1.6.2).
- b) customer's type number or drawing number and, where applicable, issue. Alternatively, a colour code may be used (see 1.1.6.3 and 1.1.6.7).
- c) tolerance identification (see 1.1.6.8).
- d) factory identification code or manufacturer's name or trade mark (see 1.1.6.4).
- e) date code (see 1.1.6.5).
- f) British Standard detail specification number.

All the symbols and codes, except the terminal markings and colour band identification if used, shall also appear on the primary package, e.g. carton, box, plastics envelope etc., used as initial protection or wrapping for delivery. Where colour band identification is used on the device the manufacturer's type number shall appear on the primary package.

1.1.6.2 Terminal identification

The terminals or leads of integrated circuits shall be marked or identified in accordance with the specified outline as given in the detail specification.

1.1.6.3 Customer's type number (or colour code)

The marking of the customer's type number shall be in accordance with that given in the detail specification.

1.1.6.4 Factory identification code or manufacturer's name or trade mark

Where the certificate of conformity enables traceability to a manufacturer's factory, the manufacturer's name or trade mark is sufficient. In all other cases the factory identification code shall be used and shall be in accordance with PD 9002.

1.1.6.5 Date code

The date code shall be in accordance with 4.2 of BS 9000 : Part 7 : 1989.

1.1.6.6 Detail specification number

Each detail specification shall carry a distinguishing number made up of the number of this specification and a unique number (e.g. the customer's reference/drawing number) identifying the item to the agreed customer's specification (see also section 2 of this standard).

1.1.6.7 Colour code identification for type number

When specified in the detail specification, the colour code identification for type number shall be as specified in table 2. The number sequence shall be from left to right, the left being signified by either a wider band of colour or a placement of the colour group towards the left hand edge of the body. Two digit numbers shall be preceded by a zero.

1.1.6.8 Tolerance identification (where applicable)

When specified in the detail specification, the component tolerance shall be printed on the device package, e.g. by the use of letter codes in accordance with BS EN 60062.

Table 2. Colour code for identification number

Colour	Identification number
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Purple (violet)	7
Grey	8
White	9

1.1.7 Eligibility for release**1.1.7.1 General**

Integrated electronic circuits and micro-assemblies shall be eligible for submission for capability approval and release to BS 9450 if the procurement of materials and components and all stages of manufacture and test are undertaken at any BS 9450 approved manufacturing facility (except as allowed in 1.1.7.4).

1.1.7.2 Film and hybrid integrated circuits, micro-assemblies, micro-modules and microwave integrated circuits

NOTE. This also applies to part completed film and hybrid circuits supplied for subsequent processing.

1.1.7.2.1 Acceptable primary stages of manufacture are either:

- a) the production of the first conductive layer as an additive process to a substrate (e.g. conductive inks applied to an alumina or porcelain on steel or similar base); or
- b) the production of the first conductive pattern as a subtractive process to a suitably prepared substrate (e.g. removal of conductive material from a copper clad epoxide glass fabric, or similar, base).

Organic printed boards with mounted or deposited components shall only be released under BS 9450 if no one dimension exceeds 110 mm. Unpopulated organic printed boards may not be released under BS 9450.

1.1.7.2.2 All stages of manufacture, up to and including the finished product, are not limited by size or complexity (other than by the constraints given in 1.1.7.2.1) but shall be restricted to practices and procedures covered by this specification and declarations within the approved manufacturer's capability manual.

1.1.7.3 Monolithic and multichip semiconductor integrated circuits whether released as wafers, bare dice or packaged components**1.1.7.3.1 Acceptable primary stages of manufacture are:**

- a) for bipolar integral circuits, the first process which changes the mono-crystalline semiconductor material from being either wholly p-type or wholly n-type.
- b) for MOS circuits, the first oxidation of the semiconductor material.
- c) for integrated circuits incorporating bulk effect devices, the first process which changes the monocrystalline semiconductor to give the required doping profile.

1.1.7.3.2 All stages of manufacture, up to and including the finished product, are not limited by size or complexity but shall be restricted to practices and procedures covered by this specification and declarations within the approved manufacturer's capability manual.

1.1.7.4 Use of non-approved subcontractors

Should an approved manufacturer wish to subcontract operations corresponding to the primary stage of processing or any subsequent stages to an unapproved manufacturer, he shall meet the requirements of **3.2.5** of BS 9000 : Part 6 : 1989 and, additionally, ensure the conditions given in a) to e) are met.

Subcontracting is prohibited when the approved manufacturer intends to release wafers, bare die or part completed film and hybrid integrated circuits.

a) The subcontracted operation shall conform to **1.1.7.2.1** and **1.1.7.3.2** as follows:

- 1) the subcontracted manufacture may be either the preparation of the substrate prior to discrete component assembly/diffusion processes (as in **1.1.7.2.1a**) and **1.1.7.3**), or the subsequent assembly of the device;
- 2) if the primary stage of manufacture conforms to **1.1.7.2.1b**), the substrate shall be released under BS EN 123000 or supplied under equivalent disciplines agreed with the NSI.

b) The supervising inspectorate shall be satisfied that the chief inspector of the certifying manufacturer has been provided with the full quality assurance and inspection documentation from the non-approved facility, and that he had the responsibility for inspection of the work and the inspection arrangements there. Such documentation shall include the inspection records for each sample of the product that undergoes inspection.

c) The chief inspector shall be provided with the production line process charts, the defined inspection points, the inspection requirements at each stage and the quality control requirements, together with the procedures for the transfer of the parts from the place of manufacture to the certifying manufacturer. The supervising inspectorate shall be informed and have access to this documentation and be able to verify the application of these requirements.

d) Any changes in inspection requirements and manufacturing procedures shall be reported back to the approved manufacturer's chief inspector who is certifying the components. These changes shall be declared on the document accompanying the transferred parts. The significant changes shall be reported by the approved manufacturer's chief inspector to the supervising inspectorate.

e) The approved manufacturer shall perform the acceptance tests required by the detail specification for the component he is certifying. He can perform the acceptance tests in a non-approved facility provided that this facility is supervised by the supervising inspectorate. Acceptance tests can be sub-contracted to approved test laboratories.

1.1.8 Structural similarity

The concept of structural similarity is not required when capability approval is used, as the relevant requirements are covered in the manufacturer's capability approval.

1.1.9 Delayed delivery

Released lots that have been in store for more than three years shall undergo and satisfy group A and group B solderability tests before delivery. No further re-testing is needed for lots delivered within three years of a re-test. When releasing bare dice, the wire bond test in group B shall be satisfied.

1.1.10 Supplementary procedure for qualification approval

Not applicable.

1.1.11 Certified test records (CTRs)

The information to be present in certified test records shall be as stated in table 30 of this standard.

Manufacturers are free, but not obliged, to give additional CTR information beyond that required in table 30, but where this additional information is derived from sources other than acceptance procedures this shall be stated.

1.1.12 Standard ratings and characteristics

1.1.12.1 General

The values for ratings and characteristics shall be chosen from the list given below. If additional items are included in a detail specification, the values and conditions under which they apply shall be stated. Any interdependence of ratings and characteristics and any limiting conditions of use shall be stated.

1.1.12.2 Supply terminal voltages

Preferred nominal values are 3.0 V, 4.0 V, 5.0 V, 9.0 V, 12 V, 24 V, 30 V and 48 V. Preferred tolerances are 5 %, 10 % and 20 %.

NOTE. The tolerances above and below the nominal value need not necessarily be the same.

1.1.12.3 Test temperatures

−55 °C, −40 °C, −25 °C, 0 °C, + 25 °C, + 70 °C, + 85 °C, + 100 °C, + 125 °C, and + 150 °C.

1.1.12.4 Preferred temperature ranges

- a) −55 °C to + 125 °C;
- b) −40 °C to + 100 °C;
- c) 0 °C to + 70 °C.

1.1.13 Unchecked parameters

Not applicable.

1.1.14 Procedure to be followed in the event of failure at groups C and D inspection

The procedure given in **12.4** of BS 9000 : Part 6 : 1989 shall be applied.

1.1.15 Ordering information

Not applicable.

1.1.16 Release prior to completion of group B tests

Not applicable.

1.1.17 Supplementary procedure for reduced inspection

The procedure in clause 2 of BS 9000 : Part 7 : 1989 shall be applied.

1.1.18 Supplementary procedure for general application category components

Not applicable.

1.1.19 Rework

Rework shall only be permitted within the procedures declared in the manufacturer's approved capability manual. Such procedures shall demonstrate, to the satisfaction of the supervising inspectorate, that the subsequent reliability of the integrated circuit as supplied to the customer is not thereby impaired.

A customer may prohibit rework on circuits to be supplied for a particular contract.

Reworked packages which have been resealed shall be subjected to and pass the 'Rapid change of temperature', 'Fine leak detection' and 'Gross leak detection' tests specified in 1.2.7.14, 1.2.7.15.1 and 1.2.7.15.2 respectively.

Where circuits have been directly embedded in hard plastic encapsulants, e.g. by moulding, casting, or dipping, using epoxy or silicone resins, no rework shall be permitted.

Replacement of defective added components and/or defective wire bonds shall be permitted within the following limits, unless otherwise restricted in the manufacturer's approved capability manual.

a) Scratched, open or discontinuous metallization paths or conductor patterns on semiconductor material shall not be reworked.

Film conductors may be repaired by the attachment of conducting links provided that the number and type of joints so made conform to the requirements of the manufacturer's approved capability manual.

b) Not more than one attempt shall be permitted to reconnect a wire or component termination at any pad or post. No reconnections shall be permitted directly over an area where the metallization of the intended bond area has been lifted.

c) On a semiconductor die, no ball bond on top of another shall be permitted.

d) Encapsulated components which have been removed from a defective substrate may be re-used on another substrate provided that they satisfactorily fulfil the requirements of the approved electrical and physical tests prior to re-use. Such components shall not be re-used more than once.

In the case of hermetically sealed components which have been removed, all glass-to-metal seals shall be inspected for cracks before re-use.

e) If a component which has been soldered is removed, not more than two solder reflow cycles shall be applied to the conductor or pad involved, whether or not a replacement component is to be re-connected.

f) Semiconductor dies which have been bonded shall not be removed and re-bonded. However dies which have been attached to headers or substrates may be detached and re-used provided that it is demonstrated that the method of attachment allows this to be done without impairing the subsequent reliability of the complete integrated circuit.

1.1.20 Sampling procedures

At the discretion of the manufacturer and with the agreement of the NSI, the manufacturer may use either LTPDs (see BS 6001) or AQLs. To ensure acceptable correlation between AQL and LTPD sampling plans, the maximum acceptance number should not be greater than four. The equivalent sampling plans are given in table 3.

Table 3. Equivalent values for sampling plans

AQL	LTDP
0.10	0.7
0.15	1.0
0.25	2.0
0.40	3
0.65	5
1.0	7
1.5	10
2.5	20
4.0	30
65	50

1.1.21 Authority of documents

In accordance with clause 7 of BS 9000 : Part 1 : 1989, where any omissions conflicts, ambiguities or inconsistencies occur, documents shall rank in the following order of authority:

a) the agreed customer/manufacturer detail specification prepared in accordance with section two.

b) this standard.

c) BS 9400 and other applicable generic specifications, e.g. BS 9300 etc.

d) BS 9000 and other standards to which reference is made.

1.2 Test procedures

1.2.1 General

The test and measurement methods and procedures given in 1.2.2 to 1.2.12 inclusive shall be applied as follows:

- a) when they are required to verify facilities or assessment tests included as part of a manufacturer's capability assessment programme; or
- b) when they are required to perform tests or measurements contained in a customer's detail specification.

A manufacturer is free to specify which tests are offered as part of his declared production capability, and which are specified in his capability manual (see also 1.2.2.2).

Tests and measurement procedures shall be applied in accordance with the inspection requirements of BS 9000.

1.2.2 Standard conditions for testing

1.2.2.1 General

Unless otherwise stated, all tests shall be performed under standard atmospheric conditions for testing, as specified in BS EN 60068-1.

Before the measurements are performed, the integrated circuit shall be stored at the measuring temperature for a time sufficient to allow the entire circuit to reach this temperature. The recovery period specified after conditioning is sufficient for this purpose.

When measurements are made at a temperature other than that specified, the ambient temperature during the measurement shall be recorded and the results shall be corrected, where necessary, to the specified temperature.

During measurements, the integrated circuit shall not be exposed to draughts or direct sun-rays, and shall be protected from unintentional radioactive and electromagnetic radiations.

1.2.2.2 Alternative test methods

The measurements and conditions specified are not the only methods which can be used but the supervising inspector shall be satisfied that other methods, including pulse methods, and/or conditions of measurements employed will give results compatible with the methods and/or conditions specified in this standard and in the relevant detail specification. By 'compatible' is meant that the value of the characteristic established by such other methods will fall within the specified limits when measured by the specified method and under the specified conditions.

1.2.2.3 Safety aspects

1.2.2.3.1 General

An employer is responsible, under the Health and Safety at Work etc. Act 1974, for ensuring the health and safety of employees.

To minimize possible hazards which may arise from performing tests contained in this standard and related documents, the precautions listed in 1.2.2.3.2 to 1.2.2.3.7 are recommended. These recommendations are not necessarily complete in their coverage and are given for guidance only.

1.2.2.3.2 Toxic vapour and poisonous residues

When performing the following tests, care should be taken to ensure that any toxic vapours or poisonous residues which may be liberated, are not inhaled or directly handled by personnel working in, or adjacent to, the test area(s), and that they are disposed of in a safe manner.

- 1.2.7.2 Cold for non-heat dissipating specimen with sudden change of temperature
- 1.2.7.3 Dry heat for non heat dissipating specimen with sudden change of temperature
- 1.2.7.4 High temperature storage
- 1.2.7.5 Damp heat, steady state
- 1.2.7.6 Damp heat, cyclic
- 1.2.7.7 Shock
- 1.2.7.8 Bump
- 1.2.7.9 Vibration
- 1.2.7.10 Acceleration steady state
- 1.2.7.11 Mould growth
- 1.2.7.13 Low air pressure
- 1.2.7.14 Rapid change of temperature
- 1.2.7.15 Sealing
- 1.2.7.16 Soldering
- 1.2.7.17 Robustness of termination
- 1.2.7.18 Flammability
- 1.2.7.19 Resistance to solvents
- 1.2.7.20 Rapid change of temperature, two-bath method
- 1.2.7.21 Damp heat steady state with bias
- 1.2.7.22 Thermal intermittence test
- 1.2.8 Electrical endurance test procedures
- 1.2.9.3 Damp heat accelerated test for long term changes in resistance and interconductor leakage
- 1.2.10 Screening test procedures

1.2.2.3.3 Fire

Flammability tests should be performed in a hooded fume cupboard (or other suitable container) lined with fire-resistant materials(s) from which the gaseous products of combustion are extracted to a safe dispersal point.

1.2.2.3.4 Hot equipment

Heated equipment used for tests (e.g. ovens, cycling chambers solder baths,) should be suitably protected to minimize the risk of accidental burns and incorporate devices to prevent overheating in the event of normal control system failure.

1.2.2.3.5 Radiation

The storage and handling of radioactive materials used for leak tests should conform to the relevant safety standards.

1.2.2.3.6 Mechanical

Pressurized or evacuated containers used for leak tests should be subject to regular inspection to minimize explosion/implosion risks and, where appropriate, should be tested in accordance with statutory regulations.

1.2.2.3.7 Electrical test methods (digital and analogue circuits)

It is assumed that personnel carrying out any of the electrical tests described in 1.2.5 of this standard will be familiar with basic safety precautions to avoid those hazards from electrical shock which are inherent in any test involving the use of power supplies which may be driven from the a.c. mains. Care should be taken to avoid accidental contact with supply voltages which are not in the 'low-voltage' category. Circuits can operate with supply voltages up to 100 V. The existence of this hazard can be verified from the conditions specified for the circuit under test.

Attention is drawn to the possibility of the following additional hazards arising, particularly under fault conditions, either within the circuit itself, or in the ancillary test equipment.

a) Toxic vapours

These might arise if a device overheats, and their effect would depend principally on the type of encapsulation used, and the chemicals used in passivation layers on the circuit or in the chip mounting.

b) Explosions

This hazard could exist if a device is severely overstressed under test; either thermally or electrically. For most measurements, adequate protection can be provided by the use of power supplies with current limiters set to a value specified appropriately for the circuit under test, but this protection may not be adequate for BS 9400 test method 3206. This explosion hazard is most likely to arise from use of test methods 2009, 2010, 2011 and 2014 given in BS 9400 : 1970.

An explosion can also occur due to rapid expansion of entrapped moisture or other liquid under normal dissipation. This can result from prolonged storage or from performing certain of the sealing tests.

c) Burns

These can occur when handling hot or cold equipment used for high temperature and low temperature measurements. In particular, circuits tested at maximum power dissipation may achieve relatively high case or chip temperatures, which could result in burns to the fingers if the device is picked up immediately after the test is terminated. This problem could also be encountered if a fault develops within a device, resulting in abnormally high internal power dissipation. In addition, burns could occur if an operator's fingers are placed in an area where microwave radiations of even modest power are focused.

d) Probe hazards

The possibility of skin injuries exists if probe testers are being used on circuit wafers or chips, and no protective clothing is worn.

While risks associated with any of the above hazards are relatively low, it is considered that they do exist, and could arise when applying any of the published test methods. They are not confined to the tests specifically mentioned.

1.2.2.4 Drying

When drying is required in the test procedure, the integrated circuit shall be conditioned before measurement is made, using either procedure 1 or procedure 2, as required by the detail specification.

Procedure 1: For (24 ± 4) h in an oven at a temperature of (55 ± 2) °C and at a relative humidity not exceeding 20 %.

Procedure 2: For (96 ± 4) h in an oven at a temperature of (100 ± 5) °C.

The integrated circuit shall be allowed to cool in a desiccator, using a suitable desiccant such as activated alumina or silica gel, and shall be kept therein from the time of removal from the oven to the beginning of the specified test.

1.2.3 External visual inspection

Unless otherwise specified, visual inspection shall be performed under approved factory lighting conditions and under normal visual conditions.

Inspection shall include the following items:

- correctness of marking.
- correctness of terminal identification.
- correct encapsulation.
- unbroken body.

1.2.4 Dimensioning and gauging procedures

This clause specifies the requirements for the dimensional inspection of integrated circuits to be used as and when required by the detail specification and in accordance with the general inspection requirements of BS 9000.

These tests shall be made in accordance with the specified drawing and table 4. The dimensions, which shall be checked as part of the group B, C and D inspection requirements, are indicated by the standardized letter references given in BS 3934.

1.2.5 Electrical test procedures

1.2.5.1 Limiting conditions of use

The test conditions for all measurements shall be such that the limiting conditions of use of the device are not exceeded.

Precautions shall include limits on maximum instantaneous currents and applied voltages. It is recommended that devices should not be inserted into, nor removed from, a test circuit while the latter is energized.

1.2.5.2 Equilibrium conditions

All electrical tests shall be conducted under equilibrium conditions unless otherwise specified or unless the measurement is being carried out under pulsed conditions. When test conditions cause significant change with time of the characteristic being measured, means of compensation for such effects shall be specified; for example, the length of time that the device shall be maintained at test conditions before making a measurement.

1.2.5.3 Temperature

Unless otherwise specified, all electrical measurements shall be made at an ambient or reference point temperature of 25 °C.

NOTE. Measurements may be carried out at temperatures other than 25 °C provided that the supervising inspector is satisfied that the device performance will be in accordance with all the provisions of the detail specification when tested at 25 °C.

The ambient temperature shall be measured as the air temperature below the integrated circuit in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

The reference point temperature for case rated integrated circuits intended for conduction cooling through a mounting base shall be measured in accordance with method 0001, given in BS 9400 : 1970.

For circuits specified to be used under conditions other than ambient or conduction cooling, the temperature shall be measured as required by the detail specification.

For measurements at low and high temperatures the methods described in 1.2.7.2 and 1.2.7.3 respectively shall be applied except that the time of exposure shall be reduced to that sufficient to allow temperature equilibrium to be reached. Recovery conditions do not apply.

The temperatures shall be selected from those listed in 1.1.12.

Table 4. Dimensional tests			
Configuration of devices	Group B	Group C	Group D
a) Wire mounted single ended, e.g. SO-3 (BSI), C4 (IEC) with base SB8-1A (BSI). B7A (IEC)	ϕD A	ϕB_2 L	All ¹⁾
b) Flat pack e.g. SO-92 type 1	H Number of leads Seated height (maximum)	$L_{(min.)}$ $b_{(max.)}$ e $z_{max.}$	All ¹⁾
c) In-line (body width does not overhang terminals) e.g. Dual-in-line, SO-87 type 1	$D_{(max.)}$ Seated height (maximum)	$b_{(max.)}$ $C_{(max.)}$ $L_{(min.)}$ Stand off height (minimum)	All ¹⁾
d) In-line (body overhangs terminals)	$D_{(max.)}$ $Z_{(max.)}$ Package width (maximum) $Z_{1(max.)}$ Seated height (maximum)	$\phi b_{(max.)}$ $L_{(min.)}$ Stand off height (minimum)	All ¹⁾

¹⁾ All dimensions included on the BS 3934 drawing called up in the specification or the drawing in the specification and prepared in accordance with BS 3934 except those already covered in groups B and C.

1.2.5.4 Measurement circuit requirements and precautions

NOTE. In 1.2.5.4d) and 1.2.5.4f), a load is chosen to represent the equivalent resistance of the test circuit and unit under test. For acceptance test purposes, the resistor value should represent the limiting conditions.

a) Open-circuit

An open-circuit shall be considered to exist if a two-to-one decrease in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of measurement. The values of high resistances (whether of circuit components or meters) specified in the circuits, shall be so high that a two-to-one decrease in their value does not affect the desired accuracy of the measurement.

b) Short-circuit

A short-circuit shall be considered to exist if a two-to-one increase in the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement. Capacitors used to couple or by-pass the test signal shall present effective short-circuits at the test frequency. In certain of the high frequency measurements, where r.f. decoupling is important, the necessary components and/or mounting conditions of the device shall be as specified.

c) Small-signal

A signal shall be considered small if a two-to-one change in its magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of measurement.

NOTE. Care should be taken that the measuring equipment does not introduce spurious oscillation or distortion likely to affect the required accuracy of measurement.

d) Constant current source

A current source shall be considered constant if a two-to-one increase of a load impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.

e) Current measuring device

The effective admittance of a current measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of the test.

f) Constant voltage source

A voltage source shall be considered constant if a two-to-one decrease of a load impedance does not produce a change in the parameter being measured that is greater than the required accuracy of measurement.

g) Voltage measuring device

The effective impedance of a voltage measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of

measurement.

1.2.5.5 Power supplies

The sources of direct currents and voltages shall not have ripple contents large enough to affect the desired accuracy of measurement. Test or supply voltages or currents shall be within $\pm 1\%$ of the specified value.

1.2.5.6 Precision of measurements

The limits quoted in detail specifications are absolute. Tolerances on measurements shall be taken into account when determining the actual measurement limits.

1.2.5.7 Multiple integrated circuits

The detail specification shall state the test requirements for each section of a multiple integrated circuit consisting of several functionally independent sections. All terminals associated solely with sections not under test shall be left open-circuit unless otherwise specified.

1.2.5.8 Measurement methods

Where applicable the measurement methods shall be selected from BS 9400 or other generic specifications in the BS 9000 series. Where not so referenced, the full text shall be given in the detail specification.

1.2.6 Mechanical test procedures

All the mechanical test procedures required for integrated circuits are included in 1.2.7.

For devices with internal elements mounted with the major seating perpendicular to the Y axis, the Y₁ orientation shall be defined as the one in which the element tends to be removed from its mount (see 3.2.3 of BS EN 165000-1 : 1996).

1.2.7 Environmental test procedures

1.2.7.1 General

This clause specifies the requirements for environmental tests to be used in accordance with the general requirements of BS 9000. The conditions given in each procedure are those from which the manufacturer chooses in order to establish his capability approval. Other conditions may be prescribed by a customer for particular applications. These conditions shall be included in the detail specification. They shall be taken from those included in BS 2011 or BS EN 60068, as appropriate.

Unless otherwise specified, all tests shall be performed under the standard atmospheric conditions for testing as specified in BS EN 60068-1.

When testing is performed by the device manufacturer, more severe test conditions than those specified are permitted. In this case temperatures may be higher than those specified when the specified temperatures are 25 °C and above, and lower than those specified when the specified temperatures are below 25 °C. In all other cases the prescribed limits of test conditions shall be used.

Wherever possible, the tests given in this clause are taken from BS 2011 (or BS EN 60068) or BS 6493 : Part 3. However, some tests are additional to those in BS 2011 or BS 6493 : Part 3 (e.g. rapid change of temperature) and in these cases the test procedures are given in full.

1.2.7.2 Test Aa: Cold for non heat-dissipating specimen with sudden change of temperature

NOTE. This test is non-destructive.

The sample shall be subjected to the procedure described in test A of BS EN 60068-2-1 : 1993. The air in the chamber need not be agitated. Unless otherwise specified there shall be no upper limit requirements for the time of recovery or the relative humidity during the recovery period.

The detail specification shall prescribe:

- a) temperature of conditioning;
- b) duration of conditioning;
- c) association with other tests in a sequence;
- d) electrical and mechanical tests to be made prior to conditioning and after recovery, as appropriate.

1.2.7.3 Test Ba : Dry heat storage

NOTE 1. This test is non-destructive.

The sample shall be subjected to the procedure described in test B of BS EN 60668-2-2 : 1993.

NOTE 2. Test samples may be released if it is demonstrated that solderability is not impaired.

The air in the chamber need not be agitated and there shall be no requirements for relative humidity during the conditioning period.

The duration of the recovery period shall be not less than 1 h nor more than 6 h and there shall be no requirement for the control of relative humidity during that period.

The detail specification shall prescribe:

- a) that the temperature of conditioning = $T_{\text{stg max}}$;
- b) that the duration of conditioning shall be $(1000 \pm 36)_{-30}^{\text{h}}$;
- c) association with other tests in sequence.
- d) the electrical and mechanical tests to be made prior to conditioning and after recovery, as appropriate.

1.2.7.4 Stabilization bake

NOTE. This test is non-destructive.

1.2.7.4.1 Purpose

The procedure provides a preconditioning at the beginning of the screening sequence.

1.2.7.4.2 Apparatus

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature and suitable electrical equipment to make the specified end point measurements.

1.2.7.4.3 Procedure

The devices shall be subjected to the following conditions for the duration specified:

- a) ambient temperature = $T_{\text{stg max}}$;
- b) duration of conditioning $(24 \pm 12)_0^{\text{h}}$;
- c) end point measurements, if required.

1.2.7.4.4 Test condition

The ambient test temperature shall be in accordance with one of the following test temperatures or as specified in the detail specification.

Test condition	Temperature
A	$70 \pm 5 \text{ }^{\circ}\text{C}$
B	$125 \pm 5 \text{ }^{\circ}\text{C}$
C	$150 \pm 5 \text{ }^{\circ}\text{C}$
D	$175 \pm 5 \text{ }^{\circ}\text{C}$
E	$200 \pm 5 \text{ }^{\circ}\text{C}$
F	$85 \pm 5 \text{ }^{\circ}\text{C}$
G	$100 \pm 5 \text{ }^{\circ}\text{C}$

1.2.7.4.5 Specified conditions

The detail specification shall prescribe:

- a) the device history, whether screened or unscreened;
- b) the test temperature;
- c) the test duration if other than 1000 h;
- d) end-point measurements;
- e) intermediate measurements if applicable;
- f) the device number or special data reporting requirements if applicable.

1.2.7.5 Test Ca : Damp heat, steady state

NOTE. This test is destructive.

The sample shall be subjected to the procedure described in test Ca of BS 2011 : Part 2.1Ca : 1977.

Unless excluded by the detail specification, devices subjected to the test shall be checked for corrosion as follows:

- a) the marking shall remain legible;
- b) where appropriate, the lead wires shall be subjected to one bending cycle as described in 1.2.7.17.2. The fracture of a lead shall constitute a failure.

The following detail specification shall prescribe:

- 1) the severity of test (4 days, 21 days or 56 days);
- 2) loading conditions;
- 3) electrical and mechanical tests to be made prior to conditioning and after recovery, as appropriate.

1.2.7.6 Test Db : Damp heat, cyclic

NOTE. This test is destructive.

The sample shall be subjected to the procedure described in test Db of BS 2011 : Part 2.1Db : 1981.

There is no special pre-conditioning procedure.

There are no initial measurements.

The high temperature shall be $(40 \pm 2)^\circ\text{C}$ or $(55 \pm 2)^\circ\text{C}$ and the low temperature shall be $(25 \pm 3)^\circ\text{C}$.

The relative humidity during rise time shall be $> 95\%$ and $< 100\%$.

The relative humidity at high temperature shall be $> 90\%$ and $< 95\%$.

The relative humidity during the remaining period shall be $> 95\%$ and $< 100\%$.

The number of cycles shall be 6 or 28.

During conditioning there shall be no loading and no measurements.

Unless otherwise specified the sample shall remain under standard atmospheric conditions for recovery for not less than 1 h nor more than 2 h.

When the test is performed as a group B test the number of cycles shall be 6.

When the test performed is a group C test the number of cycles shall be 28.

Unless excluded by the detail specification, devices subjected to the 28-cycles test in group C inspection shall be checked for corrosion as follows:

- the marking shall remain legible.
- when appropriate, the lead wires shall be subjected to one bending cycle as described in **1.2.7.17.2** and the fracture of a lead shall constitute a failure.

The detail specification shall prescribe:

- high temperature;
- number of cycles;
- final measurements;
- whether devices are to be examined for post-test corrosion.

1.2.7.7 Test Ea : Shock

NOTE. This test is non-destructive unless otherwise stated in the detail specification.

The sample shall be subjected to the procedure of test Ea given in BS EN 60068-2-27 : 1993. See also **1.2.6**.

The device shall be rigidly mounted by the body, with protection for the terminations, unless otherwise specified in the detail specification.

The half-sine pulse shape shall be used unless otherwise specified in the detail specification.

The severity shall be selected from the values given in table 5.

Table 5. Severity levels for shock test			
Condition	Peak acceleration		Pulse duration
	m/s^2	g_n	
1	294	30	18
2	490	50	11
3	981	100	6
4	4900	500	1
5	14700	1500	0.5

Three successive shocks shall be applied in each direction of three mutually perpendicular axes so chosen that faults are most likely to be revealed (i.e. a total of 18 shocks), unless a larger number of shocks is specified in the detail specification.

Unless otherwise prescribed in the detail specification, the devices shall be non-operating during the test.

The detail specification shall prescribe:

- the method of mounting, if not rigidly mounted by the body;
- the pulse shape, if not half-sine;
- the severity (condition 1, 2, 3, 4 or 5);
- the number of shocks if more than three in each direction;
- the operating conditions if the device is operating during the test;
- the measurements and mechanical/visual checks to be performed before and after the test;
- whether the sealing test shall be performed as a final measurement.

1.2.7.8 Test Eb : Bump

NOTE. This test is non-destructive.

The sample shall be subjected to the procedure described in test Eb given in BS EN 60068-2-29 : 1993. See also **1.2.6**. The preferred severities are:

- 390 m/s^2 and a total of 4000 ± 10 bumps;
- 390 m/s^2 and a total of 1000 ± 10 bumps;
- 98 m/s^2 and a total of 1000 ± 10 bumps.

The detail specification shall prescribe:

- the method of mounting;
- the association with other tests in a sequence;
- the electrical and mechanical tests to be made prior to and after conditioning, as appropriate;
- the severity of test.

1.2.7.9 Test Fc : Vibration (sinusoidal).

NOTE 1. This test is destructive, since it is a vibration endurance test.

The sample shall be subjected to test Fc given in BS EN 60068-2-6 : 1996 (see also **1.2.6**).

The device shall be rigidly mounted by the body, with protection for the terminations, unless otherwise specified in the detail specification.

NOTE 2. The mounting of the device by its terminations introduces extra complications which affect the repeatability for the test, e.g. the provision or otherwise of plated-through holes on the printed circuit board.

The severity shall be selected from annex B of BS EN 60068-2-6 : 1996, from which the values given in table 6 are preferred.

Table 6. Severity levels for vibration test			
Condition	Frequency range Hz	Amplitude or acceleration	Number of sweep cycles in each axis
1	100 to 2000	196 m/s ² (20 g _n)	15
2	55 to 500	0.75 mm or 98 m/s ² (10 g _n)	20
3	10 to 500	0.35 mm or 49 m/s ² (5 g _n)	10

Unless otherwise prescribed in the detail specification, the sample shall be divided into three subsamples and each of the subsamples shall be vibrated successively for the prescribed number of cycles in each of three mutually perpendicular axes. For this test, the three subsamples may be mounted on the three faces of a cubic mounting block, and vibrated simultaneously.

Unless otherwise prescribed in the detail specification, the devices shall not be operating during the test.

The detail specification shall prescribe:

- the method of mounting, if not rigidly mounted by the body;
- the severity (condition 1, 2, 3 or other);
- the vibration regime if other than that stated above;
- the measurements and mechanical/visual checks to be performed before and after the test;
- whether the sealing test shall be performed as a final measurement.
- operating conditions if operated during the test.

1.2.7.10 Test Ga : Acceleration

NOTE. This test is non-destructive. See also 1.2.6.

The sample shall be subjected to test Ga given in BS EN 60068-2-7 : 1993, with the following conditions.

The test shall be carried out using a centrifuge, unless otherwise specified in the detail specification. The device shall be restrained by the case or by its normal mountings, and the terminations shall be secured.

The severity shall be selected from the values given in table 7.

Table 7. Acceleration values	
m/s ²	g _n
490	50
4900	500
1 9600	2000
4 9000	5000
9 8000	10 000
19 6000	20 000
29 4000	30 000

The acceleration shall be increased to the specified value in not less than 20 s, shall remain constant for at least 1 min and shall then be decreased to zero in not less than 20 s.

The detail specification shall prescribe:

- the severity ;
- the direction of acceleration (this should be the most critical direction, e.g. that most likely to detach bonding wires from their pads);
- the measurements and mechanical/visual checks to be performed before and after the test;
- whether the sealing test shall be performed as a final measurement.

1.2.7.11 Test J : Mould growth

NOTE. This test is destructive.

The sample shall be subjected to the procedure described in test J of BS 2011 : Part 2.1J : 1989. The detail specification shall prescribe:

- whether inspection other than visual is required;
- the amount of mould growth allowable and any special requirements regarding etching of surfaces;
- in cases where performance deterioration is to be determined, the pre-test and post-test measurements;
- the period of exposure;
- any variation from the procedure of test J.

1.2.7.12 Corrosion

Not specified.

1.2.7.13 Test M : Low air pressure

NOTE. This test is non-destructive.

The sample shall be subjected to test M given in BS 2011 : Part 2.1M : 1984. The detail specification shall prescribe:

- the severity of test;
- the association with other tests in a sequence;
- the electrical and mechanical tests to be performed prior to conditioning and after recovery, as appropriate.

1.2.7.14 Test Na : Rapid change of temperature

NOTE 1. This test is non-destructive when five cycles are prescribed.

When more than five cycles are prescribed the detail specification shall state whether the test is destructive. The sample shall be subjected to the procedures described in test Na of BS 2011 : Part 2.1N : 1985 with the following requirements.

- The components shall have no voltage applied to them, and be mounted so that free circulation of air is possible between specimens. Either single-chamber or multiple-chamber equipment may be used.
- The low temperature T_A shall be $T_{\text{stg min.}} \pm 3^\circ\text{C}$. The high temperature T_B shall be $T_{\text{stg max.}} \pm 3^\circ\text{C}$.
- The number of cycles shall be five, unless more than five cycles are prescribed in the detail specification.
- At the beginning of conditioning the specimens shall be at room temperature in an unpacked, switched-off, ready-to-use state.
- The exposure time t_1 at each extreme of temperature shall be 10 min, unless a longer time is prescribed in the detail specification.

NOTE 2. The use of carriers or holders, or other factors related to the test equipment being used, may make 10 min too short a time for reasonable temperature stability to be attained.

- The transition time t_2 between extremes of temperature shall be not greater than 5 min.
- The cycles shall be performed consecutively without a break.
- Where electrical measurements are specified as part of the final inspection, recovery shall be not less than 2 h and up to 24 h.

The detail specification shall prescribe:

- the number of cycles, if more than 5;
- the initial inspection and measurements, if required;
- the value of t_1 , if greater than 10 min;
- the final inspection and measurements, if required.

1.2.7.15 Sealing

1.2.7.15.1 General

The efficacy of sealing is determined by means of leak testing. This subclause details testing procedures for both fine leaks (see 1.2.7.15.2) and gross leaks (see 1.2.7.15.3).

A fine leak is one with an equivalent standard leak rate, L , of less than 1×10^{-5} bar·cm³/s. A gross leak is one with an equivalent standard leak rate L of 1×10^{-5} bar·cm³/s or greater.

A fine leak test shall be followed by a gross leak test to ensure that larger leaks are detected if the fine leak test indicates that there is no leak. The fine and gross leak tests shall have an overlap of sensitivity: with this proviso, all gross leaks shall be considered to be equivalent.

NOTE 1. The unit of leak rate is bar·cm³/s. ¹⁾

NOTE 2. Definitions and references are those given in BS EN 60068-2-17 : 1995.

1.2.7.15.2 Fine leak detection

Tracer gas method with mass spectrometer (non-destructive)

This fine leak detection method conforms to method 1 of test Qk of BS EN 60068-2-17 : 1981 with the following specific requirements.

The tracer gas shall be either helium with a purity not less than 95 % by volume, or alternatively, helium with a purity of at least 50 % by volume provided that the $P \cdot t_1$ product is increased in the ratio 95/ X , where X is the percentage by volume of helium in the tracer gas used.

Where the purity of the helium is at least 95 %, one of the immersion conditions given in table 8 shall be selected depending on the strength of the package.

Table 8. Immersion conditions

Pressure, P bar	Minimum immersion time, t_1 min	$Pt_1 \times 60$ bar·s
2	480	57 600
3	320	57 600
4	240	57 600
5	192	57 600
8	120	57 600

For referee test purposes, the minimum specified value of t_1 for the applicable test pressure shall be used.

After immersion, the device may be subjected to a stream of air at room temperature.

The interval t_2 between the completion of the immersion conditions and the measurement in the mass spectrometer shall not exceed 60 min. When V is less than 0.01cm³, t_2 shall not exceed 30 min.

Should an increase in this time interval be necessary, this shall be agreed with the NSI and reference made to a plot of measured helium leak rate, R , and the equivalent standard leak rate, L , together with the sensitivity of the associated gross leak test.

Table 9 gives the maximum permitted value of measured helium leak rate, R . Internal volume, V , is the cavity volume remaining after assembly of internal component parts.

¹⁾ 1 bar = 10^5 N/m² = 100 kPa

Table 9. Maximum permitted helium leak rate				
Internal volume V	Max. permitted helium leak rate R	Equivalent standard leak rates (air)		Time constant $\theta = \frac{V}{L_1}$
		L_1 bar·cm ³ /s	L_2 bar·cm ³ /s	
cm ³	bar·cm ³ /s	bar·cm ³ /s	bar·cm ³ /s	θ
≤ 0.01	5×10^{-8}	$\leq 3.6 \times 10^{-8}$	$\leq 1.9 \times 10^{-5}$	$\leq 2.7 \times 10^5$
> 0.01 to 0.50	5×10^{-8}	3.9×10^{-8} to 2.5×10^{-7}	8.6×10^{-6} to 6.6×10^{-4}	2.6×10^5 to 2.0×10^6
> 0.50 to 10.0	2×10^{-7}	5.1×10^{-7} to 2.2×10^{-6}	5.0×10^{-4} to 1.5×10^{-2}	9.8×10^5 to 4.5×10^6
> 10.0 to 50.0	5×10^{-7}	3.5×10^{-6} to 7.9×10^{-6}	1.2×10^{-2} to 7.9×10^{-2}	2.8×10^6 to 6.3×10^6

The corresponding range of values of equivalent standard leak rate (air) L_1 and L_2 and the range of resulting time constants θ are given.

L_2 represents the higher value of equivalent standard leak rate, L , that can be measured by the fine leak test specified. L_2 values greater than this can only be detected by a gross leak test of suitable sensitivity.

This test shall be followed by a suitable gross leak test so that the range of possible leak rates may be assessed. For internal volumes of 1 cm³ or more, either of the gross leak tests given in 1.2.7.15.3 may be used. For internal volumes less than 1 cm³, the more sensitive gross leak fluorocarbon test shall be used.

Radioactive krypton method (non-destructive)

This fine leak detection method is in accordance with 7.3 of BS 6493 : Part 3 : 1985. The sensitivity range of the test is 10^{-9} to 10^{-5} bar·cm³/s, equivalent standard leak rate (L). The permitted leak rate depends upon the volume of the device and is given in column L_1 of table 9.

The numerical values given are applicable for krypton-85 tracer gas and for a leak rate limit close to 5×10^{-8} bar·cm³/s. The use of other tracer gases would require other numerical values.

Apparatus

The apparatus required for this test consists of a radioactive tracer activation tank and a counting station with sufficient sensitivity to determine the radiation level of the tracer gas inside the device.

The apparatus operates with a tracer gas mixture of krypton-85 and dry nitrogen with a specified activity (100 μ Ci/cm³ minimum²⁾) under standard atmospheric conditions.

Instructions for the use of the leak testing equipment, as supplied by the manufacturer of the equipment, shall be followed in calibrating and operating the equipment. Test results obtained under non-preferred conditions can be compared with those under preferred conditions by conversion through the appropriate formula given in the manufacturer's instructions.

The activation pressure and soak time shall be determined in accordance with equation 1 (see also the note below):

$$Q_s = \frac{R}{3600 skPT} \quad [1]$$

where

- Q_s is the maximum leak rate allowable for the devices to be tested, in bar·cm³/s;
- R is 1200 counts per minute above the ambient background after activation if the device leak rate were exactly equal to Q_s . This is the reject count above the background of both the counting equipment and the component if it has been through previous radioactive leak tests;
- s is the specific activity of the krypton-85 gas in the activation system, in μ Ci/cm³;
- k is the overall counting efficiency of the scintillation crystal in counts per minute per one microcurie of krypton-85 in the internal cavity of the specific component being evaluated. This factor depends upon component configuration and dimensions of the scintillation crystal. The counting efficiency shall be determined in accordance with 7.3.2.4 of BS 6493 : Part 3 : 1985;
- T is the soak time that the devices are to be activated, in h;
- P is equal to $P_e^2 - P_1^2$, where P_e is the absolute activation pressure, in bar, and P_1 is the original absolute internal pressure of the devices, in bar. The activation pressure (P_e) may be established by specification, or if a convenient soak time (T) has been established, the activation pressure (P_e) can be adjusted to satisfy equation (1).

NOTE. The complete version of equation (1) contains a factor $P_0^2 - (\Delta P)^2$ in the numerator which is a correction factor for elevation above sea level. P_0 is the sea level absolute pressure, in bar, and ΔP is the difference in pressures, in bar, between the actual pressure at the test station and sea level pressure. If $P_0 = 840$ mbar, $\Delta P = 140$ mbar at 2200 m.

²⁾ 1 Ci = 3.7×10^{10} Bq

The counting efficiency, k , of equation (1) shall be determined as follows.

A representative unit of the device type to be tested shall be provided with a tube to its internal cavity and the cavity shall be backfilled through the tube with known volume and specific activity of krypton-85 tracer gas and the tabulation should be sealed off.

The counts per minute in the shielded scintillation crystal of the counting station in which the devices are tested shall be directly read.

For each type of encapsulation to be tested, the coatings and external sealants shall be evaluated for surface sorption of krypton-85 before establishing the leak test parameters. Representative samples of the devices shall be subjected to the predetermined pressure and time conditions established for the device configuration as specified in 7.3.2.2 and 7.3.2.3 of BS 6493 : Part 3 : 1985. The count rate of the samples shall then be noted every 10 min until it becomes constant. The elapsed time shall be noted and is the wait time as specified in 7.3.4 of BS 6493 : Part 3 : 1985.

Procedure

The devices shall be placed in a radioactive tracer gas activation tank. The tank shall be evacuated to at least 0.5 mbar. The actual pressure and soak time shall be determined in accordance with 7.3.2.3 of BS 6493 : Part 3 : 1985.

The devices shall be subjected to a minimum of 2 bar absolute pressure of krypton-85/dry nitrogen mixture for a minimum of 12 min. The krypton-85/dry nitrogen gas mixture shall be evacuated until a pressure less than 0.5 mbar exists in the activation tank. This evacuation shall be complete in 5 min maximum.

The activation tank shall be backfilled with air (air wash). The devices shall then be removed from the activation tank, and leak tested within 2 h after gas exposure.

The wait time determined by 7.3.2.5 of BS 6493 : Part 3 : 1985 shall be observed but in no case shall the time between removal from the activation chamber and test exceed 2 h.

If the test is to be repeated on the same specimens, they shall first be decontaminated in vacuum for 8 h, prior to repressurization.

The actual leak rate of the component shall be calculated using the following equation:

$$Q = \frac{V + Q_s}{R}$$

where

- V is the actual readout in net counts per minute;
- Q is the actual leak rate in bar·cm³/s;
- Q_s and R are defined in 7.3.2.3 of BS 6493 : Part 3 : 1985;

Specified condition

The detail specification shall prescribe the limit of the leak rate.

This test shall be followed by gross leak pressurized test specified in 1.2.7.15.3.

1.2.7.15.3 Gross leak detection

Gross leak bubble test (non-destructive)

This test shall be in accordance with method 2 of test Qc of BS EN 60068-2-17 : 1995 and may be used for the detection of leak rates greater than 10⁻³ bar·cm³/s. It consists of placing the test specimens in a bath containing a suitable non-corrosive high boiling point liquid³⁾ maintained at a temperature of (125 ± 5) °C and observing for the emanation of bubbles which are indicative of gas leakage. The bath shall contain a volume of liquid sufficient to ensure that the insertion of the specimen has no significant effect upon the temperature.

Test specimens shall be completely immersed to a depth of not less than 10 mm above the uppermost part of the enclosure or seal to be tested.

The specimens, which shall be at a temperature of between 15 °C and 35 °C at the beginning of the test, shall be immersed in a test liquid with the seals uppermost for a period of 30⁺⁵₀ s.

Test specimens with seals on more than one surface shall be reorientated in turn to bring the respective seals uppermost.

The sample shall be classified as reject if, during the period of the test, any of the following conditions are observed:

- a) a continuous stream of bubbles; or
- b) more than two large bubbles; or
- c) an attached bubble that increases in size.

If the specimens require to be cleaned⁴⁾ after the test, they shall be subjected to a suitable solvent rinse procedure and dried in a stream of warm air.

The detail specification shall prescribe which measurements are to be undertaken prior to conditioning and after recovery, as appropriate.

³⁾ For test temperatures above 90 °C, suitable liquids should have a kinematic viscosity of the order of 0.3 cSt at the test temperature. Commonly used liquids are fluorocarbons, e.g. perfluorotributylamine or perfluoro (1-methyldecane).

⁴⁾ This process will not be required when fluorocarbon liquid is used, as the liquid drains away to leave a clean dry surface. When using hydrocarbons or silicones, or similar liquids for the immersion bath, cleaning will be necessary.

Gross leak pressurized test (non-destructive)

This test is in accordance with method 3 of test Qc of BS EN 60068-2-17 : 1995 and may be used for the detection of leak rates greater than 10^{-5} bar·cm³/s. It is conducted in two stages, involving the impregnation under vacuum and pressure of a sample of the test specimens using low boiling point fluorocarbon liquid. The effectiveness of the seals is checked by subsequent immersion of the specimens in a bath containing a high temperature liquid and checking for the emanation of gas bubbles.

Stage one. Impregnation (performed at room temperature)

The specimen shall be enclosed in a vacuum/pressure vessel and the pressure reduced to about 1 mbar for 1 h. After this period, and without breaking the vacuum, an impregnating fluid⁵⁾ shall be drawn into the vessel until the specimens are completely immersed. The vessel shall then be pressurized under the conditions given in table 10.

Table 10. Pressurization conditions		
Internal cavity volume cm ³	Minimum pressure (absolute) bar	Minimum duration h
≤ 0.1	6	1
> 0.1	3	2
or	2	3

At the end of the impregnation period, atmospheric pressure shall be restored, the specimens being retained in the liquid until required for the next state of testing.

Stage two. Immersion

Before starting stage two testing, specimens shall be removed from the stage 1 liquid and allowed to dry in air at room temperature for 3 ± 1 min.

Stage two (immersion) testing shall be conducted in accordance with the gross leak (bubble) test and employ the same rejection criteria for observed leakage from the specimens.

The specimen shall be observed from the instant of immersion for a period of 30 s, or such other period defined in the detail specification.

In the observation for leakage from the specimen it should be noted that defective devices, on being filled with a volatile fluorocarbon material, will produce a copious stream of bubbles of fluorocarbon vapour. The detail specification shall prescribe the observation period for stage 2, if it is other than 30 s.

1.2.7.16 Test T : Soldering

NOTE. These tests are destructive except where the lead finish is not materially altered by the solderability tests.

1.2.7.16.1 General

The sample shall be subjected to the procedures described in test T of BS 2011 : Part 2.1T : 1981. The use of electrical rejects is permitted. When performed as a test in subgroup B2, prior to the test the specimen shall be stored in air at 150 °C for 3 h and allowed to return to room temperature.

For multilead devices to be tested in accordance with 1.2.7.16.2 (solderability) and 1.2.7.16.4 (de-wetting), the manufacturer may count a group of five leads as one specimen, i.e. a ten-lead device counts as two specimens; however, at least three devices shall be tested.

1.2.7.16.2 Test Ta : Solderability

Solder globule method

The terminations shall be immersed into a flux consisting of 25 % by mass of pure water white rosin (colophony) with 75 % by mass of propan-2-ol for a minimum time of 5 s.

The point of application shall be (5 ± 1) mm from the body.

Where applicable, two leads of each specimen shall be tested. The leads shall be selected in a cyclic manner, lead numbers 1 and 2 on the first specimen, numbers 2 and 3 on the second specimen, and so on.

The solder shall wet a lead within 2.5 s.

When observed under $\times 10$ magnification, the surfaces shall be covered with a smooth and bright solder coating with no more than traces (approximately 5 %) of scattered imperfections, such as pin-holes or un-wetted or de-wetted areas. These imperfections shall not be concentrated in one area.

Solder bath method

Prior to the test, the terminations shall be coated with a flux consisting of 25 % by mass of colophony with 75 % by mass of isopropyl alcohol either by immersion for a minimum time of 5 s to the depth given below or by using a suitable brush. Excess flux may be removed.

The terminations shall be immersed to a point $1.5 \text{ mm} \pm 0.75 \text{ mm}$ from the body, unless otherwise specified, or to half the length of the tag or termination, as appropriate. For flexible leads having no tag or termination, the last 12.5 mm shall be immersed. Chip carriers shall be immersed with the plane of the contact pads normal to the solder surface and, where necessary, carriers may be pre-heated to a maximum of 200 °C prior to dipping. The temperature of the solder bath shall be (235 ± 5) °C.

When observed under $\times 10$ magnification, the dipped surface shall be covered with a smooth and bright solder coating with no more than traces (approximately 5 %) of scattered imperfections such as pin-holes or un-wetted or de-wetted areas. These imperfections shall not be concentrated in one area.

⁵⁾ The liquid used for impregnation in stage one should have a kinematic viscosity of the order of 0.4 cSt at room temperature, a boiling point of approximately 60 °C and a low heat of vaporization to facilitate rapid generation of vapour within the specimen when stage 2 tests are conducted.

Commonly used materials are fluorocarbons, e.g. cyclic-perfluorodipropyl ether or perfluoro-N-hexane, which shall be compatible with the liquid utilized in stage two.

For chip carriers, the inspection of the terminations shall include rejection for peeling or blistering. The detail specification shall prescribe the ageing, if applicable.

1.2.7.16.3 Test Tb : Resistance of components to solder heat

No flux shall be used. The sample shall be subjected to the procedures described in method 1B of test T of BS 2011 : Part 2.1T : 1981.

Unless otherwise specified, the terminations shall be immersed to a point ($2^{+0.5}_0$) mm from the seating plane, or, if no seating plane exists, ($6^{+0.5}_0$) mm from the point of emergence of the lead from the body.

The temperature of the solder bath shall be $(350 \pm 10)^\circ\text{C}$ unless otherwise specified.

The duration of immersion shall be 3.0^{+1}_0 s.

The detail specification shall prescribe:

- a) temperature, if other than 350°C ;
- b) final measurements.

1.2.7.16.4 De-wetting

This test consists of a double immersion in a solder bath (see 1.2.7.16.2), at a higher temperature with longer duration. The terminations are inspected after each immersion.

Prior to the test the terminations shall first be immersed into a flux consisting of 25 % propan-2-ol for a minimum time of 5 s to the depth as given below.

The terminations shall be immersed to a point (1.5 ± 0.75) mm from the body, unless otherwise specified, or to half the length of the tag or termination, as appropriate. For flexible leads having no tag or termination, the last 12.5 mm shall be immersed. The temperature of the solder bath shall be $(260 \pm 5)^\circ\text{C}$. The duration for the immersion shall be (5.0 ± 0.5) s.

When observed under $\times 10$ magnification, the dipped surface shall be covered with a smooth and bright solder coating with no more than traces (approximately 5 %) of scattered imperfections, such as pin-holes or un-wetted or de-wetted areas. These imperfections shall not be concentrated in one area.

The complete procedure is then repeated.

The detail specification shall prescribe:

- a) ageing, if applicable.
- b) the termination immersion point, if other than 1.5 mm from the body.

1.2.7.16.5 Ageing

There are four methods for this conditioning procedure, but the relevance to real-time exposure is indeterminate. Reference should be made to the guidance contained in BS EN 60068-2-44 : 1995. Each method has a suitability in particular circumstances and is only useful for comparing repeated samples.

- a) Method 1A. Steam ageing for 1 h.
- b) Method 1B. Steam ageing for 4 h.
- c) Method 2 : Test Ca. duration 10 days (see 1.2.7.5).
- d) Method 3 : Test Ba. duration 16 h at 155°C (see 1.2.7.3).

1.2.7.17 Test U: Robustness of terminations

1.2.7.17.1 Tensile test

NOTE. This test is destructive.

Electrical rejects may be used. The test is applicable to wire and pin terminations of any cross-section, provided they have not been preformed for mounting, and to packages that have flush mounted terminations, e.g. leadless chip carriers.

The test shall be carried out in accordance with test U_{a1} of BS 2011 : Part 2.1U : 1984, with the following additional provisions:

- a) no preconditioning or initial measurements are required;
- b) at least five terminations are to be tested on any one specimen, but every termination location shall be tested at least once;
- c) no final measurements are required. One broken termination on any specimen renders it a defective.

For packages with flush mounted terminations, a tinned copper wire shall be soldered normal to the plane of the pad and a force applied to the wire which tends to remove the pad from the package. The wire shall be of diameter not greater than the smaller of the rectangular plan dimensions of the pad. The force shall be a loading mass of 0.25 kg.

Should the solder break, the pad shall be examined under microscope to verify its continued adherence to the chip carrier package.

1.2.7.17.2 Bending test

NOTE. This test is destructive.

Electrical rejects may be used. The test is applicable to pliable wire terminations and pins, whether of circular or rectangular cross-section. The test shall be carried out in accordance with test U_b of BS 2011 : Part 2.1U : 1984, with the following additional provisions.

- a) No preconditioning or initial measurements are required.
- b) No more than five terminations need be tested on any one specimen, but every position shall be tested on at least three specimens.
- c) Method 2 shall be used unless otherwise specified in the detail specification.
- d) No final measurements are required. One broken termination on any specimen renders it non-conforming.

The detail specification shall prescribe the method to be used, if other than method 2.

1.2.7.17.3 Bending (row of terminations)

NOTE. This test is destructive.

Electrical rejects may be used. The test is applicable to rows of terminations which are:

- a) not intended to be bent by the user; and/or
- b) preformed for mounting.

It is not applicable to rows of terminations which have separately been subjected to the test specified in 1.2.7.17.2.

No tensile load is applied during the test. The body of the specimen and the row of terminations shall be held in a suitable jig. The ends of the terminations shall simultaneously be pushed through one cycle of bending to 45 °C and back to normal. The direction of bending shall be right angles to the plane of the row of terminations.

For specimens having more than one row of terminations, the test shall be applied to each row in turn.

No initial or final measurements are required. One broken termination on any specimen renders it non-conforming.

1.2.7.17.4 Push test (thrust)

NOTE. This test is destructive.

Electrical rejects may be used. The test is performed only on those leads which support thrust when the device is being mounted.

The test shall be carried out in accordance with test Ua₂ of BS 2011 : Part 2.1U : 1984, with the following additional provisions:

- a) no preconditioning or initial measurements are required;
- b) no more than five terminations need be tested on any one specimen, but every position shall be tested on at least three specimens;
- c) the force shall be applied to the termination at the point where the termination will intersect with the seating plane;
- d) no final measurements are required. If any termination breaks or collapses it renders the specimen non-conforming.

1.2.7.17.5 Torque

NOTE. This test is non-destructive. It is applicable only to devices with threaded terminations.

The test shall be performed in accordance with test Ud of BS 2011 : Part 2.1U : 1984 with the following additional provisions:

- a) severity 1 shall be used.
- b) there shall be no visible damage.

The detail specification shall prescribe:

- 1) initial measurements;
- 2) final measurements and requirements

1.2.7.18 Flammability

NOTE. These tests are destructive. They are normally applied to solid plastics encapsulated circuits but may also be applied to unencapsulated circuits when specified. They are not applicable to ceramic or metal cavity packages.

1.2.7.18.1 Internal

This test is designed to check that the device will not catch fire due to internal heating caused by excessive overloads.

The device shall be operated so that the internal electrical power is slowly increased from the maximum rated value until one of the following

occurs:

- a) the device becomes open circuit or its resistance increases to such a high value that any further increase in power dissipation is impracticable; or,
- b) the device ignites; or,
- c) an internal power dissipation equal to five times the maximum rated power dissipation at 25 °C is reached.

In the case of c), the power shall then be maintained for a minimum duration of 1 min. A device shall be deemed a failure if it smoulders, ignites, or emits flammable or noxious vapours.

1.2.7.18.2 External

This test may be performed on electrically non-conforming devices. In the case of cavity packages other than hermetically sealed ceramic or metal packages, empty packages may be used.

The test shall be a needle-flame test carried out in accordance with BS EN 60695-2-2 : 1995, with the following additional provisions in accordance with clause 11 of that specification:

- a) no special preconditioning is required;
- b) the number of specimens tested shall be two for each package or encapsulation type and no non-conforming specimens are permitted;
- c) unless otherwise stated in the detail specification, the specimen shall be supported with the pins horizontal and with the major axis vertical;
- d) the flame shall be applied to that part of the specimen that is most likely to ignite, if this is known. If this part is not known and is not defined in the detail specification, the flame shall be applied to one of the lower corners of the specimen;
- e) the underlying layer to be used to evaluate the effect of flaming drops shall be as described in clause 4 of BS EN 60695-2-2 : 1995.
- f) unless otherwise specified in the detail specification the flame shall be applied for 10 s.
- g) as a result of the test, both of the following requirements shall be met:

- 1) after removal of the flame the specimen shall not burn for more than 10 s.
- 2) flames, or particles falling from the specimen, shall not spread fire to the underlying tissue paper. If only one requirement is met, the report shall state which requirement was not met. If requirement (1) was not met, the report shall state the time that the specimen burnt for.

- h) no measurement of electrical or mechanical properties is required after the test.

The detail specification shall prescribe:

- i) the method of support of the test specimen, if other than as specified in 1.2.7.18.2c)
- ii) the part of the specimen to which flame shall be applied;
- iii) the period of application of the flame, if other than 10 s.

1.2.7.19 Resistance to solvents

1.2.7.19.1 Immersion in cleaning solvents

NOTE. The test is destructive and reject electrical devices may be used where no final measurement is required.

The circuits shall be tested in accordance with test XA of BS EN 60068-2-45 : 1993, subject to the following provisions:

- a) The solvent used shall be as defined in 3.1.1 of BS EN 60068-2-45 : 1993. If so specified in the detail specification, separate tests may be performed using the solvent specified in 3.1.2 of BS EN 60068-2-45 : 1993 or any other specified solvent;
- b) The temperature for the solvent as defined in 3.1.1 of BS EN 60068-2-45 : 1993 shall be $(23 \pm 5) ^\circ\text{C}$ unless boiling temperature is specified in the detail specification;
- c) No initial measurements are required unless otherwise specified in the detail specification;
- d) Conditioning shall be by method 1 (rubbing);
- e) Cotton wool shall be used as the rubbing material;
- f) Recovery time is not applicable unless final electrical measurements are to be made, in which case it shall be not more than 48 h unless otherwise stated in the detail specification;
- g) No final measurements are required, unless otherwise stated in the detail specification;
- h) The mandatory acceptance criterion is that the marking shall be legible but additional criteria may be specified in the detail specification.

The detail specification shall prescribe:

- 1) separate tests with alternative solvents, if required;
- 2) solvent boiling temperature, if required;
- 3) initial measurements, if required;
- 4) recovery time, if other than given in item f);
- 5) final measurements, if required;
- 6) additional acceptance criteria, if required.

1.2.7.19.2 Resistance to contaminating fluids

NOTE. The test is destructive and electrical reject devices may be used.

This test shall only be applied when required by the detail specification. It is normally applied only to circuits with solid plastics encapsulation.

The circuits shall be tested in accordance with BS 3G100 : Part 2 : Subsection 3.12 with the following conditions.

- a) The circuits shall be individually weighed.
- b) The test fluid(s) shall be specified in the detail specification, preference being given to the solvents specified in table 1 of BS 3 G100 : Part 2 : Subsection 3.12. Five specimens shall be used for each test fluid.

c) The procedure of clause 9 of BS 3G100 : Part 2 : Subsection 3.12 shall be used.

d) The circuits shall be immersed at a temperature of $(25 \pm 5) ^\circ\text{C}$ for a period of 1 h. Recovery shall be in 1 h to 2 h unless otherwise specified in the detail specification. Fluid still adhering after the specified period shall be removed.

e) The circuits shall be submitted to the following tests:

- 1) the dimensions measured in subgroup B1 (b) shall conform to the requirements of that subgroup.
 - 2) the circuits shall be individually weighed. No circuit shall have changed in weight by more than 1 %.
 - 3) the markings shall be legible.
- f) One non-conformity constitutes a failure for the contaminating fluid concerned.

The detail specification shall prescribe:

- 1) whether test is required;
- 2) test fluids;
- 3) the recovery period, if not 1 h to 2 h.

1.2.7.20 Rapid change of temperature, two-bath method

NOTE. This test is destructive.

The sample shall be subjected to the procedures described in test Nc of BS 2011 : Part 2.1N : 1985 with the following requirements.

- a) The duration parameters shall be given by:
 - 1) time of transfer $t_2 = 8 \pm 2 \text{ s}$
 - 2) immersion time t_1 such that $2 \text{ min} < t_1 < 20 \text{ min}$ (see also 3.3 of BS 2011 : Part 2.2N).
- b) The number of consecutive cycles shall be 10, unless otherwise specified in the detail specification.
- c) The temperature of the cold bath T_A shall be $T_{\text{stg min.}} \pm 3 ^\circ\text{C}$.
- d) The temperature of the hot bath T_B shall be $T_{\text{stg max.}} \pm 3 ^\circ\text{C}$.
- e) The identity of the liquids to be used shall be prescribed in the detail specification.
- f) Initial inspection and measurements, if any, shall be prescribed in the detail specification.
- g) Where electrical measurements are specified in h), recovery shall be not less than 2 h and up to 24 h at standard conditions for measurement.
- h) Final inspection and measurements, if any, shall be prescribed in the detail specification.

The detail specification shall prescribe:

- 1) the number of consecutive cycles, if other than 10;
- 2) the identity of the liquids to be used;
- 3) the initial inspection and measurements, if any;
- 4) the final inspection and measurements, if any.

1.2.7.21 *Damp heat steady state with bias*

NOTE. The test is destructive. This test is applicable to non-cavity devices.

1.2.7.21.1 *Purpose*

The steady state humidity test is performed for the purpose of evaluating, in an accelerated manner, the resistance of non-cavity devices to the deteriorative effects of the high humidity and heat conditions, but is not intended to evaluate external corrosion effects. Degradation results from absorption of water vapour by the encapsulation materials and presence of moisture films or penetration of moisture along physical junctions.

NOTE. A non-cavity device is a device in which enclosing or encapsulating material is in intimate contact with all exposed surfaces of the active element, and no void space is included in the device design.

1.2.7.21.2 *Testing chamber*

This shall be constructed and operated so as to conform to the conditions given in items a) to d).

- a) The temperature and humidity of the chamber are monitored by means of sensing devices located in the working space.
- b) The temperature and relative humidity in the working space are maintained at $\pm 2^\circ\text{C}$ of the specified temperature, and $\pm 5\%$ of the relative humidity.

NOTE. The temperature tolerance of $\pm 2^\circ\text{C}$ is intended to take account of absolute errors in the measurement, slow changes of temperature and temperature variations of the working space. It is necessary to keep the short-term temperature fluctuation within $\pm 0.5^\circ\text{C}$ to maintain the required humidity.

For reference purposes, the minimum value of relative humidity should be taken. The measurement of relative humidity is difficult and the calibration of the measuring instruments is of great significance. This offers the possibility of conflicting results from different test houses at different times. It should be noted that the tolerances are absolute.

- c) Condensed water is continuously drained from the chamber and not used again until it has been re-purified.
- d) When the specified relative humidity is maintained by using an injection-type chamber, the water shall have a resistivity of not less than $500\ \Omega\cdot\text{m}$.

Precautions shall be taken to ensure that the following conditions are met:

- 1) that the conditions prevailing throughout the working space are uniform and as similar as possible to those prevailing in the immediate vicinity of the sensing devices.
- 2) that the properties or loading of the specimen under test do not appreciably influence conditions within the chamber.
- 3) that no condensed water from the walls and roof of the test chamber falls on the specimens.

1.2.7.21.3 *Procedure*

The procedure consists of the following steps.

- a) Prior to exposure, the specified initial measurements shall be made at standard atmospheric conditions or as specified in the detail specification.
- b) During exposure:

- 1) when specified in the detail specification, the devices shall have a voltage bias applied. The circuit configuration for applying bias shall be chosen to satisfy the criteria listed below in order of importance;

- i) power as small as possible;
- ii) voltage as high as possible within the operating range;

NOTE. The highest stress conditions correspond to zero power, maximum allowed voltage to the device within the operating range and maximum allowed voltage between adjacent metallization lines on the die.

- 2) bias voltages and/or currents shall be applied to devices for a total time equal to the specified test time (within the allowed tolerance);
- 3) the voltage bias(es) shall continue to be applied to devices until the chamber has cooled to room temperatures when the devices may be removed from test.

If the chamber is opened for the insertion or removal of samples, the period from when specified conditions cease to exist to when they are re-established shall be discounted from the recorded test time of the devices in the chamber. The interruption periods shall not exceed 2 h per day.

1.2.7.21.4 *Recovery*

After removal from the chamber, specimens shall be allowed to recover, for a period of not less than 2 h and not exceeding 24 h, at $(25 \pm 3)^\circ\text{C}$ and normal atmospheric pressure, prior to endpoint measurements. Any residual moisture shall be removed by wiping.

1.2.7.21.5 *Final measurements*

These may be initiated any time during or upon completion of the recovery period, but all measurements shall be completed within the 8 h following the recovery period.

1.2.7.21.6 Test conditions

Test conditions shall be as follows:

- temperature: $(85 \pm 2) ^\circ\text{C}$
- relative humidity: $(85 \pm 5) \%$
- steady-state humidity test duration: $(1000 \pm 96) \text{ h}$,
unless otherwise specified in the detail specification.

1.2.7.21.7 Specified conditions

The detail specification shall prescribe:

- a) the applied voltage and circuit configuration, if different from that used in sub-group B5 in table 33.
- b) the initial and final measurements and their ambient conditions if different from standard atmospheric conditions.
- c) the test duration if different from 1000 h.

1.2.7.22 Thermal intermittence test**1.2.7.22.1 General**

This test is non-destructive unless otherwise specified in the detail specification. The test shall be conducted with reference to Test Nb of BS 2011 : Part 2.1N : 1985. It test is primarily intended for devices having no internal cavity.

1.2.7.22.2 Purpose

To determine whether the internal interconnection system of a test specimen is subject to intermittent failures when subjected to a slowly changing temperature.

1.2.7.22.3 Procedure

The single chamber shall include provision for electrical connection to, and monitoring of, device(s) under test, with access to each device terminal. The test shall be conducted as described in **1.2.7.14**.

NOTE. The cycles described in **1.2.7.14g**) may be performed either from the specified low temperature to the specified high temperature, or by using the severities given in table 11.

The duration of exposure, t_1 , shall be $\geq 1 \text{ min}$.

Electrical tests are to be performed only during the temperature cycle. The detail specification shall prescribe a maximum current per termination.

An example of a parallel detection circuit is given in figure 3. Other circuits (e.g. series detection, constant voltage generator, etc.) are also permitted.

The test apparatus shall be capable of sensing and identifying a failed device.

The threshold detector shall be set to indicate a failure at the voltage specified in the detail specification. A failure is defined by an evidence of open-circuit at any internally connected terminal or short-circuit between two leads.

After the initial change from room temperature to T_A or T_B , device terminals shall be monitored at least once for each $3 ^\circ\text{C}$ change when the temperature is varied either from minimum to maximum or from maximum to minimum (see note to table 11).

The test conditions used for testing the continuity of each lead shall be specified in the detail specification so that minimum power dissipation is obtained, thus ensuring that the case and junction temperatures are approximately equal to the ambient temperature.

No recovery is required.

1.2.7.22.4 Information to be given in the detail specification

The detail specification shall prescribe:

- a) whether the test is considered destructive or non-destructive;
- b) the severity level, A, B or C, as required;
- c) the maximum current per termination;
- d) the threshold detector failure voltage;
- e) the test conditions for testing the continuity of each lead.

Table 11. Severities to be used for the thermal intermittence test

Condition	Severity		
	A	B	C
Low temperature T_A	$(25 \pm 5) ^\circ\text{C}$	Minimum operating temperature	Minimum storage temperature
High temperature T_B	$(125 \pm 5) ^\circ\text{C}$	Maximum operating temperature	Maximum storage temperature
Rate of change of temperature (average over the period of temperature change) (see note)	3 °C /min, maximum		
Number of cycles	$\frac{1}{2}$ (i.e. from T_A to T_B or T_B to T_A)		
NOTE. A more rapid change of temperature is acceptable provided that use is made of a detector, the time constant of which is sufficiently small and the scanning rate of which is sufficiently low that it will detect intermittent failures of short duration that the normal method would have shown.			

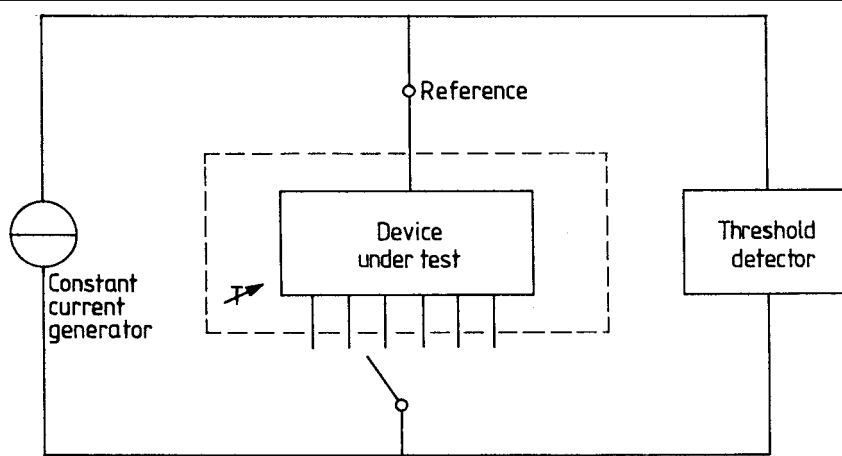


Figure 3. Parallel detection circuit

1.2.8 Electrical endurance test procedures

1.2.8.1 General

The tests shall be performed on samples from capability qualifying circuits that have passed their specified group A electrical inspection. Where these results have been recorded they may be used as start of test data, provided that pre- and post-test measurements are made on the same equipment.

The samples shall be operated for the specified period under the specified conditions.

All sections of each specimen shall be tested.

During the test, the terminal voltages and currents, or the power dissipated by any one device, shall not fall from the specified values by more than 10 %.

The ambient, or other specified temperature at which any device is operated shall not fall below the specified value by more than 5 °C. Unless otherwise specified, lead mounted devices shall be mounted by their leads with the jig mounting clips at least 5 mm from the body of the device. The point of connection shall be not less than 5 °C below the specified temperature.

NOTE. Where the test duration does not exceed a nominal 2000 h at maximum operating temperature, the tests are considered to be non-destructive. Devices from a sample passing such tests may be released if they meet the limits specified for group A and group B solderability.

1.2.8.2 Test conditions

1.2.8.2.1 General

The devices shall be subjected, for the specified time and temperature, to one of the specified test conditions as described below and in the detail specification. The specified measurements shall be made at the specified intermediate points and at the end points.

1.2.8.2.2 Steady-state, reverse bias

This test condition is illustrated in figure 4, and is suitable for use on all types of circuits, both linear and digital types. In this test as many junctions as possible shall be reverse biased to the specified voltage and power dissipation. The ambient test temperature shall be the maximum possible but shall be selected so as not to exceed the thermal rating of the device.

1.2.8.2.3 Steady-state, power

This test condition is illustrated in figure 4 and can be used on all digital type circuits and on some linear types. In this test, as many junctions as possible shall be forward biased, as specified. The ambient test temperature shall be the maximum possible but shall be selected so as not to exceed the thermal rating of the device.

For passive circuits, power shall be applied so that, as far as is practicable, each resistor is dissipating its proportional amount of power and each capacitor is subjected to its nominal voltage stress.

1.2.8.2.4 Power and reverse bias

This test condition is illustrated in figure 4, and is used for circuits where the inputs can be reverse biased and the output can be biased for maximum power dissipation or vice versa. These conditions may be switched sequentially. The ambient temperature shall be selected so as not to exceed the maximum thermal rating of the device.

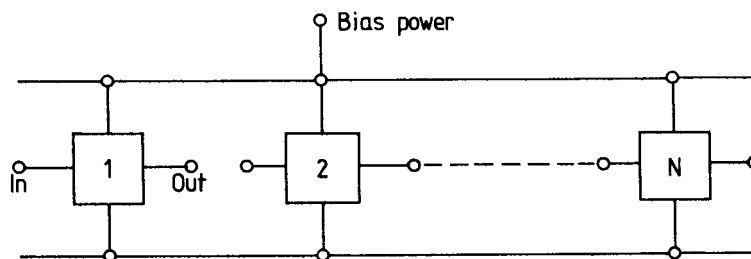


Figure 4. Example of steady state, reverse bias or power test set-up for endurance testing

1.2.8.2.5 Parallel excitation

This test condition is illustrated in figure 5, and is suitable for use on all circuit types. Each circuit is driven with an appropriate signal to simulate the normal circuit application as closely as possible. All circuits shall have a maximum load applied, excitation shall be applied at a frequency of not less than 50 Hz and the test shall be conducted at the maximum rated temperature, unless otherwise specified. This test is usually referred to as parallel switching applied to digital circuits.

1.2.8.2.6 Ring oscillator

In this test, illustrated in figure 6, any number of digital circuits greater than two are connected in series. For circuits that cause phase inversion, an odd number of circuits shall be used with the output of the last circuit connected to the input of the first circuit. The series will be free running at a frequency established by the propagation delay time of each circuit and its associated wiring. Each circuit in the ring shall be loaded to its rated maximum and biased at normal rated voltage. The test shall be conducted at maximum rated temperature unless otherwise specified. This test may be conducted with the open-ring or series switching configuration where the first device in the series is switched by an external source. In this configuration, the duty cycle and the basic frequency of operation depend mainly on the capabilities of the individual devices. When the free running or 'closed' ring configuration is employed, no more than 21 devices shall be contained in any single ring. Where the 'open' ring configuration is employed, the time duration between inputs from the external source shall be no greater than 20 times the propagation delay of the device as specified in the detail specification.

1.2.8.2.7 Sequential HIGH-LOW state operation

The life test circuit shall be so arranged that the outputs shall be operated for approximately equal periods sequentially.

- in the LOW state;
- in the HIGH state;
- continuously switched at not less than 47 pulses per s, for equal intervals between the LOW and HIGH state by means of suitable signals applied to the inputs.

The duration for the LOW and HIGH state conditions in a) and b) shall be not less than twice the time needed for thermal equilibrium to be established.

During the continuous switching period, each input shall be operated on a cyclic basis so that all inputs are operative for approximately equal periods.

Some form of monitoring circuit should be available to check the above sequence of events.

1.2.8.3 Specified conditions

The detail specification shall prescribe:

- duration.
- ambient or reference point temperature.
- test circuit to be specified from those given in 1.2.8.2.3 to 1.2.8.2.6.
- electrical conditions to be applied to all terminals.

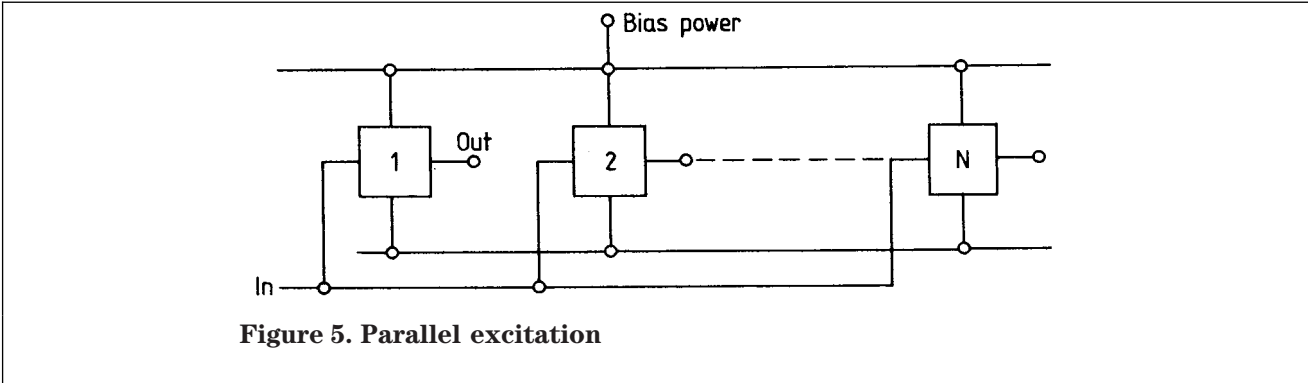
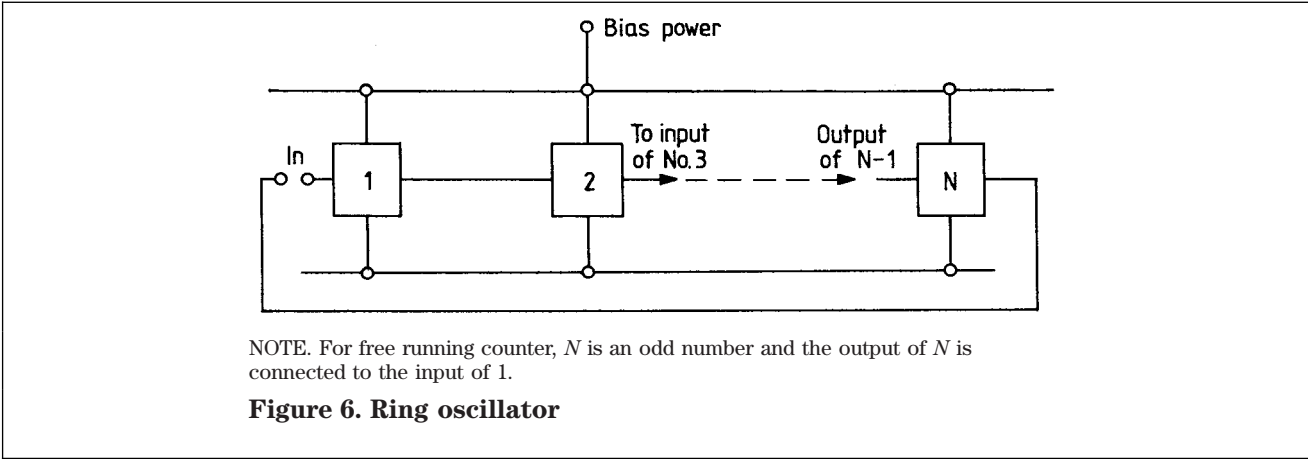


Figure 5. Parallel excitation



NOTE. For free running counter, N is an odd number and the output of N is connected to the input of 1.

Figure 6. Ring oscillator

1.2.9 Accelerated test procedures

1.2.9.1 General

Where required by the customer's specification or contract, 'thermal overstress' testing may be used as an alternative or additional to the electrical endurance test schedules prescribed in table 33. The test durations and temperatures shall be specified.

NOTE. Reference should be made to 1.2.8.1, 1.2.8.2 and 1.2.8.3 of BS 9400 : 1970 for accelerated test procedures for temperature, industrial atmosphere and humidity respectively.

1.2.9.2 Thermally accelerated test for thick film resistive elements and associated conductors

NOTE 1. This test is intended to be conducted on actual networks or approved CQCs without added components but otherwise processed in the same way as the complete microcircuit, including trimming, overglazing and soldering .

Test times and temperatures shall be calculated using the equation

$$t_s = t_o \exp \left[8120 \left(\frac{1}{T_s} - \frac{1}{T_o} \right) \right]$$

where

- t_s is the test duration, in h;
- t_o is the expected operating life time, in h,
- T_s is the test temperature, in K;
- T_o is the operating temperature, in K (maximum resistor surface temperature);

NOTE 2. This Arrhenius type equation includes an apparent activation energy of 0.7eV and Boltzmanns constant = 8.617×10^{-5} eV/K.

NOTE 3. Test temperatures may be selected from clause 1.1.12.3. It should be demonstrated that the test temperature is valid, i.e. that it does not affect the materials used such as epoxy resins and substrates.

Initial measurements shall be made at $T_{amb} = (25 \pm 5) ^\circ\text{C}$ for all resistor values. Post-test end point measurements shall be made after a 4 h minimum cooling period at the pre-stress ambient temperature ($\pm 2 ^\circ\text{C}$).

The detail specification shall prescribe post-test end points.

1.2.9.3 Damp heat accelerated test for long term changes in resistance and interconductor leakage

1.2.9.3.1 General

This test is applicable only when called up as an additional subgroup in the test schedule in the customer detail specification. It is intended as a test for thick film conductors and resistors in hybrid circuits in non-hermetic packages.

The environmental test conditions are as specified under severity A of table 11, except that the humidity tolerance shall be $\pm 3\%$ and the duration 700 h. Non-reproducible results will be obtained if water droplets are allowed to condense on the specimens during conditioning.

1.2.9.3.2 Construction and biasing of the test circuits

The test shall be carried out on specially designed circuits, related to the claims declared in the capability manual, as described below.

a) resistor elements

Three sets of four resistor elements shall be provided on the test circuit, one set each for the highest and lowest ink resistivity used and one set for an intermediate resistivity. Adjacent resistor elements shall be electrically isolated and separated along the maximum dimension by the minimum declared spacing. The aspect ratio of the elements shall be the maximum declared value and the maximum element width shall be 2 mm.

The biasing arrangements during conditioning shall be such that no power is dissipated by any resistor, and that the maximum declared voltage appears across the three parallel gaps in each set of four resistors.

b) conductors, lateral leakage

Two parallel conductors shall be provided, at least 10 mm in length and separated by the minimum declared separation for protected conductors.

Both the conductors and the gap between them shall be covered by the declared overglaze protection.

Two parallel solder-coated conductors shall be provided, at least 10 mm in length and separated by the minimum declared separation for solder-coated conductors. The gap between the conductors may be covered by the declared overglaze protection if this is provided for in the declared design rules.

In each case the bias during conditioning between the two parallel conductors shall be the maximum declared voltage between parallel conductors of each type, applied through a 1 M Ω resistor. It is preferable for this 1 M Ω resistor to be part of the hybrid circuit.

c) conductors, inter-level leakage

A number of cross-overs in parallel shall be provided. Each cross-over shall be of the minimum dimensions allowed in the declared design rules, and the number shall be such that the total conductor overlap area is at least half the maximum total area of conductor overlap in cross-overs which can occur in any customer circuit, or 1 mm², whichever is the greater.

The bias between the conducting layers during conditioning shall be the maximum declared voltage, applied through a 1 M Ω resistor. It is preferable for this 1 M Ω resistor to be part of the hybrid circuit.

1.2.9.3.3 Initial and final measurements

The measurements shall be carried out under standard atmospheric conditions for testing (see 5.3 of BS EN 60068-1: 1995). Before final measurements the specimens shall be allowed to recover with no bias applied for not less than 4 h nor more than 24 h under standard atmospheric conditions for testing. The temperature of the initial and final measurements shall not differ by more than 2 °C.

For the resistors defined in 1.2.9.3.2, the resistance of the middle two resistance elements of each set of four shall be measured in accordance with 4.4 of BS EN 140000 : 1995.

For the conductors as defined in 1.2.9.3.2 the insulation resistance shall be measured by applying the declared maximum voltage across the conductor gap and a 1 M Ω resistor in series. The result reported shall include the resistance of the 1 M Ω resistor. At no time during conditioning or testing shall any voltage be applied directly across the gap between the conductors.

1.2.9.3.4 Requirements

Unless otherwise specified in the detail specification, the change in resistance between initial and final measurements on any resistor shall not be more than $\pm 3\%$, and the final ratio between the two middle resistors of each set shall not differ by more than 1 % from the initial ratio.

Unless otherwise specified in the detail specification, the insulation resistance between parallel conducting tracks, both initially and finally, shall exceed 10 G Ω divided by the length of the parallel conductor track in millimetres.

Unless otherwise specified in the detail specification, the insulation resistance between conducting layers, both initially and finally, shall exceed 10 G Ω divided by the overlapping area of the crossing conductors in square millimetres.

1.2.9.3.5 Detail specification

The detail specification shall prescribe:

- a) whether the test is required;
- b) the variations in the requirements of **1.2.9.3.4**, if required.

1.2.10 Screening test procedures**1.2.10.1 General**

Screening options may be separately negotiated between customer and manufacturer and specified in the detail specification for general applications (see also **3.6**).

A general screening level is included in table 12, from which a screening sequence can be chosen depending upon the application. Stress levels may be selected from the clauses listed in table 12.

Screening level B, detailed in **1.2.10.2.1**, provides a definitive screening sequence for additional assessment level S2 circuits compatible with BS 9400 level S2 requirements.

Application information for S2 circuits is given in **2.5** of BS 9400.

1.2.10.2 Screening requirements**1.2.10.2.1 General**

The following screening requirements shall apply to monolithic, film hybrid and SAW devices.

- a) For S2 devices, the manufacturer shall hold capability approval to the full assessment level covering the types of circuit concerned.
- b) Packages for the general level shall be any listed in the capability manual with the packaged circuit having any operating temperature rating selected from **1.1.12.4**.

For release to screening level B (S2), cavity packaged circuits having the temperature rating stated in **1.1.12.4a** shall be used. For other screening levels, the customer may call for release at other temperatures.

- c) Added components may be category A or B (see **1.3.2**) for the general level, but category A shall be used for assessment level S2.

- d) Internal visual inspection shall be performed as follows:

- 1) Pre-assembly (substrate) (see **1.2.11.2**).
- 2) Post-assembly (pre-seal) (see **1.2.11.3**).

- e) Every potential additional assessment circuit shall be tested or inspected to the requirements for the specified screening level in the order given.

- f) Following successful screening, quality conformity testing shall be carried out to fulfil the requirements of the detail specification.

Tests for maintenance of capability approval shall be performed on unscreened CQCs except when all circuits are screened in production.

- g) Circuits for S2 assessment contained in cavity packages having an inner seal perimeter of 50 mm or more shall be screened to level B requirements (see table 12).

- h) Where the inner seal perimeter is less than 50 mm, the screening procedures of **1.2.9.1.2** of BS 9400 (level B) may be used, providing that the internal visual inspection is in accordance with **1.2.11.2** and **1.2.11.3** of this standard.

Alternatively, such small packages may be screened in accordance with BS 9450 level B (see table 12), provided that for test 5, the acceleration stress level is increased to 294 000 m/s² without the shock option, and the internal visual inspection is in accordance with this standard.

1.2.10.2.2 Screening test and inspection

For assessment level S2, the complete list of tests and inspections in table 12 level B shall be performed in the order shown.

NOTE. For monolithic devices, seal testing may be performed at any stage after acceleration steady state (provided that all shearing or forming processes are completed) and at any time before group A, B and C testing is performed.

When seal testing is performed prior to burn-in, subgroup B2 sample testing shall be performed.

1.2.10.2.3 Detail specification inspection requirements

Where the requirements of **11.1.1** of BS 9000 : Part 6 : 1989 are met, the following shall apply with reference to table 33:

- screens 10 and 11 may be accepted for group A;
- screens 4 and 9 may be accepted for subgroup B2 if seal testing is carried out after the burn-in screen;
- screen 5 may be accepted for subgroup B4;
- screen 7 may be accepted for subgroup B5;
- screen 8 may be accepted for subgroup B6 providing there are no additional requirements in the detail specification.

Group C and D conformity is demonstrated by the current validity of periodic testing of CQCs.

Table 12. Screening levels, test and inspection

Test and inspection	Screening levels (references and conditions)	
	General	Level B (S2)
1. Internal visual	1.2.11.2 and 1.2.11.3	1.2.11.2 and 1.2.11.3
2. Leakage current (see note 5)		BS 9400 test method 2013 Test voltage : 30 V d.c. T_{AMB} : 15 °C to 35 °C Max. leakage after 5 s : 1 mA
3. Stabilization bake (see note 4)	1.2.7.4	1.2.7.4 T_{stg} max.
4. Rapid change of temperature	1.2.7.14	1.2.7.14 (10 cycles T_{stg} max. to T_{stg} min.)
5. Acceleration or Shock	1.2.7.10	1.2.7.10 (49 000 m/s ² Y_1 axis) see note 2
	1.2.7.7	1.2.7.7 (14 700 m/s ² Y_1 axis)
6. Electrical	1.2.5 and as specified in detail specification (optional of no PDA)	1.2.5 Functions at 25 °C Major statics at 25 °C min., unless otherwise specified
7. Burn-in (see note 4)	1.2.10.3 and as specified in detail specification	1.2.10.3 (duration : 160 h min., ambient : 125 °C min.)
8. Electrical	As test 6 (optional if no PDA)	As test 6. PDA 10 % (see notes 3 and 6)
9. Sealing	1.2.7.15	1.2.7.15
10. External visual	1.2.3	1.2.3
11. Final electrical	1.2.5 100 % testing as subgroup A2	1.2.5 Functions at -55 °C, +25 °C, +125 °C Major statics at -55 °C, +25 °C, +125 °C Dynamic at +25 °C

NOTE 1. Level B is not applicable to solid plastic encapsulated circuits.

NOTE 2. Stress level is for circuits with inner seal perimeter of 50 mm or more. See **1.2.10.2.1h** for perimeters less than 50 mm.

NOTE 3. For multi-chip film hybrid circuits, where the observed percentage defective is found to be greater than 10 % but not greater than 20 %, the lot shall be re-submitted once to a tightened PDA (percentage defective allowable) of 7 %. Re-submitted lots shall consist only of surviving circuits which were in the original lot.

NOTE 4. Pre-seal high temperature storage and pre-seal burn-in are not standardized.

NOTE 5. Applicable to SAW devices with isolated transducer terminals only. Leakage current is performed post assembly but before sealing. Tests 3 to 11 are then performed post seal.

NOTE 6. PDA is applicable to functional major static and dynamic parameters as specified in the detail specification.

1.2.10.3 Burn-in screen

1.2.10.3.1 General

The circuits shall be subjected to the burn-in screen by operating them in accordance with one of the specified test conditions given in **1.2.8.2** and the requirements of **1.2.8.1** except for the first paragraph.

The units shall be cooled down under bias conditions. Alternatively, natural or convected cooling may be applied after removal of bias, providing that no more than 30 min elapses between removal of the bias and the time that junction temperatures drop to an estimated 35 °C maximum.

1.2.10.3.2 Specified conditions

The detail specification shall prescribe:

- a) general procedures, if other than those specified in **1.2.8.1**.
- b) the maximum allowable deviations in electrical test results.
- c) electrical conditions to be applied to all terminals.

1.2.10.3.3 Accelerated burn-in

At the manufacturer's option, and with the agreement of the NSI, the ambient temperature used for the burn-in screen for monolithic integrated circuits may be increased to a maximum of 155 °C and the test time reduced in accordance with the principles detailed in 1.2.9.2. An activation energy of 0.4 eV may be used without demonstration, or a specific value may be demonstrated.

1.2.11 Internal visual inspection

1.2.11.1 General

1.2.11.1.1 Object

This clause covers the internal visual inspection requirements for hybrid and passive film integrated circuits, including SAW devices, produced under capability approval.

Internal visual inspection criteria for semiconductor monolithic and semiconductor multichip integrated circuits, produced under capability approval, are given in 1.2.10 of BS 9400.

The purpose of internal visual inspection is to eliminate those integrated circuits having internal defects or weaknesses due to processing and/or poor workmanship which could lead to premature failure under the normal application for which the circuit is intended.

NOTE. Manufacturers wishing to qualify a new technology requiring modification to internal visual inspection requirements should at the earliest time inform the appropriate BSI Technical Committee who will bring it to the attention of the NSI.

1.2.11.1.2 Apparatus

The apparatus for internal visual inspection shall include optical equipment capable of the magnifications specified in 1.2.11.1.3 and any visual standards, e.g. gauges, drawings and photographs, necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of materials being inspected.

1.2.11.1.3 Magnification

High magnification

The range $\times 100$ min. to $\times 200$ max. shall be used for high magnification and the inspection shall preferably be performed perpendicular to the substrate surface with the device under illumination normal to the substrate surface.

Low magnification

The range $\times 10$ min. to $\times 60$ max. shall be used for low magnification and the inspection shall be performed either with monocular, binocular or stereoscopic microscope and the inspection performed at a suitable angle from the perpendicular to the substrate surface with the device under suitable illumination.

1.2.11.1.4 Procedure

The circuit shall be examined in a suitable sequence within the specified magnification range to determine conformity to the visual inspection requirements given below. The order in which the examinations are made may be varied at the discretion of the manufacturer with the exception of the inspection of package conditions which shall be the last internal inspection performed. Where doubts arise concerning marginal conformity, and where resolution by precise measurement is not practical, visual judgement may be validated by alternative non-destructive procedures. Examples may include mechanical tests to demonstrate the meeting of the design requirements for die attachment, wire or bond strength. Such alternatives shall first be agreed with the NSI.

NOTE. The visual inspection specified in 1.2.11.2.1b) or 1.2.11.2.1c) may be carried out prior to die attachment, provided that the examination is performed under the same control and supervision that is required at the final pre-seal inspection point.

Proper control shall be exercised after wafer, slice or pre-assembly inspection to ensure that defects created during handling will be detected and rejected at final pre-seal inspection.

Where low magnification is specified, the manufacturer may at his discretion use high magnification.

1.2.11.2 Pre-assembly inspection

1.2.11.2.1 General

Pre-assembly inspection for hybrid and passive film integrated circuits is given in 1.2.11.2.2, and for unencapsulated semiconductor dice in 1.2.11.2.3.

These inspections shall be carried out prior to assembly of added components, wire bonding and substrate attachment. However, where an inspection item is unimpaired by the assembled added components, it may be carried out at any stage during or after assembly, at the manufacturer's discretion.

1.2.11.2.2 Hybrid and passive film integrated circuits

NOTE. For the purposes of 1.2.11.2.2, the word 'designed' when applied to a nominal minimum or maximum dimension refers to the visual inspection limits derived from the manufacturer's layout design rules which take into account design dimensions and manufacturing tolerances.

The inspection procedure shall be as follows.

a) Basic substrate defects

Inspection of each substrate shall normally be at low magnification. Underlying layers may be inspected using light transmitted through the substrate, where this is possible. For SAW devices, where pattern dimensions less than 5 μm are involved, high magnification shall be used.

Substrates used in the construction of hybrid and passive film integrated circuits shall conform to the requirements given in table 13.

Table 13. Requirements for substrates used in the construction of hybrid and passive film integrated circuits

	Thin film	Thick film	SAW devices
Maximum acceptable number of holes through the substrate except as shown on the design drawing	None	None	
Maximum acceptable length of crack which points towards an operational part of the circuit.	125 μm	125 μm	
For SAW devices, the maximum number of cracks exhibited by any substrate stemming from a cut edge and pointing towards an active area, or any crack within an active area.			None
Minimum acceptable percentage of original design width of operating metallization remaining following reduction by chip out.	75 %	75 %	
For SAW devices, the maximum number of chip outs exhibited by any substrate in the active area			None
Minimum acceptable distance remaining between any crack not pointing towards an active area, and any active area.	25 μm	25 μm	
Substrate having attached portions of another substrate which exceed the substrate dimensions allowed by the assembly drawing.	None	None	
Minimum acceptable percentage of circumference remaining around substrate mounting hole (when designed for substrate to post attachment) after chip out.	75 %	75%	
Minimum acceptable percentage of design separation between metallization and edge of substrate	50 %	50 %	
NOTE. Substrates designed for 'wraparound' conductors need not meet this requirement			
Maximum number of cracks not originating at the substrate periphery of through hole.	None	None	

Metallization involved in the electrical operation of the circuit shall conform to the requirements given in table 14.

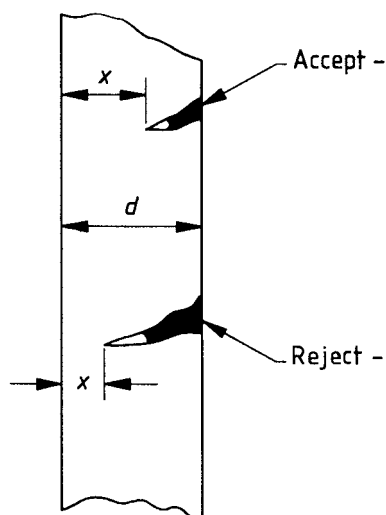
Scratches

Evidence of metallization lifting, peeling or blistering.

95 %

Table 14. Substrate metallization defects (*continued*)

	SAW devices	Thick film	SAW devices
<i>Bridging</i> For non-SAW devices, the minimum acceptable cumulative separation between the designed layout width of unconnected metallization. For SAW devices, a conductive bridge between fingers of different polarity shall be a criterion for rejection unless it can be removed by permissible rework.	2.5 $\mu\text{m}^{1)}$	25 $\mu\text{m}^{1)}$	Conductive bridge
<i>Alignment</i> Alignment between successive film depositions shall be in accordance with the manufacturer's approved layout rule limits.	Rule limits	Rule limits	
<i>Etching</i> For SAW devices, the etching finger-to-gap ratio shall be as defined in the approved design and layout rule limits.			Rule limits
¹⁾ Or 50 % of the approved manufacturer's minimum declared separation, whichever is the greater.			



Scratch exposing underlying dielectric, passivation or substrate where the remaining undisturbed metal width x is not less than $0.5d$.

d = original metal

x = undisturbed metal width

Scratch exposing underlying dielectric, passivation or substrate where the remaining undisturbed metal width x is less than $0.5d$.

Figure 7. Scratch criteria