

Rules

for the preparation of

Detail specifications

for

DIGITAL INTEGRATED CIRCUITS OF ASSESSED QUALITY

FULL ASSESSMENT LEVEL

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AMD 1836

AMENDMENT SLIP No.1 published December 1975 to BS 9490 : 1975.

RULES FOR THE PREPARATION OF
DETAIL SPECIFICATIONS FOR
DIGITAL INTEGRATED CIRCUITS
OF ASSESSED QUALITY:
FULL ASSESSMENT LEVEL

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Additional text

Add the following paragraph to Clause 2 Scope.

The rules in this standard are of a general nature and may be applied to any digital integrated circuits, which cannot be accommodated by any other of the rules in the series BS 9401 et seq.

Revised text

Delete the existing entry for subgroup B2(b) and substitute the following

Rapid change of temperature, followed by: either	1.2.6.13 Rated maximum and minimum T _{stg} values	None
Sealing (fine and gross leak) for cavity packages, or	1.2.6.14	None
Damp heat, cyclic for non-cavity packages	1.2.6.5 Six cycles	None

Revised text

Delete the existing BS 9400 reference for subgroup B3 and substitute the following.

1.2.6.16.1	As appropriate to
to	the terminations of
1.2.6.16.4	the integrated circuit
	under test.

Additional text

Note The tests in subgroups C4(a) and C4(b) may be transferred to subgroups A3(b) and A3(c) respectively, the tests shown in subgroup A3 at 25°C to be included in subgroup A3(a).

AMD 3440

AMENDMENT SLIP No. 2 published and effective from 29th August 1980
to BS 9490: 1975

RULES FOR THE PREPARATION OF DETAIL SPECIFICATIONS FOR DIGITAL INTEGRATED
CIRCUITS OF ASSESSED QUALITY

FULL ASSESSMENT LEVEL

Instructions for the insertion of new and revised pages to BS 9490

Remove page marked clause 2, and substitute revised page marked clause 2

Remove page marked clause 5, and substitute revised page marked clause 5

Remove final page of standard (unmarked) and substitute revised page marked
clause 6(e)

Insert new appendix A (7 pages) following page marked clause 6(e)

2. SCOPE

This British Standard lists the ratings, characteristics, inspection requirements and supplementary information for integrated circuits, which shall be included as minimum mandatory requirements, in accordance with the general rules given in section 2 of BS 9400, in the detail specification for these devices. A complete detail specification is, therefore, a combination of the requirements of both documents. Its purpose is to describe fully the particular integrated circuits so that the detail specification can be used for contractual purposes and for circuit design and equipment maintenance purposes.

Any detail specification prepared in accordance with this standard shall fully describe the type of circuit and its declared application, e.g. monolithic read/write memory circuit, having 64 words 2 bits per word with random access

The rules given in this standard refer primarily to integrated circuits using a sealed package type of encapsulation. They can be used, however, for solid encapsulation (plastics) types of device provided that the modifications listed in 2.2.5 of BS 9400 are included in the detail specifications for these devices.

The rules in this standard are of a general nature and may be applied to any digital integrated circuits, which cannot be accommodated by any other of the rules in the series BS 9401 et seq.

However, for more complex circuits, there are appendices detailing additions and alterations to the main document. A list of these appendices appears immediately after clause 6.

3. LIMITING CONDITIONS OF USE (RATINGS)

Limiting conditions (ratings) are not for inspection purposes.

Values of the limiting conditions of use shall be given as follows:

(a) The limiting values of positive and negative voltages at each terminal referred to a common terminal and any other inter-terminal voltages as appropriate, unless implied by limiting values of currents.

(b) The limiting values of positive and negative currents into each terminal, unless implied by limiting values of voltages.

If these voltages and currents may be exceeded for transient overload the permissible excesses and their durations shall be stated.

(c) The limiting ambient or case operating temperatures (minimum and maximum).

(d) The limiting storage temperatures (minimum and maximum).

(e) The limiting value of continuous total power dissipation over the full operating temperature range (or at 25 °C and power dissipation derating curves), or the limiting value of junction temperature, thermal resistance of junction to case and case to ambient.

(f) Any limiting mechanical or environmental conditions.

Additional ratings may be included at the manufacturer's discretion but in all cases the values of the limiting conditions of use and the conditions under which they apply shall be stated.

Any interdependence of limiting conditions shall be stated.

[Clause 4

If externally connected elements have an influence on the values of the ratings, the ratings should be given for the integrated circuit with the elements connected. Any restrictions on switching sequence of power supplies and duration of sequence shall be stated.

Any other mechanical or environmental ratings or cautionary statements peculiar to a particular integrated circuit, shall be included.

4. RECOMMENDED CONDITIONS OF USE AND ASSOCIATED CHARACTERISTICS

The following recommended conditions of use and associated characteristics shall be given. They shall not be used for inspection purposes except as prescribed in clause 5. They shall apply over the full ambient operating temperature range unless otherwise specified. Where the stated performance of the circuit varies over the ambient operating temperature range the values of the input and output voltages and their associated currents shall be stated at 25 °C and at the extremes of the operating temperature range. Values of current and voltage shall be given for each functionally different type of input and/or output. Timing information shall be given for all inputs or combinations of inputs as necessary for the declared application.

Where correct operation is obtained or operation is intended to be modified by the connection of external elements or networks, the required characteristics of these elements and/or networks, and the range(s) of their values(s) shall be stated. Where appropriate the recommended conditions of use and associated characteristics shall also be given with these elements and/or networks connected.

V_{CC} (V_{SS} , V_{EE} etc.) Maximum and minimum positive and/or negative supply voltage(s)

I_{CC} (I_{SS} , I_{EE} etc.) Maximum supply current(s) at maximum recommended supply voltage(s)

V_{IHA} V_{IHB} Range of HIGH state input voltage which ensures operation of circuit

V_{ILA} V_{ILB} Range of LOW state input voltage which ensures operation of the circuit

V_{OHB} Most negative value of HIGH state output voltage

V_{OLA} Most positive value of LOW state output voltage

$I_{IH(1)}$ Maximum value of HIGH state input current with the input at V_{IHA} (where appropriate)

$I_{IH(2)}$ Maximum value of HIGH state input current with the input at V_{OLB}

$I_{IL(1)}$ Maximum value of LOW state input current with the input at V_{OLA}

$I_{IL(2)}$ Maximum value of LOW state input current with the input at V_{ILB} (where appropriate)

[Clause 5

BS 9490: 1975

I_{OHX}^* I_{OLX}^*	Maximum value of output current (leakage), at V_{OHA} or V_{OLB}
I_{OH}^*	Maximum value of HIGH state output for each output at V_{OHA}
I_{OL}^*	Maximum value of LOW state output current for each output at V_{OLB}
I_{exp}	Maximum value of expander input current(s) (where appropriate)
I_{OS}	Maximum and minimum values of output short-circuit current applicable to only one output at a time (where appropriate)
R_L	Minimum value(s) of output load resistor (where appropriate)
C_{in}	Maximum input capacitance(s) where appropriate
C_{out}	Maximum output capacitance(s) where appropriate
t_{PHL}	Maximum value of HIGH state to LOW state propagation time at 25 °C
t_{PLH}	Maximum value of LOW state to HIGH state propagation time at 25 °C

* I_{OHX} (I_{OLX}) applies only to circuits having open-collector (open-drain) outputs and in this case it replaces I_{OH} (I_{OL}).

Limiting values of critical timing conditions, e.g. clock waveform(s), set-up time, hold time, switching frequency.

NOTE. Current values may be either positive or negative depending on the type of circuit used (i.e. DTL, TTL, ECL, MOS etc.).

5. INSPECTION REQUIREMENTS

The following data shall be given for Groups A, B, C and D inspection requirements.

The inspection levels and AQL to be quoted in the detail specification shall be as specified in 2.2 of BS 9400 unless otherwise stated.

Unless otherwise indicated tests shall be made at 25 °C. (See 1.2.4.1.4 of BS 9400).

Negative values of current shall be so indicated in the detail specification.

[Clause 5, Group A

Inspection	BS 9400 : reference and conditions of test	Limits to be specified at this point
<u>Post-test end-points for subgroup D4</u>	Tests, test conditions and limits as for post-test end-points in group B	
<u>Subgroup D5</u> CTR information	1.1.11 Attributes information for subgroup D4. Measurements information for each test except the verification test before and after the conditioning in subgroup D4 on one input and one output per package (for monolithic circuits) or per chip (for multi-chip circuits)	

NOTE 1. When method 1.2.6.15.1(1) is specified the inspection level should be reduced to S-3.

NOTE 2. Also see 1.1.10 of BS 9400.

6. ADDITIONAL INFORMATION (See 2.1 (8) of BS 9400)

The following information shall be given as minimum design data:

- (a) Diagram(s) showing basic features of operation of the circuit.
- (b) Basic element circuit diagram(s) or, where applicable, a statement of technology; information regarding input and output circuits.
- (c) Loading rules.
- (d) Variation of propagation or other critical times with temperature, and output loading where appropriate.

[Clause 6 e

(e) Input and/or output capacitances where appropriate (e.g. where outputs may be paralleled).

(f) Recommendations for any associated components (e.g. decoupling of power supply to high frequency devices).

(g) Curves or data indicating the effect of externally connected components that influence the characteristics.

(h) Where the power supply current varies significantly with frequency of operation information shall be given on the extent of these variations (by graph or otherwise).

(j) Specification writers should include the maximum temperature which may be permitted to occur on the surface of a device when dissipating maximum power during operation in accordance with the recommended maximum conditions of use.

7. LIST OF APPENDICES

Appendix A. Additional Rules for the preparation of microprocessor specifications.

[Appendix A

APPENDIX A. ADDITIONAL RULES FOR THE PREPARATION OF DETAIL SPECIFICATIONS FOR MICROPROCESSOR INTEGRATED CIRCUITS

A.1 Introduction. This appendix lists the additions and exceptions, for microprocessors, to clauses 3 to 6 of BS 9490.

A.2 Scope of appendix A. This appendix, together with clauses 3 to 6, forms the minimum mandatory requirements for a microprocessor integrated circuit, which is defined as an integrated circuit capable of:

- (a) operating on coded instructions, and
- (b) carrying out, in accordance with the instructions, all of:
 - (1) the acceptance of coded data for processing and/or storage;
 - (2) arithmetic and logical operations on the input data together with any relevant data stored in the internal registers of the microprocessor integrated circuit and/or in external memories;
- (c) the delivery of coded data;
- (c) accepting and/or delivering signals controlling and/or describing the operation or state of the microprocessor integrated circuit.

NOTE. The instructions may be fed in, built in, or held in an internal memory.

Microprocessor integrated circuits which contain alterable non-volatile memories are not fully covered by this appendix. Programming, erasing, and/or reprogramming are covered by the appropriate appendix to BS 9490 for the type of memory.

A.3 Limiting conditions of use. As specified in clause 3.

A.4 Recommended conditions of use and associated characteristics. The following recommended conditions of use and associated characteristics shall be given. They shall not be used for inspection purposes except as prescribed in clause 5. They shall apply over the full ambient operating temperature range unless otherwise specified. Where the stated performance of the circuit varies over the ambient operating temperature range the values of the input and output voltages and their associated currents shall be stated at 25 °C and at the extremes of the operating temperature range.

Values of current and voltage shall be given for each functionally different type of input and/or output. Timing information shall be given for all inputs or combinations of inputs as necessary for the declared application.

[A.4 cont'd.

Where correct operation is obtained, or operation is intended to be modified by connection of external elements, the ranges of values of these elements shall be stated. Where appropriate, the recommended conditions of use and associated characteristics shall also be given with these elements connected.

Direction of current flow may be either positive or negative. Where direction can vary from sample to sample then both positive and negative limits shall be given.

For voltage supplied integrated circuits:

- V_{CC} (V_{SS} , V_{EE} etc.) Maximum and minimum positive and/or negative supply voltage(s)
- I_{CC} (I_{SS} , I_{EE} etc.) Typical and maximum values of average supply current(s) at maximum recommended supply voltage(s) and clock frequencies

For current supplied integrated circuits:

- I_{CC} (I_{BB} , I_{EE} etc.) Maximum and minimum positive and/or negative supply current(s)
- V_{CC} (I_{BB} , V_{EE} etc.) Maximum values of average supply voltage(s) at maximum recommended supply current(s) and clock frequencies

Where appropriate, I_{CC} (I_{SS} , I_{EE} etc.) or, as applicable V_{CC} (V_{SS} , V_{EE} etc.) under standby conditions.

- V_{IHA} * V_{IHB} * Range of HIGH state input voltage which ensures operation of the circuit for each type of input
- V_{ILA} * V_{ILB} * Range of LOW state input voltage which ensures operation of the circuit for each type of input

The maximum value of input clamping voltage, where appropriate.

Maximum, and where appropriate, minimum rise and fall times for each control input signal.

Minimum and maximum values of microprocessor clock period(s) and, where appropriate, any independent clock period(s).

Minimum, and, where appropriate, maximum values of clock pulse duration at each clock input.

[A.4 cont'd.]

For multi-phase clock inputs, minimum and, where appropriate, maximum values of delays between specified edges of successive phases.

$I_{IH(1)}^*$	Maximum value of HIGH state input current with the input at V_{IHA} (where appropriate)
$I_{IH(2)}^*$	Maximum value of HIGH state input current with the input at V_{OHB} (or V_{IHB} if this is more positive)
$I_{IL(1)}^*$	Maximum value of LOW state input current with the input at V_{OLA} (or V_{ILA} if this is more negative)
$I_{IL(2)}^*$	Maximum value of LOW state input current with the input at V_{ILB} (where appropriate)

NOTE. Where clock inputs act as pulsed power supplies then information shall be given for I_{CC} , I_{SS} etc. as appropriate:

V_{OHB}^*	Most negative value of HIGH state output voltage for each type of output
V_{OLA}^*	Most positive value of LOW state output voltage for each type of output
$I_{OHX}^{**} \ I_{OLX}^{**}$	Maximum value of output current (leakage) at V_{OHA} or V_{OLB}
I_{OH}^*	Maximum value of HIGH state output current for each output at V_{OHA}
I_{OL}^*	Maximum value of LOW state output current for each output at V_{OLB} (where appropriate a minimum value shall also be stated)
I_{exp}	Maximum value of expander input current(s) (where appropriate)
I_{OS}	Maximum and minimum values of output short-circuit current applicable to only one output at a time (where appropriate)
$ I_{OZ} $	For three state outputs, the maximum value of output current in the high impedance state

* Where certain terminals may function as inputs or as outputs, then information shall be given for both these conditions.

** I_{OHX} (I_{OLX}) applies only to circuits having open-collector (open drain) outputs and in this case it replaces I_{OH} (I_{OL}).

NOTE. Current values may be either positive or negative depending on the type of circuit used.

[A.5

R_L	Minimum value(s) of output load resistor (where appropriate)
C_{in}	Maximum capacitance(s) of input(s) (including clock) where appropriate
C_{out}	Maximum capacitance(s) of output(s) (including clock) where appropriate

Minimum and/or maximum values as appropriate, of set-up and hold times for each input or group of inputs relative to the appropriate transition of a specified clock pulse or specified output pulse under specified conditions. Values should be stated to enable the critical timing requirements for each independent function of the microprocessor to be established by the user.

Maximum values of propagation times (t_{PHL} and/or t_{PLH}) for each relevant logic path.

Maximum values of output disable and enable times for three - state outputs entering and leaving the off-state condition from a specified clock transition.

Where appropriate, maximum and/or minimum values of transition time t_{THL} and t_{TLH} for each output.

NOTE. Maximum values to be given when typical transition times exceed 50 % of corresponding propagation time, minimum values to be given when typical value is less than 10 ns.

Timing diagrams for control sequences. Minimum durations of input signals and timings relative to the clock signal(s) or specified output signal pulse, necessary to bring the microprocessor into a predetermined state e.g. restart (or reset), interrupt, hold, etc. These should be related to the sequences for execution of programme instructions. These sequences should be expressed in terms of clock cycles and preferably also in terms of machine cycles.

A.5 Inspection requirements. The following data shall be given for Groups A, B, C and D, inspection requirements.

The inspection levels and AQL to be quoted in the detail specification shall be as specified in 2.2 of BS 9400 unless otherwise stated.

Unless otherwise indicated tests shall be made at 25 °C (see 1.2.4.1.4 of BS 9400).

Negative values of current shall be so indicated in the detail specification.

[Group A

Test sequences for electrical tests in subgroups A2, A4 (and where appropriate A3) shall be proposed by the manufacturer and approved by NSI, who shall retain a copy. The sequences to be used shall verify all the instructions specified for the microprocessor, and shall also verify, where appropriate, that the capability of performing the instructions is independent of any previous conditions applied to the microprocessor. In particular, it shall be verified that the reset and interrupt conditions operate correctly irrespective of any previous conditions. The customer shall have access to the test sequences used on application to the manufacturer.

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
<u>GROUP A</u>		Subgroup A5 is not applicable	
<u>Subgroup A0</u> Screening procedures (as applicable)	1.2.9	None	
<u>Subgroup A1</u> Visual inspection	1.2.2	None	
<u>Subgroup A2</u> Verification of description of integrated circuit	1001	V _{CC} (or V _{SS} , I _{CC} , I _{BB} etc., as appropriate) = nominal value	

[Appendix A, subgroup A3]

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
<u>Subgroup A2</u> cont'd		The voltages, currents, sequences and combinations of the input signals and where appropriate, of the instructions applied to the microprocessor and the resulting output waveforms, output data and/or address values as appropriate necessary to verify the intrinsic functions and operation of all externally supplied instructions shall be specified. All outputs shall be tested as appropriate to the various parts of the testing sequences and the output loading conditions shall be specified. The conditions of inputs and outputs not used during any test sequence shall be specified. Values of the essential timing conditions to be used shall be specified	V_{OL} shall be not greater than V_{OLA} and V_{OH} shall be not less than V_{OHB} (as appropriate)
<u>Subgroup A3</u> LOW state output voltage(s), V_{OL} and HIGH state output voltage(s), V_{OH}	2001 2002	V_{CC} (or V_{SS} , V_{EE} , I_{CC} , I_{BB} etc. as appropriate) = specified value for worst-case output level The sequence and combination of input signals to give the appropriate output levels shall be specified. The input levels shall be specified. Preset conditions shall be specified. Output loadings shall be specified. Each output shall be tested V_{CC}	Maximum or minimum as appropriate

[Appendix A, subgroup A3 cont

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
<u>Subgroup A3</u> cont'd			
Output leakage* current I_{OHX} or I_{OLX}	2013	(V_{SS} etc.) = specified value V_{OUT} = specified value (usually V_{CC} maximum) Other conditions as shown for HIGH state output voltage V_{OH} or LOW state output voltage V_{OL} as appropriate	Maximum
Input currents		V_{CC} (or V_{SS} , V_{EE} , I_{CC} , I_{BB} etc. as appropriate) = specified values. All inputs shall be tested. The presetting sequence shall be specified, where appropriate. The conditions of unused inputs shall be specified	
LOW state input current $I_{IL(1)}$ LOW state input current $I_{IL(2)}$ (where appropriate)	2003	V_{IN} = specified value to each input in turn, voltages at other like inputs shall be specified	Maximum
HIGH state input current $I_{IH(2)}$ HIGH state input current $I_{IH(1)}$ (where appropriate)	2004	V_{IN} = specified value to each input in turn, voltages at other like inputs shall be specified	Maximum
Output short-circuit current I_{OS} (where appropriate)	2009	Each output shall be tested separately V_{CC} (or V_{SS} , V_{EE} , I_{CC} , I_{BB} etc. as appropriate) = nominal values	Maximum Minimum

*The output (leakage) current test applies only to open-collector (or open-drain) outputs and in this case it replaces the HIGH state or LOW state output voltage test as appropriate.

[Appendix A, subgroup A3 cont']

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
<u>Subgroup A3</u> cont'd			
Average power supply current(s) $I_{CC}(I_{DD}, I_{BB} \text{ etc.})$ or where appropriate Power supply voltage(s)	2011	The input conditions necessary to cause the appropriate output state to be specified V_{CC} (V_{SS} etc.) = maximum recommended value(s). Inputs, outputs, timing sequence, test pattern shall be specified for: (a) Normal operation and (b) Standby operation, where appropriate I_{CC} (I_{BB} etc.) = specified maximum recommended value(s). Inputs, outputs, timing sequence, test pattern shall be specified for: (a) Normal operation and (b) Standby operation, where appropriate	
Output leakage current I_{OZ} (Three-state outputs only)	2013	V_{CC} (V_{SS}, V_{EE}, I_{CC}, I_{BB} etc. as appropriate) = specified value. The input levels shall be specified. The sequence and combination of input signals to give a HIGH (LOW) output level shall be applied and then the output disabled. The leakage current with V_{ILA} or lower (V_{IHB} or higher) shall be measured	Maximum
Input clamping voltage (where appropriate)	2019	Input current = specified value	Maximum

[Appendix A, subgroup A4

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
<u>Subgroup A4</u>			
Critical timing relationships e.g. set up and hold times	2015	V_{CC} (or V_{SS}, V_{EE}, I_{CC}, I_{BB} etc. as appropriate) = nominal value. The voltages, currents, sequences and combinations of input signals and where appropriate instructions applied to the micro-processor and the resulting output waveforms necessary to produce each intrinsic operational sequence as given in the control sequence timing diagrams shall be specified	Maximum and where appropriate minimum
Switching frequency (clock inputs)		Appropriate values of essential timing conditions shall be used and should be specified. Output loading shall be specified	The outputs being measured shall switch from not greater than V_{OLA} to not less than V_{OHB} or to the high impedance state where appropriate or vice-versa
Propagation times (t_{PHL} and t_{PLH}) for each relevant logic path.	2008	V_{CC} (or V_{SS}, V_{EE}, I_{CC}, I_{BB} etc., as appropriate) = nominal value The voltages, currents and sequences of all input signals required to set up each path shall be specified The duration, repetition frequency, rise and fall times of the input pulse, and the output loading shall be specified The conditions to be applied to unused inputs and/or outputs shall be specified, where appropriate	Maximum values for each path

[Appendix A, Group B

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
<u>Subgroup A4</u> cont'd (Output disable time (Output enable time from a specified clock transition. (for three-state outputs only) Transition times, (t_{THL} and t_{TLH}), for each output, (where appropriate, see clause 4)	2007	Conditions as for propagation times, plus: The relevant clock transition shall be specified V _{CC} etc. = nominal value Duration, repetition frequency, rise and fall times of input pulse and output loading to be specified Any requirements for pre-setting sequence(s) to be specified Conditions of unused inputs and/or outputs to be specified, where appropriate	Maximum values for each Maximum and/or minimum values
<u>GROUP B</u> As for Group B in clause 5			
<u>GROUP C</u> As for Group C in clause 5, except subgroup C6		Delete reference to multi- chip and monolithic	

[Appendix A, Group D

Inspection	BS 9400 Reference	Conditions of test	Limits to be specified
GROUP D			
As for Group D in clause 5 except:			
ADD:			
<u>Subgroup D2</u>			
For MOS circuits and others as appropriate			
Input	2012	VCC (or VSS, VEE, ICC, IBB etc. as appropriate) = specified value.	Maximum
or		Specified applied voltage at input or output as appropriate and frequency if other than 1 MHz	
Output capacitance at each terminal	2012		
<u>Subgroup D5</u>		Delete reference to multi-chip and monolithic	

A.6 Additional information (see 2.1(8) of BS 9400). The following subclauses from clause 6 are relevant (as amended here):

(d) Variation of propagation times, disable times, and other essential timing information given in clause 5, subgroup A4 with temperature shall be given. This information shall also be given, where appropriate with respect to output loading.

NOTE. Variation of times with temperature is not mandatory where limits are stated over the full operating temperature range.

(f) Recommendations for any associated components (e.g. decoupling of power supply to high frequency devices).

(g) Curves or data indicating the effect of externally connected components that influence the characteristics.

[A.6.1]

A.6.1 Block diagram. A block diagram for the microprocessor integrated circuit shall be given. It shall be sufficiently detailed to enable the individual functional units within the microprocessor that are affected by the execution of the instructions to be identified, including any functional blocks that are user programmable. The main data paths between the functional units, and the identification of their external connections, shall also be shown.

Identification of terminals. The following terminals shall be identified on the block diagram:

supply terminals, i.e. terminals intended to be connected to the power supplies;

input or output terminals, i.e. terminals into which or out of which pass signals. The term 'signal' includes pulse and more complex waveforms;

input/output terminals, i.e. terminals which may function at different times as input or output terminals;

three-state output terminals, i.e. output terminals which may be controlled to give a high impedance condition.

A.6.2 Functional description. The following information shall be given:

(a) size, in bits, of external data bus word;

(b) size(s) in bits, of data field(s) that may be processed.

A.6.2.1 Memory addressing range for each type of memory for which a separate addressing procedure is used; e.g. external or internal memory, read/write or read only memory. This may be shown in terms of a memory map. Size in bits of word addressed in each type of memory where this is different from that in the preceding sub-clause.

A.6.2.2 Size in bits of the address.

A.6.2.3 Number, types, and size in bits of internal register(s) both program addressable, or otherwise directly affecting the operation of the microprocessor, e.g. general purpose, accumulator, index, program counter, stack pointer, stack register, control register, arithmetic/logic unit, condition code register.

NOTE. Condition codes indicate results of arithmetic or logic operations such as a zero, carry, parity, sign etc.

A.6.2.4 Mode of memory addressing provided, e.g. immediate, direct, relative, indexed, indirect.

A.6.2.5 Number and type(s) of interrupt capability provided e.g. enabled/disabled, by program, vectored and otherwise.

[A.6.2.6

A.6.2.6 Methods of transferring input and output data and output of addresses, e.g. whether serial, parallel or a combination of both.

A.6.2.7 Indicate if microprogrammable or not.

A.6.2.8 Clock requirements.

A.6.2.9 Operation mode(s). All operation mode(s) (static, dynamic etc.) must be specified.

A.6.3 Instruction set. A comprehensive list shall be given of the instructions which may be performed by the microprocessor. This shall give the instruction code, instruction mnemonic, the operation(s) that result from the execution of the instructions including any condition codes or register contents that are affected, the number of clock cycles and preferably also the number of machine cycles required and, where appropriate, the number of program words used to form the instruction and addressing mode capabilities for each instruction.

This information may be given for each instruction or for each group of similar instructions. Differences should be indicated when these occur due to alternative modes of addressing.

Explanation of addressing modes, and machine cycle shall be given.

A.6.4 Configuration of instruction. The formats of instruction used shall be distinguished, where appropriate, to indicate the bit organization of the machine instructions, e.g. operation code field, address mode field, register definition field, operand field etc.

A.6.5 Input and output signals. The function of each input and output signal shall be tested.

In general the signals may be divided into:

DATA signals

ADDRESS signals

CONTROL signals

A.6.6 Electrical compatability. It shall be stated where the integrated circuit is electrically compatible with other particular integrated circuits or families of integrated circuits or whether special interfaces are required. Details shall be given of the type of output circuit, e.g. three-state, open-collector, etc.

A.6.7 Noise margins. Information about the microprocessor to enable noise margins to be calculated shall be given.

[A.6.8

A.6.8 Application data. Additional information concerning the variations of the characteristics in clause 4 with supply voltage, load impedance, etc., may be given.

Further information, detailing the action of each instruction, may be given to supplement that in 6.4. In particular, this should give details of the sequences and operations involved in program branching and interrupts.

Further information detailing the function and sequences of operations of each input or group of inputs may be given to supplement that in 6.4. This may include state diagrams and timing diagrams.

Information on instruction execution times may be given for particular instructions such as binary addition, register to register transfer where an average time is given, details of the instruction mix should be included.

Information detailing the typical variation of supply current(s) (or, as applicable, voltage(s)) over the specified range of clock frequencies shall be given.

A.6.9 Output loading capability. The maximum number of specified loads that can be driven by an output may be given. This information may be given for more than one type of load.

A.6.10 Other information. A statement should be given when the integrated circuit contains internal protection against high static voltages or electrical fields.

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FULL ASSESSMENT LEVEL

Instructions for the insertion of new and revised pages to BS 9490

Remove page marked clause 2, and substitute revised page marked clause 2

Remove page marked clause 6(e) and substitute revised page marked clause 6(e)

Insert new appendices B (6 pages), C (7 pages) and D (9 pages) following page
marked A.6.8.

BRITISH STANDARD RULES FOR
THE PREPARATION OF DETAIL SPECIFICATIONS FOR
DIGITAL INTEGRATED CIRCUITS OF ASSESSED QUALITY

FULL ASSESSMENT LEVEL

FOREWORD

This standard is the Rules document for digital integrated circuits regardless of the technology employed. It has been prepared using the following notation for digital variables which is particularly useful when dealing with insulated gate circuits requiring positive and negative supplies.

- (a) That range which is closest to positive infinity is to be called the 'H' range.
- (b) That range which is closest to negative infinity is to be called the 'L' range.
- (c) That boundary of any range which is closest to positive infinity is to be called the 'A' value.
- (d) That boundary of any range which is closest to negative infinity is to be called the 'B' value.

The use of this notation avoids the ambiguous use of 'max.' and 'min.'. It has the special advantage that whereas the latter do not have directional connotation, H, L, A and B always signify unambiguous directions.

The use of this notation in detail specifications is not required.

1. INTRODUCTION

This British Standard shall be read and used in conjunction with section 2 of BS 9400: 1970, 'Integrated electronic circuits of assessed quality: generic data and methods of test', which gives the general rules for the preparation of detail specifications for integrated circuits.

The object of the general rules given in section 2 of BS 9400 is to ensure that detail specifications for integrated circuits are broadly similar as regards their subject matter and presentation.

[Clause 2

2. SCOPE

This British Standard lists the ratings, characteristics, inspection requirements and supplementary information for integrated circuits, which shall be included as minimum mandatory requirements, in accordance with the general rules given in section 2 of BS 9400, in the detail specification for these devices. A complete detail specification is, therefore, a combination of the requirements of both documents. Its purpose is to describe fully the particular integrated circuits so that the detail specification can be used for contractual purposes and for circuit design and equipment maintenance purposes.

Any detail specification prepared in accordance with this standard shall fully describe the type of circuit and its declared application, e.g. monolithic read/write memory circuit, having 64 words 2 bits per word with random access.

The rules given in this standard refer primarily to integrated circuits using a sealed package type of encapsulation. They can be used, however, for solid encapsulation (plastics) types of device provided that the modifications listed in 2.2.5 of BS 9400 are included in the detail specifications for these devices.

The rules in this standard are of a general nature and may be applied to any digital integrated circuits, which cannot be accommodated by any other of the rules in the series BS 9401 et seq.

However, for more complex circuits, there are appendices detailing additions and alterations to the main document. A list of these appendices appears immediately after clause 6.

3. LIMITING CONDITIONS OF USE (RATINGS)

Limiting conditions (ratings) are not for inspection purposes.

Values of the limiting conditions of use shall be given as follows:

(a) The limiting values of positive and negative voltages at each terminal referred to a common terminal and any other inter-terminal voltages as appropriate, unless implied by limiting values of currents.

(b) The limiting values of positive and negative currents into each terminal, unless implied by limiting values of voltages.

If these voltages and currents may be exceeded for transient overload the permissible excesses and their durations shall be stated.

(c) The limiting ambient or case operating temperatures (minimum and maximum).

(d) The limiting storage temperatures (minimum and maximum).

(e) The limiting value of continuous total power dissipation over the full operating temperature range (or at 25 °C and power dissipation derating curves), or the limiting value of junction temperature, thermal resistance of junction to case and case to ambient.

(f) Any limiting mechanical or environmental conditions.

Additional ratings may be included at the manufacturer's discretion but in all cases the values of the limiting conditions of use and the conditions under which they apply shall be stated.

Any interdependence of limiting conditions shall be stated.

Inspection	BS 9400 : reference and conditions of test	Limits to be specified at this point
<u>Post-test end-points for subgroup D4</u>	Tests, test conditions and limits as for post-test end-points in group B	
<u>Subgroup D5</u> CTR information	1.1.11 Attributes information for subgroup D4. Measurements information for each test except the verification test before and after the conditioning in subgroup D4 on one input and one output per package (for monolithic circuits) or per chip (for multi-chip circuits)	

NOTE 1. When method 1.2.6.15.1(1) is specified the inspection level should be reduced to S-3.

NOTE 2. Also see 1.1.10 of BS 9400.

6. ADDITIONAL INFORMATION (See 2.1 (8) of BS 9400)

The following information shall be given as minimum design data:

- (a) Diagram(s) showing basic features of operation of the circuit.
- (b) Basic element circuit diagram(s) or, where applicable, a statement of technology; information regarding input and output circuits.
- (c) Loading rules.
- (d) Variation of propagation or other critical times with temperature, and output loading where appropriate.

[Clause 6 e

- (e) Input and/or output capacitances where appropriate (e.g. where outputs may be paralleled).
- (f) Recommendations for any associated components (e.g. decoupling of power supply to high frequency devices).
- (g) Curves or data indicating the effect of externally connected components that influence the characteristics.
- (h) Where the power supply current varies significantly with frequency of operation information shall be given on the extent of these variations (by graph or otherwise).
- (j) Specification writers should include the maximum temperature which may be permitted to occur on the surface of a device when dissipating maximum power during operation in accordance with the recommended maximum conditions of use.

7. LIST OF APPENDICES

- Appendix A. Additional rules for the preparation of detail specifications for microprocessors.
- Appendix B. Additional rules for the preparation of detail specifications for MOS static memories, including read-only (ROM) and read/write memories.
- Appendix C. Additional rules for the preparation of detail specifications for ultra-violet light-erasable electrically programmable read-only memories.
- Appendix D. Additional rules for the preparation of detail specifications for MOS read/write dynamic memories.

[Appendix A

APPENDIX B. ADDITIONAL RULES FOR THE PREPARATION OF DETAIL SPECIFICATIONS FOR MOS STATIC MEMORIES, INCLUDING READ-ONLY (ROM) AND READ/WRITE MEMORIES

B.1 Introduction. This appendix lists the additions and exceptions, for MOS Static Memories (no data refresh internal or external required) to clauses 3 to 6 of BS 9490.

B.2 Scope of appendix B. This appendix, together with clauses 3 to 6, forms the minimum mandatory requirements for static integrated circuit memories. It includes memories which may use more than one 'enable' or 'chip-select' control signal but excludes programmable read-only memories. The terms 'enable' and 'chip-select' are often used synonymously, and the former term is used throughout this appendix.

B.3 Limiting conditions of use. As specified in clause 3.

B.4 Recommended conditions of use and associated characteristics. The following recommended conditions of use and associated characteristics shall be given. They shall not be used for inspection purposes except as prescribed in clause 5. They shall apply over the full ambient operating temperature range unless otherwise specified. Where the stated performance of the circuit varies over the ambient operating temperature range the values of the input and output voltages and their associated currents shall be stated at 25 °C and at the extremes of the operating temperature range. Values of current and voltage shall be given for each functionally different type of input and/or output. Timing information shall be given for all inputs or combinations of inputs as necessary for the declared application.

Where correct operation is obtained, or operation is intended to be modified by connection of external elements, the ranges of values of these elements shall be stated. Where appropriate, the recommended conditions of use and associated characteristics shall also be given with these elements connected.

Direction of current flow may be either positive or negative. Where direction can vary from sample to sample, then both positive and negative limits shall be given.

Where any of the timing parameters apply only in specific circumstances, an explanatory note shall be given.

[B.4(a)]

(a) For voltage supplied integrated circuits:

V_{CC} (V_{DD} , V_{BB} etc.) Maximum and minimum positive and/or negative supply voltages

I_{CC} (I_{DD} , I_{BB} etc.) Maximum values of average supply current(s) at maximum recommended supply voltage(s) and the appropriate cycle repetition frequencies normally max) to give maximum supply current

(b) Where appropriate I_{CC} (I_{DD} , I_{BB} etc.) Maximum value and/or V_{CC} , (V_{DD} , V_{BB} etc.) Minimum value under standby conditions

*(c) V_{IHA} V_{IHB} Range of HIGH state input voltage which ensures operation of the circuit for each type of input

*(d) V_{ILA} V_{ILB} Range of LOW state input voltage which ensures operation of the circuit for each type of input

*(e) $|I_{IH}|$ Maximum value of input leakage current with the input at V_{IHA}

*(f) $|I_{IL}|$ Maximum value of input leakage current with the input at V_{ILB}

*(g) V_{OHB} Most negative value of HIGH state output voltage for each type of output at associated I_{OH}

*(h) V_{OLA} Most positive value of LOW state output voltage for each type of output at associated I_{OL}

(j) $|I_{OZ}|$ For three state outputs, maximum value of output leakage current in the high impedance state at maximum specified supply voltage(s)

* Where certain terminals may have more than one function then information shall be given for each of these functions.

[B.4(k)]

(k) I_{OHX} (I_{OLX}) Maximum value of output leakage current at V_{OHA} (V_{OLB})

NOTE. I_{OHX} (I_{OLX}) applies only to circuits having open drain outputs and in this case it replaces I_{OH} (I_{OL}).

(l) Timing diagrams shall be given, to comprise a complete set of signals which show the operation of each mode of the circuit. Any time intervals additional to those required by this clause of the appendix which need to be known by the user to ensure the correct operation of the memory should be stated, e.g. operation during and after leaving the standby condition.

(m) Where appropriate, maximum and/or minimum rise and fall times for each input signal required by the memory.

(n) Maximum value of capacitance of each input (including control) terminal at specified value of supply voltage(s) and terminal voltage.

(p) Maximum value of capacitance of each output terminal at specified value of supply voltage(s) and terminal voltage.

(q) Where appropriate, maximum and/or minimum values of transition time t_{THL} and t_{TLH} for each output under specified load conditions.

NOTE. Maximum values to be given when typical transition time exceeds 50 % of propagation time, minimum values to be given when typical value is less than 10 ns. If both these conditions apply, both maximum and minimum values should be given.

(r) Maximum values for output disable time from the end of each relevant 'enable' signal.

NOTE. 'Output disable time' is the time interval between the cessation of a specified 'enable' signal and the instant at which the output enters the 'off state'.

(s) Where appropriate, the maximum value of the disable and enable times for the three-state outputs entering and leaving the off-state condition measured from the relevant transition of output enable.

(t) Minimum values for the following cycle times.

(1) For read-only and read-write memories:

(i) read.

(2) Additional for read-write memories:

(i) write;

(ii) read-write;

(iii) read-modify-write (where appropriate).

[B.4(u)]

(u) Maximum values for the following access times:

- (1) from start of each enable (see note);
- (2) from start of read (where appropriate);
- (3) from valid address (see note).

NOTE. This time is not applicable to memories with latched address inputs.

(v) Minimum, and where appropriate, maximum values for the following pulse durations.

(1) For read-only and read-write memories:

- (i) enable (where appropriate).

(2) Additionally for read-write memories only:

- (i) write.

(w) Minimum values for the following set-up times.

(1) For read-only and read-write memories:

- (i) valid address before start of enable (where appropriate).

(2) Additionally for read-write memories only:

- (i) valid address before start of write;
- (ii) start of enable before end of write (where appropriate);
- (iii) data in before end of write;
- (iv) data in before end of enable (where appropriate).

(x) Minimum values for the following hold times.

(1) For read-only and read-write memories:

- (i) valid address after end of enable (where appropriate).

[B.4 continued

(2) Additionally for read-write memories only:

- (i) data in after end of write;
- (ii) valid address after end of write;
- (iii) enable after end of write (where appropriate);
- (iv) write after end of enable (where appropriate);
- (v) data in after end of enable (where appropriate).

(y) Minimum time for which data remains valid:

- (1) after end of enable;
- (2) after address is no longer valid;
- (3) after end of output enable (where appropriate).

(z) Minimum values for the following delay time.

(1) For read-write memories with common input/output terminals:

- (i) data input after end of read (where appropriate)

B.5 Inspection requirements. The following data shall be given for groups A, B, C and D, inspection requirements.

The inspection levels and AQL to be quoted in the detail specification shall be as specified in 2.4 of BS 9400 unless otherwise stated.

Unless otherwise indicated tests shall be made at 25 °C (see 1.2.4.1.4 of BS 9400).

Negative values of current shall be so indicated in the detail specification.

[Appendix B, group A

Inspection	BS 9400 reference	Conditions of test.	Limits to be specified
GROUP A			
<u>Subgroup A0</u>			
Screening procedures (as applicable)	1.2.9	None	
<u>Subgroup A1</u>			
Visual inspection	1.2.2	None	
<u>Subgroup A2</u>			
Verification of the description of the memory	1001	V_{CC} (or V_{DD}, V_{BB} etc. as appropriate) - Nominal value The voltages, currents, sequences and combinations of the input signals, and the resulting output waveforms necessary to verify each functional operation of the memory, shall be specified. All outputs shall be tested as appropriate to each functional check, and the loading conditions shall be specified. The conditions of inputs and/or outputs not used during any test sequence shall be specified The timing sequence(s) used shall be in accordance with those specified under B.4(1)	V_{OL} not greater than V_{OLA} and V_{OH} not less than V_{OHB} (as appropriate)

[Appendix B, subgroup A3

Inspection	BS 9400 reference	Conditions of test	Limits to be specified
<u>Subgroup A3</u>			
Input leakage current:		V_{CC} (or V_{DD} , V_{BB} etc. as appropriate) = specified value. All inputs shall be tested. The presetting sequence shall be specified, where appropriate. The conditions of unused inputs shall be specified	
High state input leakage current $ I_{IH} $	2013	$V_{IN} = V_{IHA}$ to each input in turn, voltages at other like inputs shall be specified	Maximum
Low state input leakage current $ I_{IL} $	2013	$V_{IN} = V_{ILB}$ to each input in turn, voltages at other like inputs shall be specified	Maximum
Average power supply current(s) I_{CC} (I_{DD} , I_{BB} etc)	2011	V_{CC} (or V_{DD} , V_{BB} etc. as appropriate) = maximum recommended value(s). Inputs, outputs, timing sequence, test pattern shall be specified under specified conditions for: (a) normal operation, (b) standby operation where appropriate	Maximum
Output voltage:		V_{CC} (or V_{DD} , V_{BB} etc. as appropriate) = specified value for worst case output level The input levels shall be specified. The sequence and combination of input signals to give the appropriate output levels shall be specified	

[Appendix B, subgroup A3
(Continued)]

Inspection	BS 9400 reference	Conditions of test	Limits to be specified
<u>Subgroup A3</u> (contd.)			
Low state output voltage(s) V_{OL}	2001	I_{OL} to be specified	Maximum
High state output voltage(s) V_{OH}	2002	I_{OH} to be specified	Minimum
*Output leakage current $ I_{OHX} $	2013	V_{CC} (or V_{DD} , V_{BB} etc. as appropriate) = specified value Other conditions as shown for High state output voltage V_{OH} V_{OUT} = specified value (usually V_{CC} max)	Maximum
Output leakage current $ I_{OZ} $ (Three state outputs only)	2013	V_{CC} (or V_{DD} , V_{BB} etc. as appropriate) = specified value The input levels shall be specified. The sequence and combination of input signals to give HIGH (LOW) output level shall be applied and then the output disabled. The leakage current V_{ILA} or lower (V_{IHB} or higher) shall be measured	Maximum

* The output leakage current test applies only to open drain outputs and in this case it replaces the High state output test.

[Appendix B, subgroup A4

Inspection	BS 9400 reference	Conditions of test	Limits to be specified
GROUP B As in BS 9490 except: <u>Subgroup B7</u> Electrical endurance	1.2.7	Dynamic test circuit to be specified Electrical conditions applied to all terminals to be specified Duration and temperature to be specified	None
GROUP C As in BS 9490 - except subgroup C6		Delete reference to multichip and monolithic	
GROUP D As in BS 9490 - except: ADD <u>Subgroup D2</u> Input capacitance (for each input and functional control terminal) Output capacitance <u>Subgroup D5</u>	2012 2012	V_{CC} (or V_{DD}, V_{BB} etc. as appropriate) = specified value Specified applied voltage at input or output as appropriate and frequency if other than 1 MHz Delete reference to multichip and monolithic	Maximum

[B.6.1

Inspection	BS 9400 reference	Conditions of test	Limits to be specified
<u>Subgroup A4</u>			
Critical timing relationships		V_{CC} (or V_{DD} , V_{BB} , etc. as appropriate) = specified value. The voltages, currents and sequences of all input signals shall be specified. Sequences shall be in accordance with the specified timing diagrams. Appropriate values of essential timing conditions shall be specified. Output loading shall be specified. The conditions applied to the unused inputs and/or outputs shall be specified as appropriate. Worst case set up, hold times etc. as for Recommended conditions of use (not necessarily applied simultaneously)	Maximum Maximum
<u>Read</u> Access time: (a) from address (b) from each enable	2022		
Disable time from the end of each enable signal	2023	Conditions as for Access time	Maximum
'OFF state' enable and disable times (for three-state output only)	2021	Conditions as for Access time	Maximum
Data valid times	2022	Conditions as for Access time	Minimum
Transition times (where appropriate)	2007	V_{CC} (or V_{DD} , V_{BB} etc. as appropriate) = specified value. Duration, repetition frequency, rise and fall times of input pulses and output loading to be specified. Any requirements for presetting sequence(s) to be specified. Conditions of unused inputs and/or outputs to be specified where appropriate	Maximum and/or minimum value

[Appendix B, group B

B.6 Additional information (see 2.1.8 of BS 9400). The following information shall be given as minimum design data.

B.6.1 Block diagram. A block diagram or equivalent circuit information for the integrated circuit shall be given. The block diagram shall be sufficiently detailed to enable the individual functional units within the memory (e.g. 'Address decode', 'chip enable', 'buffer' output circuits, etc.) to be identified, together with their external connections.

B.6.2 Functional description. The functions performed by the circuit shall be specified, and the following information shall be stated:

- (a) the total number of bits of information capable of being stored in the memory circuit;
- (b) the number of bits per word capable of being stored in the memory circuit;
- (c) the method of addressing (e.g. multiplexed, latched, etc.);
- (d) the functions(s) performed by each terminal.

B.6.3 Loading rules. Information on the output loading capability shall be given.

B.6.4 Temperature and loading variation. Typical variation of access times, disable times, and other essential timing information given in B.5, subgroup A4 with temperature shall be given. This information shall also be given, where appropriate with respect to output loading.

NOTE. Variation of times with temperature is not mandatory where limits are stated over the full operating temperature range.

B.6.5 Noise margins. Information shall be given to enable noise margins to be calculated.

B.6.6 Electrical compatibility. It shall be stated whether the integrated circuit memory is electrically compatible with other particular integrated circuits or families of integrated circuits, or whether special interfaces are required.

B.6.7 Power supplies. Where appropriate information shall be given of the typical variation of power supply current(s) (or, as applicable, voltage(s)), over the specified range of control signal frequencies (including pulsed supplies where appropriate).

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