

**Harmonized system of quality assessment
for electronic components**

**Capability detail specification:
Multilayer printed boards**

ICS 31.180

Committees responsible for this British Standard

The preparation of this British Standard was entrusted to Technical Committee EPL/52, Printed circuits, upon which the following bodies were represented:

British Telecommunications plc
Electrical and Electronic Insulation Association
Federation of the Electronics Industry
GAMBICA (BEAMA Ltd.)
Institute of Metal Finishing
Ministry of Defence
National Supervising Inspectorate (BSI PC)
Printed Circuit Interconnection Federation
Surface Mount and Related Technologies (SMART) Ltd.

This British Standard, having been prepared under the direction of the Electrotechnical Sector Board, was published under the authority of the Standards Board and comes into effect on
15 April 1996

© BSI 1998

The following BSI references relate to the work on this standard:
Committee reference EPL/52
Draft announced in
BSI News, July 1995

ISBN 0 580 25425 9

Amendments issued since publication

Amd. No.	Date	Text affected
9807	February 1998	Indicated by a sideline in the margin

Summary of pages

The following table identifies the current issue of each page. Issue 1 indicates that a page has been introduced for the first time by amendment. Subsequent issue numbers indicate an updated page. Vertical sidelining on replacement pages indicates the most recent changes (amendment, addition, deletion).

Page	Issue	Page	Issue
Front cover	2	3/26	2
Inside front cover	2	4/26 - 8/26	original
a	1	9/26	2
b	blank	10/26 - 26/26	original
i	2	26a/26 - 26f/26	1
ii	2	Inside back cover	original
1/26	original	Back cover	original
2/26	2		

Contents

	Page
Cooperating organizations	Inside front cover
Foreword	ii
1 General	1
2 Capability qualifying component (CQC)	1
3 Capability approval	3
4 Capability test programme	3
5 Additional capability	4
6 Traceability	4
Table I Capability approval test schedule	5
Table IIa Additional metallic conductor finishes	10
Table IIb Additional contact finishes	14
Table III Permanent organic finishes	15
Table IV Bonded heatsinks	17
Appendix A Test pattern for marking inks	19
Appendix B Test pattern for solder masks	20
Appendix C Test pattern for bonded heatsinks	21
Appendix D Untitled	22

National foreword

This British Standard has been prepared by Technical Committee EPL/52. It is a capability detail specification (CapDS) within the CECC system and should be read in conjunction with BS EN 123300. This edition includes Amendment 1 to BS CECC 23300-003 : 1991 and reflects industry requirements by reducing the permitted failures to zero and increasing the range of metallic finishes.

It has been produced to reflect the capability levels established in the United Kingdom for the supply of printed boards to the defence, computer, communications and similar industries over many years. It is generally equivalent to that defined by BS 9000 *General requirements for a system for electronic component of assessed quality*, and in particular by BS EN 123300 : 1992 *Harmonized system of quality assessment for electronic components: Sectional specification: Multilayer printed boards*.

The capability level defined is enhanced compared to that described by BS EN 123300-800 : 1992. In particular capability has been extended to include the following:

- a) more surface finishes, now split into two groups and referred to the connector area and the remainder of the board respectively;
- b) more metallic finishes;
- c) solder resistant organic finishes;
- d) marking inks;
- e) bonded heatsinks;
- f) accelerated ageing;
- g) additional capability in the definition of minimum conductor and spacing widths; traceability.

Figures 1 to 4 have been reproduced by kind permission of the Institute for Interconnecting and Packaging Electronic Circuits (IPC), 2215 Sanders Road, Northbrook, Illinois 60062-6135, USA.

Cross-references

Publication referred to	Corresponding British Standard
EN 123000 : 1991	BS EN 123000 : 1992 <i>Harmonized system of quality assessment for electronic components: Generic specification: Printed boards</i>
EN 123200 : 1992	BS EN 123200 : 1992 <i>Harmonized system of quality assessment for electronic components: Sectional specification: Single and double sided printed boards with plated through holes</i>
EN 123300 : 1992	BS EN 123300 : 1992 <i>Specification for harmonized system of quality assessment for electronic components: Sectional specification: Multilayer printed boards</i>
IEC 68 series	BS 2011 series <i>Environmental testing</i>
IEC 249 series	BS EN 60249 series <i>Base materials for printed circuits</i>
ISO 1463 : 1981	BS 5411 <i>Methods of test for metallic and related coatings — Part 5 : 1984 Measurement of local thickness of metal and oxide coatings by the microscopical examination of cross-sections</i>
ISO 3543 : 1981	Part 12 : 1981 <i>Beta backscatter method for measurement of thickness</i>

There is no British Standard equivalent to CECC 00010 : 1980 which comprises a list of the tests in IEC 326-2 and its supplement IEC 326-2A. A related British Standard to IEC 326-2 and its supplements is BS 6221 : Part 2 and its amendments.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

1 General

1.1 Scope

This Capability Detail Specification is based on BS EN 123300. It relates to multilayer printed boards made with materials and surface finishes as specified in 2.

1.2 Object

To specify the Capability Qualifying Component 'CQC', its characteristics to be tested, the test methods and conditions to be applied and the requirements to be fulfilled for testing basic and extended capability.

2 Capability Qualifying Component (CQC)

Test boards to be used as CQCs for basic capability shall

- be made from a combination of the materials specified in 2.1 of this Capability Detail Specification. The construction shall be as given in 8.3 of EN 123300.
- bear the composite test pattern (CTP) specified in 8.2 of EN 123300, (or equivalent composite test pattern), for basic and other metallic finishes; CTPs as specified in 8.2 of CECC 23200 are to be used to demonstrate organic surface finishes and external bonded heat sinks.
- have one of the surface finishes specified by groups 11, 12, 13 14, 15, 16 or 17 in 2.2 of this Capability Detail Specification.

Test boards to be used as CQCs for additional capability shall be modified to demonstrate the claimed capability - see 5.

2.1 Materials

Material group designation	Specification IEC	Base material		Base material thickness range mm	Cu-thickness μm
		Type	Grade		
A	249-2-11	Epoxide woven glass	General purpose	0.05...0.8	18, 35, 70, 105
	249-2-12	Epoxide woven glass	Defined flammability		
	249-3-1G	Pre-preg	General purpose	≥ 0.05	n.a.
	249-3-1GF	Pre-preg	Defined flammability		

2.2 Surface finishes

2.2.1 Metallic finishes

Finish group designation	Surface finish	Abbreviation for QPL
11	Bare copper	Cu
12	Copper with temporary protective coating	Cu(tpc)
13	Copper with oxide	Cu(CuO)
14	Tin, tin-lead	Sn, SnPb
15	Tin-lead (fused)	SnPb(f)
16	Tin-lead (dipped and levelled)	SnPb(dl)
17	Immersion Gold over electroless nickel	AuNi(smt)
21	Specimen K 5 μm min. gold plated on copper remainder using finish group 11 - 17 (see below)	5 Au/Cu, Cu, Sn, SnPb
22	Specimen K 0.7 μm min. gold plate on nickel remainder using finish group 11 - 17 (see below)	0.7 Au/Ni, Cu, Sn, SnPb
23	Specimen K 2.5 μm min. gold plated on copper remainder using finish group 11 - 17 (see below)	2.5 Au/Cu, Cu, Sn, SnPb
24	Specimen K 2.5 μm min. gold plate on nickel remainder using finish group 11 - 17 (see below)	2.5 Au/Ni, Cu, Sn, SnPb

The demonstration of metallic finish groups 21, 22, 23 or 24 shall be combined with a finish from groups 11, 12, 13, 14, 15, 16 or 17. Each claimed combination of metallic finishes shall be tested separately.

2.2.1.1 Accelerated ageing

The ability of finishes from groups 11, 12, 13, 14, 15, 16 or 17 to solder after extended or adverse storage conditions is demonstrated using accelerated ageing. This test shall be carried out on those finishes where accelerated ageing is claimed. Each finish that has complied with the requirements of the accelerated ageing test is highlighted by the inclusion of an asterisk (*) adjacent to that finish in the manufacturers abstract of capability as published in the QPL.

2.2.2 Organic finishes

Finish group designation	Organic finish	Abbreviation for QPL
a	Dryfilm solder mask	DSM
b	Wet resist solder mask	WSM
c	Liquid photo polymer solder mask	LSM
d	Marking inks	MI

The demonstration of organic finish groups a, b, c or d shall be over a finish from groups 11, 12, 13, 14, 15, 16 or 17. All claimed types of solder resist and marking ink shall be tested separately.

2.3 Variant designation

The combination of any material group designated in 2.1 and any of the surface finishes as designated in 2.2 constitutes a variant. The variant is designated by the combination of material and finish group designations e.g. A12(b) or A12/21(c).

2.4 External bonded heatsinks

Each heatsink material for which approval to bond to a printed wiring board is required shall be separately assessed. All types of heatsink adhesive systems shall be separately assessed.

3 Capability approval

3.1 Range of capability approval

Capability approval granted on the testing of one variant is valid within the limits specified in 3.7 of EN 123000 for

- metal-clad base material within one group designation, all base material thicknesses and all foil thicknesses of the material in accordance with 2.1; and
- all metallic surface finishes within one surface finish group as quoted in 2.2.1, that is

finish group 11	covers finish group 11 only
finish group 12	covers finish group 11 and 12
finish group 13	covers finish group 11 and 13
finish group 14	covers finish group 11 and 14
finish group 15	covers finish group 11 and 15
finish group 16	covers finish group 11 and 16
finish group 17	covers finish group 17 only
finish group 21	covers finish group 21 only
finish group 22	covers finish group 22 and 24
finish group 23	covers finish group 21 and 23
finish group 24	covers finish group 24 only

3.2 QPL information

The QPL information shall be given in accordance with 3.4 of EN 123000 and shall contain the following details relative to the Capability Detail Specification.

- Reference to the CECC Generic Specification : 123000
- Reference to the CECC Sectional Specification : 123300
- Reference to the BS CECC Capability Detail Specification : BS CECC 23300-003
- Base material for which approval is granted as given in 2.1
- The surface finishes for which approval is granted as given in 2.2
- Any additional capability, 3.5.3 of EN 123000 refers

4 Capability test programme

Each separate process shall be assessed within the test programme.

4.1 Capability demonstration

Capability shall be demonstrated by using 9 composite test patterns (CTPs) of one variant from each material group claimed. Testing shall be in accordance with Table I.

4.1.1 Other metallic surface finishes

If claimed, other metallic surface finishes, as designated in 2.2.1, shall be demonstrated by the manufacture of 3 CTPs plus sufficient extra A and H specimens to meet the requirements of Table II. Testing shall be in accordance with Table II.

Note:- The maximum claimed active board size for the finish shall be demonstrated.

4.1.2 Organic surface finishes

Each claimed organic surface finish, as designated in 2.2.2, shall be demonstrated by the manufacture of 3 CTPs, complying with 8.2 of EN 123200 (PTH), using the pattern specified in Appendix A (marking inks) or Appendix B (solder masks). Testing shall be in accordance with Table III.

4.1.3 External bonded heatsinks

Each bonded heatsink and adhesive system shall be demonstrated by the manufacture of 3 CTPs, complying with 8.2 of EN 123200 (PTH), using the pattern specified in Appendix C. Testing shall be in accordance with Table IV.

4.1.4 Demonstration of impedance control

Special CQCs shall be constructed in accordance with figure 5 of Appendix D7 of this Capability Detail Specification, configured as either a 'stripline' or 'microstrip'. Demonstrations shall be made for the following variants, as required and defined by the approved manufacturer:

- each base material type (e.g. woven glass epoxide);
- each impedance geometry (microstrip, stripline);
- each impedance extreme, and a 50 Ω mandatory demonstration;
- conductor width and lateral separation minima;
- each metallic surface finish.

Tolerances at 50 Ω and each impedance extreme shall be claimed prior to demonstration, and achieved.

For each solder resist type and thickness claimed, impedance value derating factors shall be declared.

Impedance control shall be shown on the capability approval certificate as a separate appendix.



5 Additional capability

Maximum number of layers - For boards with seven or more layers the construction shall be equivalent to that given for six layers with thickness and tolerances proportion to the number of layers incorporated.

Maximum active board size (mm) - length and breadth - see 8.3 of EN 123300.

Plated-through hole diameters - specimen C (microsection coupon) of CTP employed

minimum drilled hole diameter, use 2 mm pads

minimum clearance diameter, use 2.5 mm pads

Maximum aspect ratio -
$$\frac{\text{nominal base material thickness for maximum number of layers}}{\text{minimum drilled hole diameter}}$$

Minimum conductor width and spacing - Specimen F of CTP to be modified to provide additionally 5 conductors and 4 spacings, each of the claimed minimum. Initial foil thickness of less than 35 μm may be used for this demonstration but this thickness shall be declared. Different minima may be declared and demonstrated for inner and outer layers.

6 Traceability

Traceability of all test specimens to the original production panel shall be maintained. The method used to identify individual test specimens shall not affect the test results.

Table I
Capability Approval Test Schedule

Characteristics	Test No. CECC 00 010	Specimen of CECC Composite Test Pattern	Number of specimens		Test Conditions	Requirements/Material		Remarks
			Required	Failures Permitted		249-2- 4 (glass)	249-2- 5 (glass)	
GENERAL EXAMINATION	(before subdivision into specimens)							
Visual inspection								
Conformity and identification	1	Complete CQC	All CQCs	0		Pattern, material and finishes shall comply with this Capability Detail Specification. Any identification for traceability purposes shall be verified.		
Appearance and workmanship	1a	Complete CQC	All CQCs	0		The boards shall appear to have been processed in a workmanlike manner, in accordance with good current practice. The base material, conductors, metallic surface finishes and temporary organic coatings shall be of uniform appearance. They shall be free from cracks, burns, pits, nodules and blisters. Metallic surface finishes shall be free of scratches which penetrate to an underlying surface.		
Plated-through holes	1a	Complete CQC	All CQCs	0		Plated-through holes shall be clean and free from inclusions of any sort that could affect component insertion and solderability. Plating voids are permissible provided their total area does not exceed 10% of the total wall area. The largest dimension shall not exceed 25% of the hole circumference in the horizontal plane and 25% of the thickness of the board in the vertical plane. Plated-through holes shall have no plating voids at any interface of hole wall and external land. The interface shall be considered to extend into the holes below the surface of the board a distance of one and a half times the total copper thickness on the surface. There shall be no circumferential cracks of the copper, or circumferential separation of the copper from the wall in the plated-through hole. Holes with plating voids shall not exceed 5% of the total number of plated-through holes.		
Conductor defects	1b	Complete CQC	All CQCs	0		There shall be no breaks in conductors intended to be continuous. The presence of local defects e.g. nicks and pinholes, shall not reduce the conductor width by more than 25%. The length of a defect shall not be greater than the nominal conductor width. Indentations in conductors, other than those in edge board contacts, shall not be a reason for rejection of the printed board.		
Particles between conductors	1b	Complete CQC	All CQCs	0		There shall be no conductive material bridging conductors shown as intended to be mutually unconnected by the composite test pattern. Residual particles are permissible provided the leakage path is not reduced by more than 20%.		

Table I (Cont.)

Characteristics	Test No. CECC 00 010	Specimen of CECC Composite Test Pattern	Number of specimens		Test Conditions	Requirements/Material		Remarks
			Required	Failures Permitted		249-2- 4 (glass)	249-2- 5 (glass)	
Edge connector defects	2a	K	All specimens	0		The surface of edge board contacts within the contact zone shall be smooth and free from pitting or scratches penetrating their surface finish. Within the contact zone of each contact there shall be no more than one indentation or bump as defined in Appendix D1.		
Dimensional examination								
Board dimensions	2	Complete CQC	All CQCs	0		CQC outline dimensions and thickness as claimed.		NOTE: Thickness measurement of boards shall exclude added metallic and organic coatings.
Flatness	12a	Complete CQC	All CQCs	0		The radius of curvature shall not be less than: 3000 mm		
Board thickness in the zone of edge board contacts	2	K	All specimens	0		1.6 ± 0.2 mm (6 to 8 layers only).		NOTE: Not applicable to boards with more than 8 layers.
Holes	2	Complete CQC	All CQCs	0		Hole diameter shall comply with 8.2 of EN 123300, or as claimed, with a tolerance of ± 0.1 mm.		
Misalignment of hole and land	1a, 2a	Complete CQC	All CQCs	0		There shall be no breakout from the land perimeter. There shall be no interruption of the junction between the land and connecting conductor.		
Conductor width	2a	F	All specimens	0		Conductor widths greater than or equal to 0.25 mm shall not deviate from nominal values by more than + 0.08/- 0.05 mm. Conductor widths less than 0.25 mm nom. shall be within the manufacturers declared tolerance.		Conductor defects and particles between conductors shall be disregarded when evaluating conductor width and spacing - see 'Visual inspection'. Artwork for CTPS may need etch factor allowances to meet these requirements.
Conductor spacing	2a	F	All specimens	0		Conductor spacings of 0.5 mm nom. shall not be below 0.42 mm. Conductor spacings of 0.25 mm nom. shall not be below 0.17 mm. Conductor spacings less than 0.25 mm nom. shall be within the manufacturers declared tolerance.		
SPECIFIC EXAMINATION	(after subdivision into specimens)							
Electrical tests								
Change of resistance, plated-through holes	3c	D	6	0	5 immersions of 260 °C	Increase between first and last 25 °C immersion = 10% max. Increase between first and last 260 °C immersion = 10% max. Increase during any one 260 °C immersion = 120% max.		NOTE: Thermal shock may be applied using either method 19a or 19b.
Change of resistance, inter- connections	3c	L	6	0	5 immersions of 260 °C	Increase between first and last 25 °C immersion = 10% max. Increase between first and last 260 °C immersion = 10% max. Increase during any one 260 °C immersion = 120% max.		NOTE: Thermal shock may be applied using either method 19a or 19b.