

**Harmonized system of quality
assessment for electronic components**

Technology Approval Schedule: Film and hybrid integrated circuits

ICS 31.180

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the CECC title page, pages 2 to 30 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

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Technology Approval Schedule: Film and hybrid integrated circuits



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European Committee for Electrotechnical Standardization
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Foreword

This Technology Approval Schedule was prepared under the auspices of CENELEC/TC CECC/SC 47AX, Film and hybrid integrated circuits.

The original text was formulated by members of the UK ONS and the current owner of the document is:

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It is based, wherever possible, on Publications of the International Electrotechnical Commission and International Standards Organization, and in particular, on ISO 9000.

The text of this TAS was circulated to the CECC for acceptance in accordance with clause **2.10** of CECC 00111-VIII (RP11-8).

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Introduction

The requirements for Technology Approval of manufacturers of electronic and electromechanical components are given in RP 14-VI. The procedures for approval defined in that RP require the manufacturer to have available an appropriate Technology Approval Schedule (TAS).

This schedule defines how the principles and requirements of RP 14-VI are applied to Film and Hybrid Integrated Circuits

It is intended for film and hybrid integrated circuit manufacturers who can demonstrate continuous process control, usually by statistical means, and continuous quality improvement. It is therefore best suited to the high volume, low complexity manufacturer. For low volume, high complexity custom hybrid manufacturers the Capability Approval procedures as defined in EN 165000-1 are more suited.

It is recognized that the technologies covered by this TAS are broad and diverse. Each manufacturer may have his own methods of satisfying the contents of this specification. The sections identified shall be considered when forming the Description of Technology in the Technology Approval Declaration Document (TADD — refer to Annex B). Other documentation may be referred to and made available to cover the requirements of this TAS.

1 General

1.1 Scope

This TAS specifies the terms, definitions, symbols, quality system, test, assessment and verification methods and other requirements relevant to the design, manufacture and supply of Film & Hybrid Integrated Circuits in compliance with the general requirements of the CECC System for electronic components of assessed quality. It should be read in conjunction with EN 165000-1 — *Generic Specification*, which contains details on the test methods referenced herein.

NOTE The Self-Audit Checklist of EN 165000-3 is required to be completed and verified by the ONS prior to the commencement of Technology Approval.

Where specified, the manufacturer shall include the requirements of this TAS in his TADD, refer to Annex B.

1.2 Related documents

IEC 60068, *Environmental tests*.

IEC 60749, *Mechanical and climatic test methods*.

EN ISO 9000, *Quality System*.

EN 165000, *Film and Hybrid Integrated Circuits — Part 1: Generic specification: capability approval procedure — Part 2: Internal visual inspection and special tests — Part 3: Self-audit checklist and report for film and hybrid integrated circuit manufacturers — Part 4: Customer information, product assessment level schedules and blank detail specification*.

CECC 00007, *Sampling Plans and Procedures for Inspection by Attributes*.

EN 100114-I, *Approval of manufacturers and other organizations*. (RP 14-I)

CECC 00114-V, *Process Approval of Specialist Contractors within the Electronics Industry*. (RP 14-V)

CECC 00114-VI, *Technology Approval of Electronic Component Manufacturers*. (RP 14-VI)

CECC 00111, *CECC specifications*. (RP 11)

EN 100015, *Protection of Electrostatic Sensitive Devices*.

CECC 00016, *Basic requirements for the use of Statistical Process Control (SPC) in the CECC system*.

CECC 00200, *Register of Approvals*.

CECC 00300, *List of European Standards (Ens), CECC Publications and Related National Documents*.

CECC 00400, *Handbook for the production of CECC documents*.

CECC 00401, *Glossary of terms*.

ECQAC 1120, *Harmonized system of quality assessment for electronic components. ECQAC requirements for the drafting of qualification approval and capability approval test reports*¹⁾.

ECQAC 1220, *Harmonized system of quality assessment for electronic components. ECQAC policy for uncertainty of measurements*¹⁾.

1.3 Units, symbols and terminology

Units, graphical symbols, letter symbols and terminology shall, wherever possible, be taken from the following documents:

ISO 1000, *SI units and recommendations for use of their multiples and of certain other units*.

IEC 60027, *Letter symbols to be used in electrical technology*.

IEC 60050, *International electrotechnical vocabulary*.

IEC 60617, *Graphical symbols for diagrams*.

EN 165000, *Generic specification: Film and Hybrid Integrated Circuits Capability Approval Procedure*.

Any other units, symbols and terminology peculiar to one of the components covered by a generic specification, shall be taken from the relevant IEC or ISO documents listed under “Related Documents”, where not given in 1.5.

1.4 Standard and preferred values

Where practical, values should be selected from the following:

- a) dimensions : IEC 191-2
- b) temperatures: – 65, – 55, – 40, – 25, – 10, 0, + 5, + 25, + 40, + 55, + 70, + 85, + 100, + 125, + 150 °C.

1.5 Definitions

In addition to the general requirements of 1.3.1, for the purposes of this specification and associated blank detail specifications, the following definitions apply:

added component

any component added to a hybrid film integrated circuit which is not formed on the surface of the substrate

NOTE Added components are incorporated components.

burn-in

a non-destructive procedure designed to screen out early lifetime failures. Burn-in is an accelerated conditioning with a device under its operating electrical load at an elevated temperature, which is generally the maximum operating temperature that does not exceed the thermal rating of the device

custom built

a qualifying term for a circuit manufactured to a specific customer's requirements

electrical endurance

a procedure similar to burn-in, but of extended duration. Electrical endurance may be considered destructive or non-destructive dependent upon duration and severity

embedding

a process using resins which can be hardened to produce a body embedding the circuit, for example:

- casting;
- potting;
- dip-coating;
- transfer moulding.

¹⁾ available from CENELEC/CS in Brussels

film integrated circuit

an integrated circuit whose circuit and elements, including the interconnections, are film elements formed on the surface of an insulating substrate

hybrid film integrated circuit

a film integrated circuit in which the main part of the circuit elements are produced in-situ as film circuit elements on a substrate, and which is completed by added components mounted on the substrate or elsewhere in the package

measurement uncertainty

a statement of the limits of the range within which the true value of the measurement is expected to lie in relation to the recorded result, with a defined confidence level

multilayer film circuit

a circuit of more than one layer of film interconnection, separated by at least one insulating film or gap

part-finished

a qualifying term for a film integrated circuit or hybrid film integrated circuit taken uncompleted from a production line. It cannot be completely assessed to the specification applicable in its normal finished state

package

total or partial envelope of an integrated circuit which provides:

- mechanical protection;
- environmental protection;
- outline dimensions.

the package may also contain or provide terminals and contribute to the thermal characteristics of the integrated circuit

process test vehicle (PTV)

a device or test structure used to verify, analyze or monitor processes or electrical/physical attributes

product assessment level schedules (PALS)

define the minimum circuit process and test requirements for the different market sectors/operating environments

qualification circuit (QC)

a circuit which is representative of circuits manufactured to declared and identical processes and used for approval tests to one of the Product Assessment Level Schedules (PALS)

screening

examination or testing applied to all products in a lot for the purpose of detecting and removing potential failures

2 Definition of the circuit technology

2.1 Scope

Film and hybrid integrated circuits may be considered to belong to two principal technology types/build standards:

- i) devices containing solder-attached and/or chip-and-wire components which are unencapsulated or non-hermetically encapsulated;
- ii) devices which are hermetically sealed or contain components that are individually hermetically sealed.

There are eleven Product Assessment Level Schedules (PALS) applicable to film & hybrid integrated circuits intended for release under this TAS. (refer to EN 165000-4)

Devices that fall into category i), above, may be assessed under PALS 1 to PALS 5, and devices in category ii) may be assessed under PALS 6 to PALS 11.