

Harmonized system of quality assessment for electronic components — Generic specification: Discrete semiconductor devices

UDC 621.382

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The preparation of this British Standard was entrusted by the Electronic Components Standards Committee (ECL/-) to Technical Committee ECL/12, upon which the following bodies were represented:

- British Broadcasting Corporation
- British Telecommunications plc
- Electronic Components Industry Federation
- Electronic Engineering Association
- GAMBICA (BEAMA Ltd.)
- National Supervising Inspectorate
- Telecommunication Engineering and Manufacturing Association (TEMA)

The following bodies were also represented in the drafting of the standard, through subcommittees and panels:

- Engineering Equipment and Materials Users Association
- UK Optical Sensors Collaborative Association

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National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with CENELEC Electronic Components Committee (CECC) 50000 Issue 4 “*Harmonized system of quality assessment for electronic components: Generic specification: Discrete semiconductor devices*” as amended by CECC amendments No. 1 (1987), No. 2 (1988) and No. 3 (1991).

This standard gives the terminology, quality assessment procedures and test and measurement conditions applicable to the entire family of discrete semiconductor devices. It also includes in Appendix II the general inspection requirements for semiconductor devices (see also 3.5.2).

This standard is a harmonized specification within the CECC system. The existing non-harmonized British Standard, BS 9300:1969 “*Specification for semiconductor devices of assessed quality: Generic data and methods of test*”, will eventually be superseded by this standard, but for a period both standards will remain in force because of current approvals to BS 9300. BS CECC 50000:1981, which is superseded by this revision, is withdrawn.

This standard specifies the use of substances and/or test procedures that may be injurious to health if adequate precautions are not taken. It refers only to technical suitability and in no way absolves either the supplier or the user from statutory obligations relating to health and safety at any stage of manufacture or use.

The fourth issue of CECC 50000 results from amendments and additions that have been agreed since Issue 3 was published. Because of the number of pages affected by these amendments, it was decided that it would be clearer to publish a fourth issue rather than an amendment sheet.

Terminology and conventions. The text of the CECC specification has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards; attention is particularly drawn to the following.

The comma has been used throughout as a decimal marker. In British Standards it is current practice to use a full point on the baseline as the decimal marker.

Cross-references. The British Standard harmonized with CECC 00100 and CECC 00101 to CECC 00103 is BS 9000 “*General requirements for a system for electronic components of assessed quality*” Part 1: “*Specification of basic rules and procedures*”, Part 2: “*Specification for national implementation of CECC basic rules and rules of procedure*”.

International Standards	Corresponding British Standards
ISO 497:1973	BS 2045:1965 <i>Preferred numbers</i> (Technically equivalent)
ISO 1000:1973 ^a	BS 5555:1976 <i>SI units and recommendations for the use of their multiples and of certain other units</i> (Identical)
IEC 68	BS 2011 <i>Basic environmental testing procedures</i> (The relevant separately published Parts are all identical.)
IEC 117	BS 3939 <i>Guide for graphical symbols for electrical power, telecommunications and electronics diagrams</i> (All separately published Parts are identical)
IEC 148:1969	BS 3363:1980 <i>Letter symbols for semiconductor devices and integrated microcircuits</i> (Identical)
CECC 00007:1973	BS E9007:1975 <i>Harmonized system of quality assessment for electronic components: Basic specification: Sampling plans and procedures for inspection by attributes</i> (Identical)

^a Now superseded by ISO 1000:1981, the identical British Standard for which is BS 5555:1981

Related British Standards for IEC 27, IEC 50, IEC 147, IEC 191 and IEC 410:1973 are BS 5775, BS 4727, BS 9300, BS 3934 and BS 6001:1972 respectively. A related British Standard for ISO 2015 is BS 4760:1971.

There is at present no corresponding British Standard for IEC 134. The Technical Committee has reviewed the provisions of IEC 134, to which reference is made in the text, and has decided that they are acceptable for use in conjunction with this standard.

A British Standard does not purport to include all the necessary provisions of a contract. Users of British Standards are responsible for their correct application.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, the CECC title page, pages ii to vi, pages 1 to 82, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

English version

Harmonized System of Quality Assessment for
Electronic Components

GENERIC SPECIFICATION:

DISCRETE SEMICONDUCTOR DEVICES

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION GNERIQUE:

DISPOSITIFS DISCRETS A SEMICONDUCTEURS

Harmonisiertes Gütebestätigungssystem für
Baelemente der Elektronik

FACHGRUNDSPEZIFIKATION:

EINZEL- HALBLEITERBAUELEMENTE



4

Issue
Edition
Ausgabe

CECC 50 000

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Foreword

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for "DISCRETE SEMICONDUCTOR DEVICES". It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification, the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and the United Kingdom.

Preface

The new issue of this generic specification was prepared by CECC Working Group 5 "SEMICONDUCTOR DIODES AND TRANSISTORS" in conjunction with Working Group 7 "RECTIFIER DIODES AND THYRISTORS". It is based whenever possible on the Publications of the International Electrotechnical Commission (IEC) and in particular on those referred to under "related documents".

The amendments with respect to Issue 3 were submitted to the Vote in CECC (Secretariat)... documents whose numbers are given below and the relevant reports on the Voting were ratified by the President of the CECC for printing as a CECC specification; for ease of comparison with issue 3, a short reference to the items affected is also given.

Document	Voting		Report on Voting		Affects
1107	Dec.	1981	1169	§ 4.3.4	Non operative F.E.T.
1134	March	1982	1211	§ 2.5	Marking (general)
1143	April	1982	1212	§ 4.3.4 + 4.5.2.11	D-051 to D-056 (current reg. diodes)
1185	Aug.	1982	1267	App. VI § 1	Screening
1713	July	1985	1841	§ 2.6	Ordering inform. (levels)
1714	July	1985	1842	§ 3.5.5	Certified test records
1721	July	1985	1848	§ 4.3.4	T-031 to T-033 (matched transistors)

Implementation

This issue 4 replaces issue 3 (1980) and its corrections or amendments. THERE ARE NO CHANGES IN FORMER CLAUSE NUMBERS AND NO FORMAL NEED TO AMEND IMMEDIATELY EXISTING DETAIL SPECIFICATIONS PROVIDED THAT:

- 1) they effectively comprise, as was indicated in the preface of issue 3 and in CECC 50001 given as an example, a Sub-Group A2a on non-operatives (the old A2 having become A2b), which was not always understood nor done;
- 2) the ONH and ONS, having left a reasonable time for action, effectively check that the amendment to the "marking", clause 2.5 (letter for level of quality assessment and, if applicable, screening sequence) is implemented in practice.

Section 1. Scope

This document applies to discrete semiconductor devices, namely diodes, transistors, rectifier diodes and thyristors. It does not apply to:

- stacks or assemblies made with these components
- some devices of high power or devices when only small quantities are required, in which case the limitation of the scope will be given in the relevant blank detail specifications.

Section 2. General

2.1 Order of precedence

Where any discrepancies occur, documents shall rank in the following order of precedence, provided that the generic, blank detail and detail specifications have been prepared in accordance with the requirements of the system:

1. The Internal Regulations of the FEN e.V (Association for the Promotion of Electrotechnical Standardization)
2. Detail specification
3. Relevant generic and blank detail specification
4. CECC Rules of Procedure and other documents to which reference is made
5. Basic specifications

The same order of precedence shall apply to equivalent national documents.

2.2 Related documents

ISO 497	(1973)	Guide to the choice of series of preferred numbers and of series containing more rounded values of preferred numbers
ISO 1000	(1973)	S.I. units and recommendations for the use of their multiples and of certain other units
ISO/R 2015	(1971)	Numbering of weeks
IEC 27	(latest issue)	Letters symbols to be used in electrical technology (several parts)
IEC 50	(latest issue)	International Electrotechnical Vocabulary
IEC 68	—	Basic environmental testing procedures, namely:
IEC 68-1	(1978)	Part 1: General
IEC 68-2-2	(1974)	] Dry heat Test Ba
IEC 68-2-2A	(1976)	
IEC 68-2-3	(1969)	Damp heat, steady state, Test Ca
IEC 68-2-30	(1980)	Damp heat, cyclic, Test Db
IEC 68-2-6	(1970)	Vibration (sinusoidal), Test Fc
IEC 68-2-7	(1968)	Acceleration, steady state, Test Ga
IEC 68-2-14	(1974)	Change of temperature, Tests Na, Nb and Nc
IEC 68-2-17	(1978)	Sealing, Tests Qc, Qk and Ql
IEC 68-2-20	(1979)	Soldering, Test T
IEC 68-2-21	(1975)	Robustness of terminations, Test U
IEC 68-2-27	(1972)	Shock, Test Ea
IEC 68-2-38	(1974)	Composite temperature/humidity cyclic Test Z/AD
IEC 68-2-45	(1980)	Immersion in cleaning solvents, Test XA
IEC 117	(latest issue)	Recommended graphical symbols (several parts)
IEC 134	(1961)	Rating systems for electronic tubes and valves and analogous semiconductor devices

IEC 147	(latest issue) Essential ratings and characteristics of semiconductor devices and general principles of measuring methods (all relevant parts)
IEC 148	(latest issue) Letter symbols for semiconductor devices and integrated micro-circuits (several parts)
IEC 191	(latest issue) Mechanical standardization of semiconductor devices (several parts)
IEC 410	(latest issue) Sampling plans and procedures for inspection by attributes (see also CECC 00007)
CECC 00007	(latest issue) Basic specification: Sampling plans and procedures for inspection attributes
CECC 00101 to CECC 00113	(latest issue) Rules of procedures, and especially referred to:
CECC 00107	(latest issue) RP7: Quality Assessment Procedures
CECC 00108	(latest issue) RP8: Attestation of conformity
CECC 00109	(latest issue) RP9: Certified Test Records
CECC 00111	(latest issue) RP11: Specifications and their Harmonization

NOTE Up-dating of IEC 68 and IEC 147 references is under consideration

2.3 Units, symbols and terminology

Units, graphical symbols, letter symbols and terminology shall, whenever possible, be taken from the following documents:

ISO 1000, *S.I. units and recommendations for the use of their multiples and of certain other units*.

IEC 27, *Letter symbols to be used in electrical technology*.

IEC 50, *International electrotechnical vocabulary*.

IEC 117, *Recommended graphical symbols*.

IEC 148, *Letter symbols for semiconductor devices and integrated micro-circuits*.

Where further items are required they shall be derived in accordance with the principles of the documents listed above.

2.4 Preferred values of ratings and characteristics

Preferred values of voltages and currents for characteristics shall conform to IEC 147-0 B, sub-clauses **3.5.1** and **3.5.2**.

Preferred nominal values and limits of voltages in the E 24 series for voltage regulator and reference diodes shall be as given in IEC 147-0 B, sub-clause **3.5.3**.

2.5 Marking

The following shall be marked on the device, in the following order of precedence, as space permits. All the information, except the terminal marking, shall appear on the primary pack used as initial protection or wrapping for delivery:

- 1 Terminal identification (2.5.1)
- 2 Type designation (2.5.2)
- 3 Date code (2.5.4) and/or:
factory identification code or manufacturer's name or trade-mark (2.5.3)
- 4 Mark of Conformity unless a Certificate of Conformity is used

*In addition, the primary pack shall be marked with the detail specification reference, followed by the letter defining the level of quality assessment (App. II A/B) and, if applicable by the letter identifying the screening sequence (App. VI)

Example: CECC 50002-000 E-C

NOTE The detail specification shall prescribe the information actually marked on the device

2.5.1 Terminal identification (reference IEC 147-0 B, sub-clauses 3.8 and 3.9)

The terminals shall be identified in at least one of the following ways:

- in accordance with the specified outline or base drawing
- in accordance with one of the methods given in 2.5.1.1, 2.5.1.2 or 2.5.1.3
- as specified in the detail specification

2.5.1.1 Diodes

Polarity of diodes shall be clearly indicated by one or more of the following methods:

- the rectifier arrow graphical symbol pointing towards the cathode
- a colour code as follows:

Diodes in A20 (IEC 191-2) and smaller outlines:

These diodes shall be marked with a contrasting colour band or dot at the cathode end. Alternatively, when the type is identified by coloured bands, the cathode end may be identified by the use of a double width band for the first digit. If there is a possibility of the colour code at the cathode end of diodes in envelopes smaller than A1B (IEC 191-2) being confused with a type marking, then the latter shall be omitted.

Diodes in outlines larger than A20:

Red shall be used for the cathode.

2.5.1.2 Transistors

When so specified in the detail specification, transistor terminals shall be identified by the following colour code:

Collector terminal	Red
Emitter terminal	Blue
Base terminal	Yellow

Fourth terminal if present:

- if connected to collector, emitter or base: the relevant colour of this electrode
- if connected to anything else (for instance a shield): uncoded

When it is appropriate to identify only one terminal, the collector shall be marked.

2.5.1.3 Thyristors

The thyristors terminals shall be indicated by one of the following methods:

- The thyristor graphical symbol with the arrow directed towards the cathode terminal
- A colour code as follows:

Cathode terminal(s)	Red
and/or	
Anode terminal(s)	Blue (or black)
Gate terminal(s)	Yellow (or white)

2.5.2 Type designation

The type designation shall be given preferably in letters and figures or, when specified, with one of the colour codes hereafter.

2.5.2.1 For JEDEC type numbers

The following code is applicable to the “number” part the type designation (the number following 1N or 2N) and to the possible suffix letter following this number.

The numbering sequence shall be from left to right, the left being signified by either a wider colour band or a placement of the colour group towards the left side of the body.

Two-digit numbers shall be preceded by a zero.

Colour	Digit	Suffix letter
Black	0	none
Brown	1	A
Red	2	B
Orange	3	C
Yellow	4	D
Green	5	E
Blue	6	F
Purple (violet)	7	G
Grey	8	H
White	9	J

2.5.2.2 For PRO-ELECTRON type numbers

The following alternative methods are applicable to small diodes:

Prefix		Serial	Version letter
Method I 2 broad bands		Number	(if any)
Method II Body colour		Method I: narrow bands.	Method II: one broad band, followed by narrow band(s)
AA. — brown	Z. — white	0. — black	A. — brown
BA. — red	Y. — grey	1. — brown	B. — red
	X. — black	2. — red	C. — orange
	W. — blue	3. — orange	D. — yellow
	V. — green	4. — yellow	E. — green
	T. — yellow	5. — green	F. — blue
	S. — orange	6. — blue	G. — violet
		7. — violet	H. — grey
		8. — grey	J. — white
		9. — white	

The cathode side is indicated by the broad band(s).

2.5.2.3 Any other type numbers

The colour code used shall be defined in the detail specification, with the digits 0 to 9 indicated by the same colours as in the above codes.

2.5.3 Manufacturer's name or trade-mark

Where the certificate of conformity enables traceability to a manufacturer's factory, the manufacturer's name or trade-mark is sufficient. In all other cases, the factory identification code shall be used.

2.5.4 Date code system

The date code system is as ISO/R 2015 for the week, preceded by the last two digits of the year (example: 7245 — 45th week of 1972).

2.6 Ordering information

Unless otherwise specified, the following minimum information is necessary to order a given device:

- precise type number
- CECC reference of detail specification (see note 1), with issue number and/or date when relevant
- level of quality assessment as defined in Appendix II (see note 2) and, if required, screening sequence as defined in Appendix VI
- when taped components are required, reference shall be made to IEC 286
- any other particulars

Example: 1N 000 to CECC 50001-000, issue 2, level F

NOTE 1 When the intention is to have within the System several types of discrete semiconductor devices falling within the same family, for instance obtained by a selection of the values of electrical characteristics, such types should preferably be grouped in a single detail specification, which shall bear a single CECC reference number.

NOTE 2 When the intention is to allow the same discrete semiconductor device to be ordered according to different levels of quality assessment, such levels should preferably be given in a single detail specification which shall bear a single CECC reference number.

Section 3. Quality assessment procedures

The quality assessment tests are subdivided into Group A and Group B tests that are performed lot-by-lot, and Group C tests that are performed periodically.

3.1 Manufacturing stages and conditions for manufacturer's approval

3.1.1 Approval of manufacturers

A manufacturer wishing to obtain manufacturer's approval shall meet the requirements of CECC 00107 and shall state the category of devices for which he seeks approval (see Section 1 Scope).

3.1.2 Primary stage of manufacture

The primary stage of manufacture for bipolar semiconductor devices is the first process which changes the monocrystalline semiconductor material from being either wholly P-type or wholly N-Type.

The primary stage of manufacture for MOS devices is the first oxydation.

3.1.3 Extension of manufacturer's approval

A manufacturer may have his approval extended to cover a factory of his company, located in a country which does not have an approved ONS for the technical area concerned, whether this country is a CECC member country or not, provided that the conditions of CECC 00107-I, § 2, § 7 and § 8.6 are met. Either the primary or one or more subsequent manufacturing stages (including qualification approval and capability approval testing, quality conformance inspection or both) may be performed in an approved manufacturer's factory located in a non-CECC member country.

3.1.4 Subcontracting of manufacturing stages

An approved manufacturer may subcontract either the primary or one or more subsequent manufacturing stages (but excluding qualification approval and capability approval testing and quality conformance inspection) to non-approved manufacturers provided that the conditions of CECC 00107-I § 7 are met.

3.2 Definition of a production lot

Unless otherwise stated, a production lot (hereinafter referred to as "lot") consists of devices having the same design, manufactured on the same production line, only differing by a selection based on electrical characteristic limits, and normally produced during one week.

NOTE 1 After this selection has been made, the lot can be divided into sub-lots of types, on which structural similarity can apply.

NOTE 2 Attention is also drawn to the clause of CECC 00107 relevant to the formation of inspection lots.

3.3 Structurally similar devices

The crucial criterion for the grouping of types of devices as structurally similar is that the differences between the various types have no influence on the results of the test for which the group has been formed. To simplify the practical operation of inspection schemes, a more restricted definition is adopted for the purpose of this document.

Structurally similar devices are produced by one manufacturer, with essentially the same design, materials, processes and methods. They only differ because of manufacturing variations usually resulting in their classification into types having different electrical characteristics.

For the purposes of obtaining samples both for qualification approval and for quality conformance testing, discrete semiconductor devices may be grouped as described hereafter.

3.3.1 Electrical characteristic tests in Groups A and/or C

Components having the same device design, manufactured on the same production line but differing only by a selection based on electrical characteristic limits shall be divided into sub-lots of types according to these different electrical characteristic limits.

Such components should preferably be included in the same detail specification but in any case the details of the grouping used shall be explained in the qualification approval test report.

3.3.1.1 Different electrical characteristic limits

For those particular tests where different electrical characteristic limits apply for each of the sub-lots, then each sub-lot shall be sampled with a sample size appropriate to the number of components in each sub-lot.

Examples of such particular tests are:

- the selection of diodes into various sub-lots with different voltage ratings
- the selection of transistors into various sub-lots with different “forward current transfer ratio” limits
- the selection of rectifier diodes into various sub-lots with different voltage ratings.
- the selection of thyristors into various sub-lots with different voltage ratings.

3.3.1.2 Identical electrical characteristic limits

For those particular tests where the same electrical characteristic limit and test conditions apply for all the sub-lots, then the total lot shall be assessed by testing either:

- a single sample, of a size appropriate to that for the total lot, comprising equal or proportionate quantities of all the sub-lots, or
- a single sample, of a size appropriate to that for the total lot, taken at random from the total lot.

An example of such a particular test is the forward voltage-drop test for all the reverse voltage rated types of diodes, where the same limit applies to all types.

3.3.2 Environmental tests in Groups B and/or C

Components which have been encapsulated by the same method, have the same basic type of internal mechanical structure, have used the same* piece parts and have been subjected to common sealing and finishing processes, may be considered as structurally similar, as described below, and a single sample, of a size appropriate to that of the total lot, taken to assess the total lot of such similar components.

* NOTE “same” means that the piece parts meet the same requirements at the incoming inspection.

3.3.2.1 Components made on the same production line

The tests to which the above grouping can apply are:

- Visual inspection
- Dimensions
- Solderability, soldering heat
- Robustness of terminations
- Corrosion (for instance damp heat, steady state)
- Change of temperature and accelerated damp heat (or sealing)
- Vibration
- Acceleration (steady state)
- Shock.

An example of such components are various types of transistors made on the same production line and encapsulated in a case made with the same piece parts.

3.3.2.2 Components made on different production lines

The tests to which the above grouping can apply are limited to:

- Visual inspection
- Dimensions
- Solderability, soldering heat
- Robustness of terminations
- Corrosion (for instance damp heat, steady state).

3.3.3 Endurance test

For endurance tests such as:

- Electrical endurance
- Storage at high temperature,

components having the same device design, manufactured on the same production line but differing only by a selection based on electrical characteristic limits, shall be divided into sub-lots of types according to those different electrical characteristic limits. Devices from one of these Sub-lots may be used for electrical endurance tests in accordance with 3.3.3.1 or 3.3.3.2.

Such devices should preferably be included in the same detail specification but in any case the details of the grouping used shall be declared in the qualification approval test report.

3.3.3.1 When the tests are specified in Group B lot-by-lot

1) For all devices except Voltage Regulator and Voltage Reference diodes,

the total lot may be assessed for each type of endurance test by taking a single sample of a size appropriate to that of the total lot, from any one sub-lot provided that:

- a) the total quantity of devices in the sub-lot chosen together with the total quantity of devices in all the other sub-lots which have either a lower rating or a less severe characteristics limit, comprise not less than 60 % of the total lot size of all the sub-lots, and
- b) the following additional tests shall be performed once every three months for the sub-lot with either the highest rating or the most severe electrical characteristics limit, using a sample size appropriate to the average lot size during the three months period:
 - electrical endurance for 168 h
 - storage at high temperature for 1 000 h (when specified in blank detail specification)

Example: Sub-lots of diodes having V_R max = 20; 50; 75; 150; 200 V

with relevant quantities: $N_1; N_2; N_3; N_4; N_5$

The total lot may be assessed, for instance, by sub-lot $V_R = 75$ V provided that

- a) $N_1 + N_2 + N_3 \geq 60 \% (N_1 + N_2 + N_3 + N_4 + N_5)$ and that
- b) Sub-lot $V_R = 200$ V be especially assessed every three months.

2) For Voltage Regulator and Voltage Reference Diodes only,

the total lot may be assessed by taking a single sample, of size appropriate to that of the total lot, from the sub-lot containing the greatest number of components.

3.3.3.2 When the tests are only specified in Group C — periodic

For each type of endurance test, the total lot may be assessed by taking a single sample, of the size specified in the blank detail specification, preferably from the sub-lot containing the greatest number of components, but also assuring adequate rotation of other types over a longer period.

3.3.4 NOTE The application of the rules of 3.3 are illustrated in the diagrams of Appendix I.

3.4 Qualification and capability approval procedures

3.4.1 Qualification approval procedure

Qualification approval may be given provided the results of the Group A, B and C tests on one lot are within the limits prescribed in the relevant detail specification.*

The sample size for qualification approval shall be the minimum size for the applicable sampling conditions which lead to an acceptance criterion of one defect.

The qualification report shall include a complete record of all the test results and measured values.

* NOTE If required by the blank detail or detail specification, a Group D inspection is provided, containing such tests that are additional to those of Groups A, B and C. They are only for the purpose of qualification approval or requalification as indicated in CECC 00107. This "Group D", however, does not form a sequence of tests as such and the detail specification shall specify which of the Group D, tests is (are) applicable to a given device, where appropriate.

3.4.2 Capability approval procedure

See Appendix VII

3.5 Quality conformance inspection

3.5.1 Division into Groups and Sub-Groups

Group A inspection (lot-by-lot)

This Group prescribes the visual inspection and the electrical measurements to be made on a lot-by-lot basis to assess the principal properties of a device.

Group A inspection is divided into appropriate sub-groups as follows:

Sub-group A1:

This Sub-Group comprises visual inspection, and polarity inspection when specified.

Sub-Group A2:

This Sub-Group comprises those measurements which are of primary importance for verifying the description of the device; it may be subdivided to assess non-operative devices.

Sub-Group A3/A4:

These Sub-Groups may not be required. When they are required, they shall comprise those measurements which are of secondary importance for verifying the description of the device.

The choice between Sub-Groups A3 or A4 for given measurements shall be governed by the desirability to perform them at given sampling requirements, but shall also take into account whether the measurements can be made automatically on a large sample or shall be performed manually, but on a reduced number of specimens.

Group B inspection (lot-by-lot)

This Group prescribes the procedures to be used on a lot-by-lot basis to assess certain additional properties of the device, and includes mechanical, climatic and electrical endurance tests which can be completed in less than one week.

Group C inspection (periodic)

This Group prescribes the procedures to be used on a periodic basis to assess certain additional properties of the device, and includes electrical measurements, mechanical, climatic and endurance tests which are appropriate for checking at periodic intervals, generally three months or longer.

Samples for periodic tests shall be drawn from lots which have been accepted in Group A and B tests. Furthermore, the individual specimens shall have passed those Group A measurements called for in the failure criteria.

In the event of failure at Group C inspection the procedure as defined in CECC 00107 shall be followed.

Division of Group B and Group C inspection into Sub-Groups

For ease of comparison, and to facilitate change from Group B to Group C and vice versa when necessary (see 3.5.3), the tests in these Groups have been divided among Sub-Groups which bear the same number for corresponding tests.

The division is as follows:

Sub-Groups B1/C1:

Comprise those measurements which control the dimensional interchangeability of the device.

Sub-Groups B2a/C2a:

Comprise those measurements which assess the electrical properties of the device which are of a design nature.

Sub-Groups B2b/C2b:

Comprise those measurement which further assess, by measurement under different conditions of voltage, current or temperature, some of the electrical characteristics of the device already measured in Group A.

Sub-Groups B2c/C2c:

Comprise verification of limiting values of the device, where appropriate.

Sub-Groups B3/C3:

Comprise those tests which are intended to assess the mechanical robustness of the terminations of the device (for instance stud torque, lead bending).

Sub-Groups B4/C4:

Comprise those tests which are intended to assess the ability of the device to be soldered.

Sub-Groups B5/C5:

Comprise those tests which are intended to assess the ability of the device to withstand climatic stresses (for instance change of temperature).

Sub-Groups B6/C6:

Comprise those tests which are intended to assess the ability of the device to withstand mechanical stresses (for instance vibration).

Sub-Groups B7/C7:

Comprise those tests which are intended to assess the ability of the device to withstand long term humidity.

Sub-Groups B8/C8:

Comprise those tests which are intended to assess the failure characteristics of the device under endurance testing.

Sub-Groups B9/C9:

Comprise those tests which are intended to assess the electrical properties of the device under storage conditions at extremes of temperature.

Sub-Groups B10/C10:

Comprise those tests which are intended to assess the performance of the device during variations of air-pressure, if required.

Sub-Groups RCE:

List a selection of the tests and/or measurements done in the preceding Sub-Groups, the results of which are to be presented in the Certified Test Records.

3.5.2 Inspection requirements

The tables of Appendix IIA/Appendix IIB as applicable summarize the general rules concerning inspection requirements; nevertheless the relevant blank detail specification shall take precedence except that a detail specification can still add to the number tests per Sub-Groups especially in Group A, or add a certain Sub-Group (for instance B2c or C2c), in which cases the relevant rules of Appendix IIA/Appendix IIB shall be used.

The inspection levels (IL) and AQL values, or alternatively the sample sizes (n) and acceptance criteria (c), given in the tables apply to the whole of each Sub-Group or section of each Sub-Group and not to any single test in the Sub-Group.

When “n a” is indicated, this means that the relevant Sub-Group is not applied.

3.5.3 Supplementary procedures for reduced inspection

3.5.3.1 *Reduced inspection for Group B tests*

Special reduced inspection procedures for the tests in all Sub-Groups of Group B inspection may be used provided that the conditions detailed hereafter are met.

Such procedures apply to each Sub-Group individually, as and when it meets the required conditions.

1) When sample sizes are based on the AQL system

When the conditions given in IEC 410 for the change from normal to reduced inspection are met, a manufacturer may carry-out the appropriate Sub-Group B test at normal inspection under Group C conditions at intervals of 3 months instead of on a lot-by-lot basis.

Reversion to normal inspection in Group B shall be made as soon as a sample has failed in the corresponding Sub-Group C.

2) When sample sizes have fixed values

When the previous 10 consecutive lots have been accepted on normal inspection, a manufacturer may carry-out the appropriate Sub-Group B test at normal inspection conditions but on 1/4 of the lots; optionally, especially for B8 endurance test, the manufacturer may test every lot with a sample equal to, or just above, 1/4 of the normal sample size and a moving 4 lots acceptance criterion equal to that already specified in the table. (Example: either test 38 devices every 4 lots with 1 reject allowed, or alternatively test 10 devices every lot with a moving acceptance criterion of 1 on 4 consecutive lots).

Reversion to normal inspection shall occur as soon as the acceptance criterion on reduced inspection is exceeded.

3.5.3.2 *Reduced inspection for Group C tests*

The procedure given in CECC 00107 is applicable to all Sub-Groups of Group C, including electrical endurance, which have a periodicity of three months or less; it is not applicable to those Group C tests performed because special reduced inspection in Group B was applied.

3.5.4 Sampling requirements for small lots or for expensive devices

(Sampling plans: see IEC 410)

Where the lot size indicates that, for the specified AQL and inspection level, a sampling plan with an acceptance number of zero shall be used, the Chief Inspector, at his discretion and with the approval of the ONS, may use any one of the following alternative procedures:

- 1) 100 % inspection
- 2) The plan having a larger sample with acceptance number of 1 for the specified AQL
- 3) The plan indicated for the given lot size and inspection level but the next higher AQL, if this leads to a plan with an acceptance number of 1
- 4) The plan with acceptance number of 0. However, if a single defective is obtained, either of the following procedures may be applied:

(4.1) A second sample shall be inspected, of such a size as to bring the combined first and second samples to that given by 2) above (that is the sample for a plan to accept on 1 for the same AQL). The lot is acceptable if no further defectives are obtained in the second sample.

(4.2) If the preceding 4 consecutive lots were acceptable under original inspection, such a lot may be held until the next lot has been inspected. If the sample from this next lot is acceptable, both lots shall be accepted. If the sample from this lot is not acceptable, both lots shall be rejected.

If both lots are accepted under this clause and in a subsequent lot a single defective occurs (when accepting on zero defects) before a clear run of four lots has been accepted then this lot shall be rejected immediately (without holding for the next lot).

Example:

The system in (4.1) above is best illustrated by an example:

A batch of four hundred devices is to be sample tested at AQL = 1,0 % and inspection level S4. Looking at the sampling chart, the 281 to 500 column is used for a batch of 400.

S4 and the batch size of 400 gives a sample size of 13. This sample of 13 and an AQL of 1 % indicate an acceptance criterion of no failures, and thus if there are no failures, all 400 are acceptable. If one device fails, the AQL = 1,0 % column is read down to the Figure 1 below the arrow.

The sample size for one failure is 50. Therefore, an additional $(50 - 13) = 37$ devices are tested.

If there are no further failures, all 400 are accepted. In spite of the first failure, only 50 devices have been tested from a batch of 400.

3.5.5 Certified test records

When the detail specification prescribes Certified Test Records and they are requested by a bona fide user of components, the procedure of CECC 00109 shall apply; these certified test records shall then contain the information asked for in the relevant blank detail specification.

3.5.6 Delivery of devices subjected to destructive or non-destructive tests

Tests are indicated, either in this document and/or in blank detail and detail specifications as “non-destructive” (ND) or “destructive” (D). Devices having undergone a test (ND) may be, or (D) shall not be, included in the lot for delivery. “Destructive” does not mean that the device is destroyed but that there may be either a potential risk of it being damaged, or that its appearance may have changed (for instance a solderability test, although indicated as (ND) in blank detail specifications, may become destructive and be indicated as such in the detail specification of a device with gold-plated leads: after testing, the leads will have a different appearance and the tested devices, although not damaged, can no longer be delivered).

On this ground, the indication may depend on the exact type of device and shall not be considered rigid; any deviations should be considered and agreed between the Chief Inspector and the ONS.

Devices subjected to non-destructive tests may be delivered provided they are re-tested to Group A requirements and satisfy them.

3.5.7 Delayed deliveries

Before delivery of lots which have been in store for more than two years, the lots, or the quantities to be delivered, shall satisfy the requirements of Sub-Group A2; in addition, they shall also satisfy the requirements of the solderability test of Sub-Group B4, except that sample size and acceptance criterion shall be 22/0 or 38/1.

If this has been done for the complete lot, no further retesting before delivery is needed for another period of two years.

3.5.8 Supplementary procedure for deliveries

When this has been nationally recognized, manufacturers may, at their discretion, supply devices that have met a higher assessment level against orders for a lower assessment level.

3.5.9 Unchecked parameters (additional information)

When additional information is given, in detail specifications, this shall not be the subject of inspection.

3.5.10 Screening

When screening is specified either in a detail specification or in the order for a given device, it shall be performed as indicated in Appendix VI unless otherwise stated.

Section 4. Test and measurement conditions

4.1 Standards conditions for testing

Unless otherwise specified, all measurements are carried out under the following conditions based on IEC 68-1.

Ambient temperature :	25 ± 5 °C
Relative humidity :	between 45 % and 75 % (but see sub-clause 5.3.2 of IEC 68-1)
Atmospheric pressure :	between 860 and 1 060 millibars

Measurements may be carried out at other temperatures provided the ONS is satisfied that the device will be in accordance with all the provisions of the detail specification when tested at an ambient temperature of 25 ± 1 °C, and relative humidity between 48 % and 52 %, when this is important.

4.2 Visual examination

4.2.1 Visual inspection

Unless otherwise specified, visual inspection shall be performed under normal factory lighting and under normal visual conditions. Inspection shall include the following items:

- Correctness of marking
- Correctness of terminal identification
- Correctness of appearance (for instance no broken encapsulation or terminals, no cracks in encapsulation, no open encapsulation).

4.2.2 Dimensions

Dimensions shall be checked in accordance with the specified drawing. The dimensions that shall be checked as part of Group B or C, are prescribed in Appendix III.

4.2.3 Permanence of marking

See § 4.4.12 Immersion in cleaning solvents

4.3 Electrical measurements

4.3.1 Alternative methods

Measurements may be carried out by using the methods specified or any other method giving compatible* results, but in case of dispute, only the specified method shall be used.

* NOTE By “compatible” is meant that, when the results obtained with the alternative method satisfy appropriate limits, the device would have met the originally specified limits as if it had been measured with the originally specified method (see also CECC 00107).

4.3.2 Precision of measurement

The limits quoted in detail specifications are absolute. Measurement inaccuracies shall be taken into account when determining the actual measurement limits. Usual precautions should be taken to reduce measurement errors to a minimum and to avoid damage to the device, and the most important of these are given in IEC 147-2.

4.3.3 Measurements at high temperature

The measurement shall be carried out by one of the following methods. Unless otherwise stated in the blank detail or detail — specification, the temperature shall be selected from the following, where underlined values are preferred:

- For silicon devices : 175 ± 5 , 150 ± 5 , 125 ± 5 , 100 ± 3 °C
- For germanium devices: 70 ± 3 , 55 ± 3 °C

Method 1

The measurement shall be carried out as specified in 4.4.1, except that the duration of exposure is limited to a time sufficient to reach temperature equilibrium, and that recovery conditions do not apply.

Method 2

The device to be measured shall be mounted by its normal fixing to a copper or similar high conductivity metal block. The block, which should have a mass of at least ten times that of the device under test, shall be maintained at the specified temperature. Sufficient time for the device to reach temperature equilibrium shall elapse before the measurements commence.

4.3.4 Methods for electrical measurements

1) Electrically non-operative devices are defined as being:

EITHER

— of inverted polarity, for all types of diodes,

OR

— open-circuited, that is, unless otherwise specified in the detail specification:

for diodes (including rectifier diodes): $V_F > 10 V_{F \text{ max specified}}$

for thyristors: $V_{TM} > 10 V_{TM \text{ max specified}}$

for bipolar transistors: $h_{21E} < 5$ (except when specified value is ≤ 20)

	Types A and B	Type C
for field-effect transistors:	$ V_{GSoff} > 3 V_{GSoff \text{ max}} $	$ V_{GS(TO)} > 3 V_{GS(TO) \text{ max}} $
or	$ V_{GSoff} < 0,1 V_{GSoff \text{ min}} $	

OR

— short-circuited, that is, unless otherwise specified in the detail specification:

for diodes (including rectifier diodes): $I_R > 100 I_{R \text{ max specified}}$

for thyristors: $I_{RM(1)} > 100 I_{RM(1) \text{ max specified}}$

for bipolar transistors: leakage current (such as I_{CBO}) > 100 relevant max specified

	Types A and B	Type C
for field-effect transistors:	$ V_{GSoff} > 3 V_{GSoff \text{ max}} $	$ V_{GS(TO)} < 0,1 V_{GS(TO) \text{ min}} $
or	$ I_{GSS} > 10 I_{GSS \text{ max}} $	or $ I_{GSS} > 10 I_{GSS \text{ max}} $

2) Methods for electrical measurements are listed hereafter, with reference to the relevant IEC document; they shall be used when required by the detail specification and as prescribed in this latter document. (see also 4.3.1).

Ref.	Symbol	Title	IEC Method	
<u>General</u>				
G-001	R _{th}	Reference point temperature	IEC 147-2 A -sub-clause 2.1	
G-002		Thermal resistance (excluding transistors)	IEC 147-2 A -ch. I, sect. 3, sub-cl. 2.2	
G-003	R _{th}	Thermal resistance (transistors)	IEC 147-2 C -ch. II, cl. 12	
<u>Diodes, signal and switching — General measurements</u>				
D-001	V _F	Forward voltage	IEC 147-2 B -ch. I, sect. 1, cl. 2	
D-002	I _R	Reverse current	IEC 147-2 B -ch. I, sect. 1, cl. 1	
D-003	Q _s	Recovered charge	IEC 147-2 B -ch. I, sect. 1, sub-cl. 4.2.2	
D-004	t _{rr}	Reverse recovery time	IEC 147-2 B -ch. I, sect. 1, sub-cl. 4.2.3	
D-005	t _{fr}	Forward recovery time	IEC 147-2 B -ch. I, sect. 1, sub-cl. 4.1 The recovery voltage should be stated, in the detail specification, at either 110 % or 120 % of V _F , but preferably 110 %	
D-006	C _{tot}	Capacitance	IEC 147-2 B -ch. I, sect. 1, cl. 3	
D-007	η	Detector voltage efficiency	IEC 147-2 B -ch. I, sect. 1, cl. 5 Detail to be specified in detail specifications	
D-008		Detector power efficiency		
D-009		V _(BR)		Avalanche breakdown voltage
D-010		W _{RRM} /W _{RSM}		Reverse transient energy
D-011	P _{RRM} /P _{RSM}	Peak reverse power	Methods are described in Appendix V	
<u>Diodes, voltage regulator and reference</u>				
D-021	V _Z	Working voltage	IEC 147-2 B -ch. I, sect. 2, cl. 1	
D-022	r _Z	Differential resistance	IEC 147-2 B -ch. I, sect. 2, cl. 2	
D-023	αVZ	Temperature coefficient of working voltage	IEC 147-2 B -ch. I, sect. 2, cl. 3	
D-024	V _n	Noise	No IEC method — A test is described in Appendix V	
<u>Diodes, variable capacitance</u>				
D-031	e _{TK}	Tracking error	No IEC method — A test is described in Appendix V	
D-032	Q	Effective Q value	IEC 147-2 B -ch. I, sect. 5, cl. 5	
D-033	r _s	Series resistance	IEC 147-2 B -ch. I, sect. 5, cl. 6	

Ref.	Symbol	Title	IEC Method
<u>Rectifier diodes</u>			
D-041	V_{FM}	Peak forward voltage, pulse method	IEC 147-2 E -ch. I, sect. 3, sub-cl. 1.3.3
D-042	I_{RM}	Peak reverse current	IEC 147-2 E -ch. I, sect. 3, sub-cl. 1.2.3
D-043	I_{FSM}	Surge (non repetitive) forward current	IEC 147-2 E -ch. I, sect. 3, sub-cl. 5.1
D-044	V_{RSM}	Non repetitive peak reverse voltage	IEC 147-2 E -ch. I, sect. 3, sub-cl. 5.2
D-045	Q_r	Recovered charge	IEC 147-2 E -ch. I, sect. 3, sub-cl. 1.6
D-046	$V_{(BR)}$	Avalanche breakdown voltage	IEC 147-2 A -ch. I, sect. 3, sub-cl. 4.1
D-047	P_{RSM}	Peak non-repetitive surge reverse power	IEC 147-2 H -ch. I, sect. 3, sub-cl. 4.2
<u>Current regulator/reference diodes</u>			
D-051	I_S	Regulator current	IEC 747-3 -ch. IV, sect. 3, sub-cl. 1
D-052	α_{IS}	Temperature coefficient of regulator current	IEC 747-3 -ch. IV, sect. 3, sub-cl. 2
D-053	Δ_{IS}	Regulator current variation	IEC 747-3 -ch. IV, sect. 3, sub-cl. 3
D-054	V_L	Limiting voltage	IEC 747-3 -ch. IV, sect. 3, sub-cl. 4
D-055	g_s	Small signal regulator conductance	IEC 747-3 -ch. IV, sect. 3, sub-cl. 5
D-056	g_k	Knee conductance	IEC 747-3 -ch. IV, sect. 3, sub-cl. 6
<u>Transistors, bipolar — General measurements</u>			
T-001	I_{CBO}	Collector-base cut-off current	IEC 147-2 -ch. II, cl. 2
T-002	I_{EBO}	Emitter-base cut-off current	IEC 147-2 -ch. II, cl. 3
T-003	$V_{CE sat}$	Collector-emitter saturation voltage	IEC 147-2 -ch. II, cl. 4
T-004	$V_{BE sat}$	Base-emitter saturation voltage	IEC 147-2 -ch. II, cl. 5
T-005	V_{BE}	Base-emitter voltage	IEC 147-2 -ch. II, cl. 6 Figure 3b
T-006	h_{21E}	Static value of common-emitter forward current transfer ratio	IEC 147-2 -ch. II, sub-cl. 10.1
T-007	C_{22b}	Output capacitance, input open-circuited	IEC 147-2 -ch. II, cl. 8 Figure 5c supplemented by: IEC 147-2 -ch. II, sub-cl. 14.3 NOTE when an electrode is directly connected to the case, the basic circuit may be altered.
T-008	F	Noise factor	IEC 147-2 C -ch. II, cl. 15
T-009	$I_{CE.}$	Leakage/cut-off currents	No IEC method — A test is described in Appendix V
T-010	$I_{S/B}$	Second breakdown current rating	A method is described in Appendix V

Ref.	Symbol	Title	IEC Method
T-011	V_{CEOsus}	Collector-emitter sustaining voltage	A method is described in Appendix V
<u>Transistors, bipolar; low frequency measurements</u>			
T-021	h_{21e}	Common-emitter small-signal forward current transfer ratio	IEC 147-2 -ch. II, sub-cl. 9.2.1
<u>Transistors, bipolar; matched pairs</u>			
T-031	$\frac{h_{21E(1)1}}{h_{21E(1)2}}$	Ratio of static values of common-emitter forward current transfer ratios	Methods are described in Appendix V
T-032	$ V_{\text{BE1}} - V_{\text{BE2}} $	Difference between base-emitter voltages	
T-033	$ \Delta(V_{\text{BE1}} - V_{\text{BE2}}) $	Change of difference of base-emitter voltages between two temperatures	
<u>Transistors, bipolar; high frequency measurements</u>			
T-041	f_T	Transition frequency	IEC 147-2 -ch. II, sub-cl. 14.2
T-042	C_{12e}	Common-emitter reverse transfer capacitance	No IEC method. A test is described in Appendix V
T-043	$\left \frac{h_{12b}}{\omega} \right $	Reverse transfer time factor	IEC 147-2 C -ch. II, sub-cl. 14.5
T-044	—	Scattering parameters	IEC 147-2 M -ch. II, sub-cl. 14.7
<u>Transistors, bipolar; switching time measurements</u>			
T-061	t_s	Storage time	No IEC method According to diagram to be specified in the detail specification
T-062	t_r	Rise-time	
T-063	t_{on}	Turn-on time	
T-064	t_{off}	Turn-off time	
<u>Field-effect transistors</u>			
T-071	$\begin{bmatrix} I_{\text{GDO}} \\ I_{\text{GSS}} \\ I_{\text{GS}} \end{bmatrix}$	Gate leakage or cut-off currents	IEC 147-2G -ch. IV, cl. 2
T-072	$I_D - I_{\text{DSS}}$	Drain current	IEC 147-2G -ch. IV cl. 3
T-073	I_{DSX}	Drain cut-off current	IEC 147-2G -ch. IV cl. 4
T-074	V_{GSoff}	Gate-source cut-off voltage	IEC 147-2G -ch. IV cl. 5
T-075	$V_{\text{GS(TO)}}$	Gate-source threshold voltage	IEC 147-2G -ch. IV cl. 6
T-076	C_{11ss}	Short-circuit input capacitance	IEC 147-2G -ch. IV cl. 7

Ref.	Symbol	Title	IEC Method
T-077	g_{22ss}	Short-circuit output conductance	IEC 147-2G -ch. IV cl. 8
T-078	g_{21s}	Short-circuit forward transconductance	IEC 147-2G -ch. IV, cl. 10
T-079	V_n, F	Noise voltage, noise factor	IEC 147-2G -ch. IV, cl. 12
T-080	—	Y-parameters	IEC 147-2G -ch. IV, cl. 13 and IEC 147-2C -ch. IV, cl. 14
(NOTE for high frequencies, s parameters (T-044) can be used alternatively)			
T-081	—	Switching times	IEC 147-2G -ch. IV, cl. 14
T-082	$r_{DS(ON)}$	Drain-source on-state resistance	IEC 147-2G -ch. IV, cl. 15
T-083	r_{dss}	Drain-source resistance	IEC 147-2G -ch. IV, cl. 16
T-084	G_P	Power gain	No IEC method
T-085	V_{DSsat}	Drain-source saturation voltage	
T-086	C_{22ss}	Short-circuit output capacitance	IEC 147-2G -ch. IV, cl. 9
T-087	C_{12ss}	Short-circuit feedback capacitance	IEC 147-2G -ch. IV, cl. 11
T-088	$V_{DS(ON)}$	Drain-source on-stage voltage	IEC 147-2G -ch. IV, cl. 15
Thyristors			
T-101	V_{TM}	Peak on-state voltage (pulse)	IEC 147-2E -ch. III, sect. 1, sub-cl. 1.2.3
T-102	I_{RRM}	Repetitive peak reverse current	IEC 147-2E -ch. III, sect. 1, sub-cl. 1.4.1
T-103	I_{DM}	Peak off-state current	IEC 147-2E -ch. III, sect. 1, sub-cl. 1.3.3
T-104	I_{TSM}	Surge (non repetitive) on-state current	IEC 147-2E -ch. III, sect. 1, sub-cl. 3.3
T-105	V_{RSM}	Non repetitive peak reverse voltage	IEC 147-2E -ch. III, sect. 1, sub-cl. 3.1
T-106	V_{DSM}	Non repetitive peak off-state voltage	IEC 147-2E -ch. III, sect. 1, sub-cl. 3.2
T-107	I_H	Holding current	IEC 147-2E -ch. III, sect. 1, sub-cl. 1.7
T-108	I_L	Latching current	IEC 147-2E -ch. III, sect. 1, sub-cl. 1.11
T-109	$\begin{bmatrix} I_{GT} \\ V_{GT} \end{bmatrix}$	Gate trigger current and voltage	IEC 147-2E -ch. III, sect. 1, sub-cl. 1.5
T-110	V_{GD}	Gate non-trigger voltage	IEC 147-2A -ch. III, sect. 1, sub-cl. 1.6
T-111	di/dt	Critical rate of rise or on-state current	IEC 147-2E -ch. III, sect. 1, sub-cl. 3.4
T-112	dv/dt	Critical rate of rise of off-state voltage	IEC 147-2D -ch. III, sect. 1, sub-cl. 1.10

4.4 Climatic and mechanical tests

The following tests shall be used when required by the detail specification, and as prescribed in this latter document. They are indicated as “destructive” or “non destructive” according to 3.5.6.

When testing is carried out by the device manufacturer, over-stress testing is permitted; in all other cases, the limits given in the test conditions for each of the following tests shall be used.

When a sequence of testing is required, it shall be specified in the detail specification.

(For dates of applicable IEC 68 documents, see under 2.2 “Related documents”).