
British Standard

Harmonized system of quality assessment for electronic components: Sectional specification : Film and hybrid integrated circuits (capability approval)

Système harmonisé d'assurance de la qualité des composants électroniques
Spécification intermédiaire: Circuits intégrés hybrides et à couches (agrement de savoir-faire)

Harmonisiertes Gütebestätigungssystem für Bauelemente der Elektronik
Rahmenspezifikation: Integrierte hybrid und Schichtschaltungen (anerkennung der befähigung)

National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with CENELEC Electronic Components Committee (CECC) 63200 : 1984 'Harmonized system of quality assessment for electronic components : Sectional specification : Film and hybrid integrated circuits (capability approval)'.

This standard is a harmonized specification within the CECC system.

Terminology and conventions. The text of the CECC specification has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards; attention is drawn especially to the following.

The comma has been used as a decimal marker. In British Standards it is current practice to use a full point on the baseline as the decimal marker.

Cross-references

International standard	Corresponding British Standard
IEC 63 : 1963	BS 2488 : 1966 Schedule of preferred numbers for the resistance of resistors and the capacitance of capacitors for telecommunications equipment (Technically equivalent)
IEC 68	BS 2011 Basic environmental testing procedures (The relevant Parts are all identical)
CECC 63000 : 1984	BS CECC 63000 : 1985 Harmonized system of quality assessment for electronic components. Generic specification : Film and hybrid integrated circuits (Identical)

The Technical Committee has reviewed the provisions of IEC 147, to which reference is made in the text, and has decided that they are acceptable for use in conjunction with this standard.

Compliance with a British Standard does not of itself confer immunity from legal obligations.



Amendment No. 1
published and effective from 30 September 1987
to BS CECC 63200 : 1985

Harmonized system of quality assessment
for electronic components

Sectional specification: Film and
hybrid integrated circuits
(Capability approval)

NOTE. This Amendment is identical with the 1st Amendment and 1st Supplement published to CECC 63200, Issue 1 (1985), which were issued separately by CECC. Because of the difference in pagination between BS CECC 63200 and the CECC specification, the instructions for replacement of pages differ from those given in the CECC Amendment.

Instructions for the insertion of new and revised pages

AMD 5491
September 1987

Replace pages 1/2 (page 2 unchanged on back).
Replace pages 3/4 (page 4 unchanged on back).
Replace pages 29/30 (page 29 unchanged on front).
Replace pages 41/42 (page 42 unchanged on back).
Replace pages 43/44 (page 44 unchanged on back).
Replace pages 45/46 (page 46 unchanged on back).
Replace pages 49/50.
Remove page 51 (back of page 51 blank) and replace by pages 51/52.
Insert pages 53/54 to 81/82.

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for FILM and HYBRID INTEGRATED CIRCUITS (F&HICs). It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification, the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and the United Kingdom, and copies of it can be obtained from the addresses shown on the blue flysheet.

PREFACE

This sectional specification was prepared by CECC Working Group 21 : "HYBRID MICRO-CIRCUITS".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC Publication 147 : Essential ratings and characteristics of semiconductor devices and general principles of measuring methods.

The text of this sectional specification was circulated to the CECC for voting in the documents listed below and was ratified by the President of the CECC for printing as a CECC Specification.

<u>Documents</u>	<u>Voting date</u>	<u>Report on the voting</u>
CECC(Secretariat)1179	August 1982	CECC(Secretariat)1276
CECC(Secretariat)1287	May 1983	CECC(Secretariat)1394
CECC(Secretariat)1365	July 1983	CECC(Secretariat)1412
CECC(Secretariat)1451	January 1984	CECC(Secretariat)1538

At present this specification covers F&HICs using thick film techniques only but amendments are under preparation to cover F&HICs manufactured using thin film techniques as well.

Associated with this specification is one blank detail specification referenced by a CECC number. When completed as specified in Section 2 of this specification, the blank detail specification forms a detail specification. Such detail specifications may be used for the acceptance of a complete product and the granting of initial capability approval for the limits of capability identified by the manufacturer in his capability manual and maintenance of capability approval in accordance with the CECC System.

SECTION 1 - SCOPE

This sectional specification applies to F&HICs manufactured as catalogue products or as custom built products using thick film or thin film techniques and whose quality is assessed on the basis of capability approval.

It presents preferred values for ratings and characteristics. It selects from CECC 63 000 the appropriate methods of test and gives general performance requirements, to be used in detail specifications for F&HICs derived from this specification.

The concept of preferred values is directly applicable to catalogue products but does not necessarily apply to custom built products.

Passive networks can be qualified to this specification or to alternative specifications, when introduced.

SECTION 2 - GENERAL, PREFERRED CHARACTERISTICS, RATINGS AND SEVERITIES FOR ENVIRONMENTAL TESTS

2.1 RELATED DOCUMENTS

IEC 63	(1963)	Preferred number series for resistors and capacitors. Amendment Nr 1 (1967) Amendment Nr 2 (1977)
IEC 68	-	Basic environmental testing procedures.
CECC 63 000	(1984)	Generic specification for F&HICs.

Note : The above references apply to the current editions except for IEC 68, for which the referenced edition and the applicable test clauses of CECC 63 000 shall be used.

2.2 PREFERRED RATINGS AND CHARACTERISTICS

The values given in detail specifications shall preferably be selected from the following :

2.2.1 Preferred climatic categories

The F&HICs covered by this document are classified into climatic categories according to the general rules given in IEC Publication 68-1.

The lower and upper category temperature and the duration of the damp heat, steady state test shall be chosen from the following :

Minimum ambient temperature : - 55 °C, - 40 °C, - 25 °C, - 10 °C and + 5 °C

Maximum ambient temperature : + 40 °C, + 55 °C, + 70 °C, + 85 °C, + 100 °C, + 125 °C and + 155 °C

Duration of the damp heat, steady state test : 04, 10, 21 and 56 days.

The severities for the cold and dry heat tests are the lower and upper category temperatures respectively. Because of the construction of some F&HICs these temperatures will occur between two of the preferred temperatures given in IEC Publication 68-2. In this event the nearest preferred temperature within the actual range of the F&HIC shall be chosen for this severity.

TABLE 6 - FILM MATERIALS

Characteristics	Similarity rules
1 - Conductive materials (type, composition)	Same
2 - Multilayers (type, dielectric, composition)	Any combination within the maximum number of layers on the CQC.
3 - Resistive materials : . composition . resistivity per square	Same purchased material series. Any combination within the range of extreme values covered by CQCs.
Maximum power per unit area of resistor elements	Any combination limited to the maximum power rating covered by CQCs.
Trimming process	Same trimming process.
Resistance values and tolerance	For a given tolerance, combination allowed within the range of minimum and maximum resistance values covered by the CQCs.
Temperature coefficient	Combination allowed within guaranteed absolute values of the CQC.
Differential temperature coefficient and differential ohmic value tolerance	Combination allowed in the range of extreme ohmic values of the CQCs.
Number of resistive elements	No limitation
Interconnection mode	Same
4 - Protective coatings	Same

TABLE 7 - ADDED NON-ENCAPSULATED ACTIVE CHIP COMPONENTS (Note 1)

Characteristics	Similarity rules
<u>Component type</u> (Notes 2 and 3)	
(1) Transistor and diode (2) Integrated circuit	Combination allowed within (1) or (2) but not between these two generic families
<u>Presentation of components</u>	
(1) Diffusion face up (2) Diffusion face down	Combination allowed within but not between these two presentations
<u>Methods of mounting</u>	
Adhesive, eutectic, soldering, other	Combination allowed within but not between these mounting methods
<u>Wiring</u>	
(1) Materials (gold wire, aluminium wire, other)	No combination allowed between different basic metal wires
(2) Methods (thermocompression, thermosonic, other)	No combination allowed between different bonding methods
(3) Wire diameter	Combination allowed within ± 50 % of wires used in CQCs
(4) Tape cross-sectional area	Combination allowed within ± 50 % of sectional area used in CQCs
<u>Dimensions</u>	
(1) Diode and transistor chip area	Combination allowed between 50 % of the smallest and 200 % of the largest chip area on the CQC
(2) Integrated circuit chip area	Combination allowed between 50 % of the smallest and 200 % of the largest chip area on the CQC
(3) Number of outputs	Any combination allowed
<u>Protective coatings</u>	Same coating material, chip technology and passivation combination

NOTES

1. When non-qualified added components are given qualified status by the procedures in clause 3.6.2.2 (1) of CECC 63 000, structural similarity for hybrid circuits require the same manufacturing source for each added component.
2. If the CQC has no integrated circuit, the number of transistors or diodes shall be a minimum of three.
3. If the hybrid CQC contains one or more monolithic circuit chips, the ratio : total number of wires bonded to chip(s) to total number of CQC package leads electrically connected to the chips, shall be equal to or greater than 0,5.

APPENDIX B

MINIMUM CONTENTS OF A MANUFACTURER'S CAPABILITY MANUAL FOR THICK FILM CIRCUITS

B.1 SCOPE

This appendix establishes the requirements for the capability manual for thick film hybrid integrated circuits. It does not apply to thin film or semiconductor integrated circuits.

The term hybrid is defined in 2.3.10 of CECC 63 000 and the scope of this appendix includes the use of any of the added components in association with the basic thick film technology.

Note : In addition to the requirements stated herein the manufacturer may include additional information, for example on process control and inspection schedules, which he considers necessary for the full control of his capability.

For ease of reference the capability manual shall give information under the headings given below as appropriate. Under item 1 of the capability manual, the manufacturer shall declare the entire scope of his capability and state which assessment level applies. Where the procedure under 3.2 of CECC 63 000 is invoked the capability manual shall make reference to the surveillance of those stages which are not carried out under the direct surveillance of an approved Chief Inspector.

B.2 CUSTOMER PARTICIPATION IN THE LAYOUT

The manufacturer shall declare whether he permits customer participation in the technological design and layout of circuits. In the case of a device manufactured to this standard where the customer has provided the design and layout it shall be the responsibility of the manufacturer to ensure that his approved design data and layout rules have been followed.

B.3 CAPABILITY ABSTRACT

The statement of basic technology in addition to the details required in 1.2 of CECC 63 000 for thick film integrated circuits shall include the following which shall be used in the QPL:

- Type of substrate, for example alumina, beryllium oxide
- Types of inks, numbers of layers and methods of pattern formation, for example screen printing, ink writing
- Range of film elements, for example conductors, resistors, capacitors, and so on
- Methods of trimming of film elements, for example laser, spark erosion, air abrasion
- Methods of lead attachment to the substrate, for example soldering
- Basic encapsulation method, for example hermetic, plastic

- Types of added components, for example chip capacitors, discrete semiconductor devices, semiconductor dice, and related methods of attachment
- Methods of interconnecting within the film circuits according to type, for example bonding, soldering
- (Not for integral substrate packages). Methods of attaching substrate to package (for example eutectic bond, organic bond, and so on)
- Boundaries of capability - Range of values/tolerance, matching where appropriate, conductors, resistors, capacitors, and so on.

Note : It may not be possible to achieve all the limits of the capability in combination.

B.4 MATERIALS AND ADDED COMPONENTS

This section of the capability manual shall :

- Identify and provide evidence of the existence of purchasing specifications for the materials which are critical for the quality of the products
- Describe the methods used to verify the suitability of materials for production and identify the documentation necessary to ensure consistent quality of the specified materials
- Indicate the inspection methods for added components to be incorporated. See 3.6.2 of CECC 63 000.

B.4.1 Materials purchasing specifications

The manual shall identify the relevant purchasing specifications under the appropriate headings as listed below. The "specification contents" column lists the data which shall be included in the purchasing specifications but such data is not required in the capability manual. The list of items included in each sub-clause is intended for guidance and is not exhaustive. Items are applicable where relevant to the particular process technology.

(1) Materials in circuit and package

	<u>Specification contents</u>
- Substrates	Types of material, composition and characteristics, thermal and mechanical characteristics.
- Printing inks, pastes and glazes	Types, composition and characteristics.
- Assembly materials	Types of materials, for example lead frames, adhesives, solders, leads and terminations, varnishes.

Specification contents

- | | |
|---------------------------------------|--|
| - Added components | Types, specification numbers or other reference data of the added components approved for use. Information on preferred types of components. In addition the capability manual shall provide details of an appropriate purchasing system and inspection and testing requirements for added components. |
| - Package and encapsulation materials | Types of materials, e.g. cases, caps, lids, finishes, platings, mouldings, thermo-setting resins, varnishes, coatings, identification and marking. Material combinations, e.g. Kovar-glass, glass-ceramic. Type of plastic used for plastic or part-plastic encapsulations. List of standard packages used, or reference to control of drawings for non-standard packages. |

(2) Materials used in processing

- | | |
|------------------------|---|
| - Artwork | Types and characteristics of materials used in circuit design and artwork, for example dimensional stability; durability. |
| - Printing screens | Types, mesh characteristics. |
| - Processing materials | Types of materials, chemicals used in circuit preparation, adjustment, trimming. |
| - Assembly materials | Types and characteristics of materials used as aids to assembly, for example cleaning agents. |

B.4.2 Material verification

The manual shall describe the methods for the verification of the suitability of the above materials for production and other documentation necessary to ensure consistent quality of those materials which are critical to the quality of products.

B.5 DESIGN DATA AND LAYOUT RULES

Reference shall be made to the detailed rules used in the design and layout of circuits. The manual shall contain the following data as appropriate.

CharacteristicsDesign limit(s) to be stated(1) Conductor tracks

Track width	Min.	
Track thickness (fired)	Min.	Max.
Spacing between parallel tracks	Min.	
Spacing between track, bonding pad, terminal pad or any combination thereof	Min.	
Spacing between any metallization and edge of substrate	Min.	
Terminal pad dimensions	Min.	
Probe pad dimensions	Min.	
Conductor track resistivity		Max.
Current density for each conductor material		Max.
Track dissipation		Max.
Any requirements for solder build up of tracks		
Solderability characteristics		
Bondability characteristics		
Voltage stress which can be applied between parallel tracks at minimum design spacing		
Insulation resistance under same conditions	Min.	
Dimensions of lead-through holes		
Spacing of lead-through holes from edge of substrate	Min.	
Track adhesion after processing/ageing	Min.	
Mounting pad geometry, dimensions, positional tolerances for each type of added component, spacing from other tracks		
Wire-bonding or other interconnecting pad dimensions	Min.	
Spacing between tracks under chip capacitors	Min.	
Rules relating to underpassing conductors		

(2) Dielectric and cross-over insulation, capacitance

Overlap of dielectric over conductor track	Min.	
Thickness of dielectric	Min.	
Capacitance of cross-over (per unit area)		Max.
Spacing of dielectric to edge of substrate	Min.	
Insulation resistance of dielectric (per unit area)	Min.	
Range of capacitance values	Min.	Max.
Voltage breakdown	Min.	

Characteristics

Design limit(s) to be stated

(3) Resistors

Range of resistor values	Min.	Max.
Temperature coefficient of resistance		Max.
Dissipation per unit area of stated surface at ambient temperature		Max.
Stability % per 1000 h at max. dissipation		Max.
Stability % per 1000 h at max. voltage stress		Max.
Noise data - where low noise performance is claimed		Max.
Non linearity (IEC 440)		Max.
- For rectangular resistors		
Linear dimensions	Min.	Max.
Aspect ratio (L/W)	Min.	Max.
- For other resistor profiles		
Design equations with limits as necessary		
- For all resistors		
Overlap of resistor on conductor track	Min.	
Undisturbed conductor track width (for single resistor)	Min.	
Distance of probe pad from end of resistor		Max.
Spacing from resistor to conductor track	Min.	
Spacing between resistor material	Min.	
Glaze or protection overlap	Min.	
- For each type of trimming		
Rules for trimming including limiting conditions		
Absolute tolerance relating to size and ohmic value after trimming as appropriate	Min.	
Matching tolerance after trimming	Min.	
Tracking tolerance after trimming (temperature and ageing)	Min.	
- Where appropriate, additional data shall be given on :		
The effect of resistivity of terminal materials particularly for short profile resistors		
High voltage stability		
Noise and the design requirements for low-noise resistors		

Where the realization of the circuit pattern is by means other than screen printing many of the above requirements shall apply and shall be given as appropriate.

Characteristics

Design limit(s) to be stated

(4) Glaze and protection

Where appropriate, the requirements for glaze and other protection for circuit elements shall be stated.

(5) Solder and braze

Where appropriate, the requirements for solder and braze compositions used either by over-printing or by syringe application shall be declared.

(6) Pattern registration

Data on the dimensional tolerances for pattern registration.

(7) Added components

Positional tolerances relating component tab, wire or other termination to the area of mounting pad	Min.
Distance between adjacent added components	Min.
Distance between added components and adjacent film areas	Min.
Distance between edge of component and edge of substrate	Min.
Clearance between assembled circuit, including added components and inside of package	Min.

(8) Attachment

(Not for integral substrate packages)

The basic methods used for attachment of substrates to packages shall be stated (for example eutectic bond, organic bond, and so on).

Maximum values for the dimensions and mass of the substrate assembly carried by the attachment shall be related to limiting conditions for thermal shock, mechanical shock, vibration, acceleration, thermal resistance and (for non cavity packages only) humidity.

(9) Thermal characteristics

Thermal resistance or power dissipation of substrate/package combinations	Max.
Temperature and temperature gradients	Max.
Rules or data relating density and spacing of power dissipating elements such as resistors and rectifiers	
Rules or data relating density and spacing of power dissipating circuit elements such as semiconductor devices with respect to the thermal characteristics of substrate and package combinations	

(8) Final sealing

The requirements for pre-encapsulation inspection
The issue, preparation and inspection of encapsulation materials, preforms, bases, caps, lids, epoxies, prior to use
The sealing process
The post-encapsulation inspection
Marking and lead identification

(9) Final test

The requirements for the acceptance testing of completed circuits
Final inspection and packing for despatch

(10) Rework

Additionally the charts shall show each process step where rework may take place and identify the controlling specifications. These specifications shall conform to the applicable requirements and shall state the maximum number of rework cycles in each case.

B.7 CAPABILITY QUALIFYING CIRCUITS

To satisfy the requirements the manual shall describe in detail the CQCs to be used for assessment and shall indicate for each circuit the aspect or aspects of the declared capability which are being assessed.

Every CQC shall have a detail specification which shall include a dimensioned layout drawing. Specifications for packaged CQCs shall be in the style and content of the relevant blank detail specification.

NOTE : A group of CQCs may be included in a single composite specification.

The range of CQCs selected shall, as a minimum, assess the following characteristics of the capability, as appropriate.

B.7.1 Circuit design and processing

(1) Conductor characteristics (film)

- Conductor resistivity for all conductor materials
- Insulation resistance between tracks at minimum design spacing for each material type
- Breakdown voltage between tracks at minimum design spacing for each material type
- Maximum current density for each film
- Capacitance of crossovers
- Breakdown voltage of crossovers

- Maximum number of conductor layers for each material type
- Insulation resistance between conductors at minimum design spacing for each material type for each conductor layer
- Insulation resistance between adjacent conductor layers
- Insulation resistance between underpassing conductor and add-on component termination at minimum design spacing
- Minimum size vias
- Insulation resistance between trimmed resistor termination and underpassing conductor.

(2) Resistor characteristics (film)

- Minimum, maximum and intermediate resistance values for each resistor ink series terminated by each conductor material type
- Trimmed resistor tolerance for each ink series for laser and/or abrasive methods
- Resistor matching for each ink series
- Temperature coefficient of resistance (absolute and tracking) for each ink series
- Minimum and maximum aspect ratios for each resistor ink series
- Smallest physical size for each resistor ink series
- All preceding resistance characteristics in respect of each resistance ink series screened on printed dielectric layers.

(3) Capacitor characteristics (film)

- Minimum, maximum and intermediate capacitance values for each ink series
- Capacitance tolerance
- Dissipation factor
- Temperature coefficient of capacitance
- Capacitance tracking with temperature.

(4) Added components

- All attachment methods
- Maximum mass to contact area ratio for each added component type
- All interconnection methods
- Maximum differential expansion strain between substrate and leadless components for each attachment method.

B.7.2 Packaging

(1) Solid encapsulated and unencapsulated circuits

Packages having the maximum number of lead-out positions for each package type.

(2) Cavity packages

Packages having the maximum number of lead-out positions and/or greatest seal length with the same sealing method for each package type.

B.7.3 Endurance characteristics

Thick-film integrated circuits designed to the maximum declared design rule combinations of power dissipation and operating temperature shall be assessed for each package type.

APPENDIX C

STRUCTURAL SIMILARITY RULES FOR CAPABILITY APPROVAL FOR THIN FILM CIRCUITS

C.1 SCOPE

This appendix defines the rules for deciding if a new circuit is covered by the manufacturer's declared capability and the testing performed on CQCs. It may also be used as a guide to the manufacturer in selecting CQCs to cover a capability. Where the rules do not cover specific circumstances, the manufacturer's chief inspector and the ONS shall agree the additional criteria and shall submit a subsequent proposal for amendment of this document through their national committee.

C.2 PROCEDURES

When structural similarity is to be decided upon, the following procedures shall be considered.

C.2.1 Defining CQC(s) within the structural similarity rules

- (1) Table 13 is structured to align with the test sequences given in Table 1 of this specification and Table 3 of the BDS. Circuits selected for the periodic inspection schedules shall also be representative of the circuits currently in production.
Having first classified the circuit according to 1.2 of CECC 63 000, the manufacturer should use Table 4 in this specification to classify the materials, processes and basic technology which represent his capability.
- (2) The manufacturer should then review his current and/or intended range of products against the similarity combination rules given in Tables 5-10 and 13. This enables a decision to be made on the number of different CQC types needed for capability approval from the technological standpoint.
- (3) The selection process then extends to Tables 11 and 12 which define the limits of combination for mass and dimensions.
Additional CQCs to those nominated in (2) above may be required to cover these aspects.
- (4) After choosing suitable environmental test severities from Section 4 of CECC 63 000, a chart can be constructed which shows the tests and severities applicable to each CQC.
- (5) Structural similarity of a circuit with a CQC (or CQCs) requires that the layout design rules used and electrical and environmental ratings and characteristics shall not be more severe than those for the CQCs.

The choice of CQCs lies between

- Special circuits designed to cover as many capability boundaries as is practicable with each type; this will result in the minimum number of CQC types

or

- A wider range of normal custom/catalogue circuits as CQCs to cover the capability.

C.2.2 New Circuits :

Each new circuit to be manufactured for sale and release within the system shall first be checked to ensure that it can be constructed using validated design rules, contains validated materials and can be made using approved processes and package styles.

Next, its features should be considered in relation to existing CQCs - ie. for the cover they give in terms of materials and technology (Tables 5-10), mass and dimensions (Tables 11 & 12), appropriate tests and severities (Tables 13 and Section 4 of CECC 63 000). Its features shall be covered by one or more CQC.

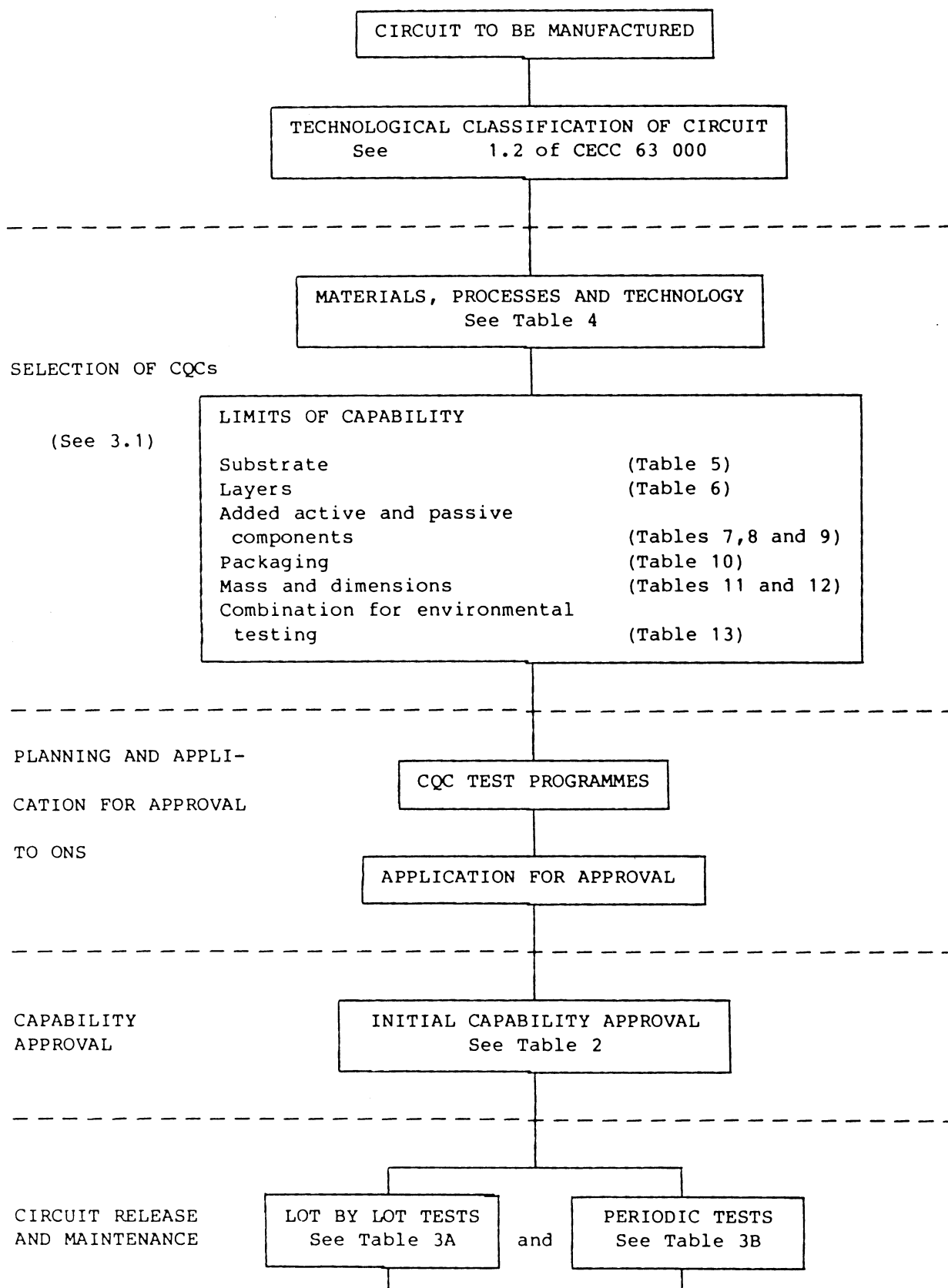
Where existing CQCs do not cover the new circuit, the manufacturer wishing to release it, shall first extend his capability in accordance with the specific need and the requirements of 3.6.3 (5) of CECC 63 000. In this case the extra tests may be performed either on a CQC or on the new circuit itself.

C.2.3 Guidance on procedures :

The following diagrams give guidance on the implementation of the principles described in C.2.1 and C.2.2 above.

- (1) Selection and testing of CQCs for capability approval.
- (2) Procedure for new circuits.

(1) Selection and testing of CQCs for capability approval



(2) Procedure for new circuits

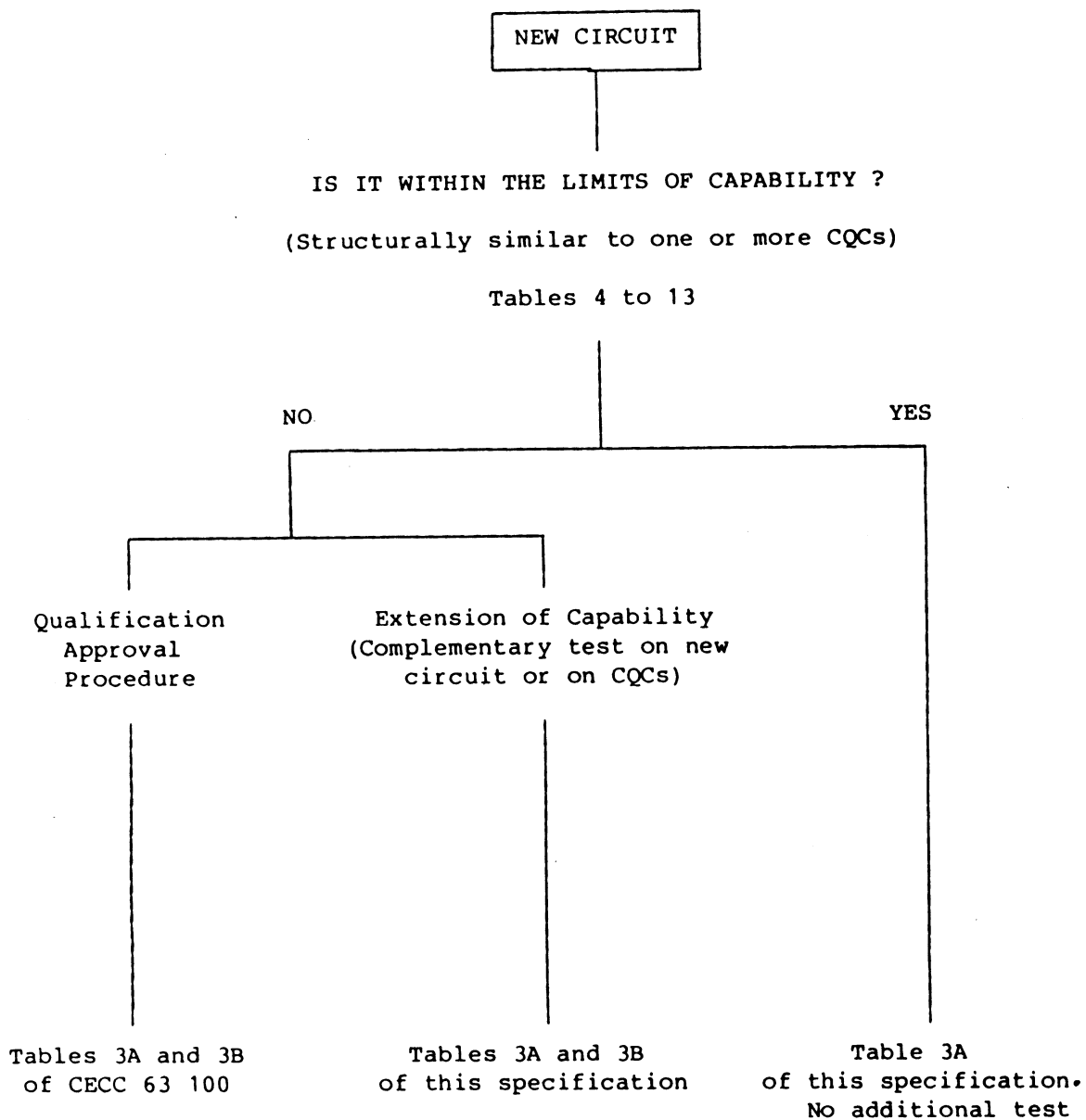


TABLE 4 - CLASSIFICATION OF TECHNOLOGY, MATERIALS AND PROCESSES

- Individual statements in each of the columns below give examples of material and process technologies to which Tables 5-10 may be applied.
- The list of items is not necessarily complete.
- Items listed in the various columns are not necessarily linked horizontally.

Item	Basic technology	Basic materials	Basic process/method
<u>Substrates</u> (Table 5)		Alumina Glass Coated metal Beryllium oxide Sapphire Silicon	Pressed/slip-cast Flame polished Lapped & polished
<u>Film Elements</u> (Table 6) a) Function as : Resistors Capacitors Inductors Thermistors Opto-electronic devices Conductors Crossovers Via holes Active devices		Copper Tantalum nitride/ oxide Nickel, chromium, nickelchromium Gold Tungsten Titanium Palladium Platinum Molybdenum, molybmanganese Magnesium Aluminium Silicon oxide/ nitride Organic materials	Evaporation Sputtering Plating Spinning (centrifugal) Dip lacquering Anodization
b) Pattern generation			Metal mask Photolithography Additive Subtractive Laser machine Ion beam Electron beam
c) Trimming methods			Spark machine Laser machine Ion beam Electron beam Anodisation
d) Multilayer	Organic dielectric Inorganic dielectric	Conductors and insulators	Sequential vacuum deposition Spinning (centrifugal) Dip lacquering Anodisation Sputtering

(Continued)

(Continuation)

Item	Basic technology	Basic materials	Basic process/method
Added components (Tables 7, 8, 9)	Encapsulated	Germanium Silicon Ga As P	Eutectic
Diodes	Hermetic		Adhesive
Transistors	Plastic		Solder preform
Integrated circuits	Chip carrier		Solder paste
	Tape leads		
	Wire leads		
Opto-electronic	Non-encapsulated	Thick film Nickel-chromium Tantalum Diffused silicon	Wire bond Al, Au
Resistors	Passivated		Thermo-compression
Capacitors	Non-passivated		Ultrasonic
Inductors	Face-up		Thermo-pulse
	Flip chip		Solder reflow
	Beam lead		Resistance weld
	Spider		Thermo-sonic
		Ceramic	Adhesive
		Tantalum	Wire, soldered
		Foil	
		Silicon	
<u>Packaging</u> (Table 10)	Basic style and form :	Basic encapsulation materials :	Method of closure/ encapsulation :
	Leadless	Metal	Glass/Metal seal
	Dual-in-line	Ceramic	Organic seal
	Single-in-line	Metal-ceramic	Resistance weld
	Flat-pack	Metal-glass	Laser weld
	Chip carrier	Organic	Solder seal
	Non-encapsulated	Silicones	Electron beam weld
	Hermetic		Cast mould
	Moulded plastic		Injection mould
	Conformal coating		Plastic box fill
			Dip coat
			Drop coat
			Spray coat
			Fluidized bed

TABLE 5 - SUBSTRATES

Characteristics	Similarity rules
Material	For combination, the proportion of main material representing at least 90 % of the substrate volume shall be equal to within 2 %
Thickness	Same nominal substrate thickness
Size	Combinations allowable for :
(L = length of CQC)	$0,2 L \leq \text{length} \leq 2 L$
(W = width of CQC)	$0,2 W \leq \text{width} \leq 2 W$
Mechanical parameters	Same purchase and inspection specifications
- camber	
- roughness	
- porosity	
- appearance	

TABLE 6 - FILM MATERIALS

Characteristics	Similarity rules
1 - Conductive materials (type, composition)	Same
2 - Basic process	Same
3 - Multilayers (type, dielectric, composition)	Any combination within the maximum number of layers on the CQC
4 - Resistive materials : - composition - resistivity per square	Same purchase material series. Any combination within the range of extreme values covered by CQCs
Maximum power per unit area of resistor elements	Any combination limited to the maximum power rating covered by CQCs
Trimming process	Same trimming process
Resistance values and tolerance	For a given tolerance, combination allowed within the range of minimum and maximum resistance values covered by the CQCs
Temperature coefficient	Combination allowed within guaranteed absolute values of the CQC
Differential temperature coefficient and differential ohmic value tolerance	Combination allowed in the range of extreme ohmic values of the CQCs
Number of resistive elements	No limitation
Interconnection mode	Same
5 - Protective coatings	Same

TABLE 7 - ADDED NON-ENCAPSULATED ACTIVE CHIP COMPONENTS (Note 1)

Characteristics	Similarity rules
<u>Component type</u> (Notes 2 and 3)	
(1) Transistor and diode (2) Integrated circuit	Combination allowed within (1) or (2) but not between these two generic families
<u>Presentation of components</u>	
(1) Diffusion face up (2) Diffusion face down	Combination allowed within but not between these two presentations
<u>Methods of mounting</u>	
Adhesive, eutectic, soldering, other	Combination allowed within but not between these mounting methods
<u>Wiring</u>	
(a) Materials (gold wire, aluminium wire, other)	No combination allowed between different basic metal wires
(b) Methods (thermocompression, thermosonic, other)	No combination allowed between different bonding methods
(c) Wire diameter	Combination allowed within ± 50 % of wires used in CQCs
(d) Tape cross-sectional area	Combination allowed within ± 50 % of sectional area used in CQCs
<u>Dimensions</u>	
(1) Diode and transistor chip area	Combination allowed between 50 % of the smallest and 200 % of the largest chip area on the CQC
(2) Integrated circuit chip area	Combination allowed between 50 % of the smallest and 200 % of the largest chip area on the CQC
(3) Number of outputs	Any combination allowed
<u>Protective coatings</u>	Same coating material, chip technology and passivation combination

NOTES

1. When non-qualified added components are given qualified status by the procedures in 3.6.2.2 (1) of CECC 63 000, structural similarity for film and hybrid circuits require the same manufacturing source for each added component.
2. If the CQC has no integrated circuit, the number of transistors or diodes shall be a minimum of three.
3. If the hybrid CQC contains one or more monolithic circuit chips, the ratio : total number of wires bonded to chip(s) to total number of CQC package leads electrically connected to the chips, shall be equal to or greater than 0,5.

TABLE 8 - ADDED ENCAPSULATED ACTIVE COMPONENTS OTHER THAN CHIPS (Note 1)

Characteristics	Similarity rules
<u>Component type</u> (Notes 2 and 3)	
(1) Transistor and diode (2) Integrated circuit	Combination allowed within (1) or (2) but not between these two generic families
<u>Presentation of component</u>	
(1) Encapsulated components with leads (2) Encapsulated components without leads	For a given encapsulation style, combination allowed within but not between the presentation categories (1) and (2) and also within 200 % of the number of leads on the encapsulated component on the CQC
<u>Mounting methods and interconnections</u>	
Soldering, adhesive, welding	Combination allowed within but not between these mounting methods
<u>Component encapsulation</u>	
	No combination allowed unless :
	1) The environmental classification of the component is the same or higher than the environmental classification of the CQC
	or
	2) The CQC is hermetically sealed

NOTES

1. When non-qualified added components are given qualified status by the procedures in 3.6.2.2 (1) of CECC 63 000, structural similarity for film and hybrid circuits require the same manufacturing source for each added component.
2. If the specimen has no integrated circuit, the number of transistors or diodes shall be a minimum of three.
3. If the hybrid CQC contains one or more monolithic circuit chips, the ratio : total number of wires bonded to chip(s) to total number of CQC package leads electrically connected to the chips, shall be equal to or greater than 0,5.

TABLE 9 - ADDED PASSIVE COMPONENTS (Note 1)

Characteristics	Similarity rules
<u>Component type</u>	
(1) Components with leads (2) Components without leads	No combination allowed between (1) and (2) but any combination allowed within each component family (1) or (2) covered by CQCs e.g. ceramic capacitors class I, resistor chips, etc...
<u>Mounting methods and interconnections</u>	
Soldering, adhesive, wire-bonding, welding	Combination allowed within but not between these methods
<u>Dimensions</u>	
. Assessment level K and L	Combination allowed within the limit of double or half the lateral dimensions of each component used in the CQCs
. Assessment level M	Any combination allowed

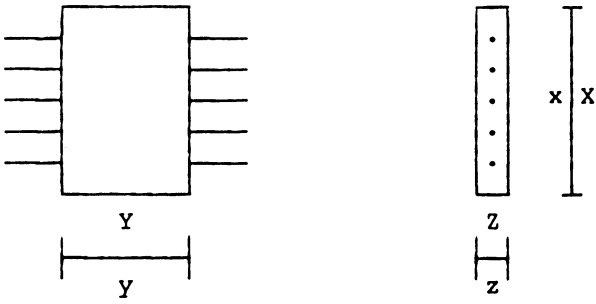
NOTE

1. When non-qualified added components are given qualified status by the procedures in 3.6.2.2 (1) of CECC 63 000, structural similarity for hybrid circuits require the same manufacturing source for each added component.

TABLE 10 - PACKAGING

Characteristics	Similarity rules
<u>Encapsulation process</u>	
1 - Non-encapsulated	Combination within the limits of the substrate size (see Table 5) and same lead attachment methods and materials
2 - Embedded	No combination allowed between different material and protective coating systems
3 - Cavity (organic seal)	
. Package material	Same
. Sealing material	Same
. Encapsulated environment	Same or lesser humidity content (dew point)
4 - Cavity (inorganic seal)	
. Package material	Same
. Sealing material	Same
. Encapsulated environment	Same or lesser humidity content (dew point)
<u>Lead</u>	
1 - Material, process and coating	Same material for leads and insulating material
2 - Seal lead length	Same or greater
3 - Material and method of connection to substrate	Same
4 - Mechanical material characteristics	Same or greater
5 - Spacing	Same or greater
6 - Dimensions	Same or greater cross sectional area
<u>Marking system and method of application</u>	Any possible system and method of application
<u>Substrate attachment</u>	Same material and process

TABLE 11 - MASS AND DIMENSIONS OF PACKAGE

			
Parameter	CQC or Master circuit	Associated devices	Limits (1) (2)
Length	X	x	$aX \leq x \leq bX$
Width	Y	y	$aY \leq y \leq bY$
Surface	$S = XY$	$s = xy$	$eS \leq s \leq fS$
Thickness	Z	z	$gZ \leq z \leq hZ$
Number of terminations	N	n	$uN \leq n \leq vN$
Mass	M	m	$jM \leq m \leq kM$
Mass per termination	$\frac{M}{N}$	$\frac{m}{n}$	$w \frac{M}{N} \geq \frac{m}{n} \quad (3)$

- (1) Where there are two limits, the more severe shall be considered
(2) For cylindrical packages apply the same rule with $X = Y = \text{diameter}$
(3) This criterion is applicable only where the mechanical tests are carried out with the F&HIC fixed by its terminals. It is not applicable to cylindrical packages with diameter less than 15,41 mm nor to rectangular packages with dimensions less than 17 mm x 17 mm

TABLE 12 - LIMITS OF ASSOCIATION IN RELATION WITH MASS AND DIMENSIONS

Assessment Levels (3) (4)	a	b	e	f	g	h	j	k	u	v	w
K (1)	0,5	1,5	0,25	1,5	0,8	1,2	0,2	1,8	0,5	2	1,2
K (2)	0,2	1,5	0,1	1,5	0,8	1,2	0,2	1,8	0,5	2	1,2
L (1)	0,3	2	0,3	2	0,5	1,5	n.a.	n.a.	0,3	2	n.a.
L (2)	0,2	2	0,1	2	0,5	1,5	n.a.	n.a.	0,3	2	n.a.
M (1)	0,3	2	n.a.	n.a.	0,5	1,5	n.a.	n.a.	n.a.	n.a.	n.a.
M (2)	0,2	2	n.a.	n.a.	0,5	1,5	n.a.	n.a.	n.a.	n.a.	n.a.

- (1) For passive HICs
(2) For active HICs
(3) "n.a." means "not applicable"
(4) The letters used in the headings correspond to those of column 4 of Table 11

TABLE 13 - COMBINATION CRITERIA FOR ENVIRONMENTAL TESTING

This table serves as the basis for establishing test programmes for the assessment or the extension of a claimed capability. This table aligns with Table 1 of this specification and Tables 2 and 3 of the blank detail specification.

It specifies per test group the technological aspects and criteria to be met for deciding on structural similarity between a given non-encapsulated or embedded hybrid integrated circuit and/or CQCs.

When one or more of the criteria of a test group are not met, structural similarity principles can not be applied and the manufacturer's capability has to be extended to cover the particular requirements for that test group.

Note : Requirements are either mandatory (x) or not applicable (-).

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
APPLICABLE TEST TABLE : - Sealing (Cavity circuits only)						
Sub-Group 04						
1	-	-	x	x	Same or less severe test schedule(s) and/or conditions	
2	-	-	x	x	Same package style/material and construction method (Table 10)	
3	-	-	x	x	Similarity within Table 11	
4	-	-	x	x	Same materials at peripheral and final seal faces and same method of making seals (Table 10)	
5	-	-	x	x	Same basic substrate material (Table 5)	(1)
6	-	-	x	x	Same external lead material, plating/coating process and material(s) and thickness of plating/coating (Table 10)	(2)
(1) Applicable only when the substrate is an integral part of the sealing envelope. (Integral Substrate Package)						
(2) Only applicable where leads form part of the seal						
APPLICABLE TEST TABLES : - Vibration swept frequency or						
Group 1						
Sub-Group C2						
1	x	x	x	x	Same or less severe test schedules and/or conditions	
2	-	x	x	x	Same package style/material and construction method (Table 10)	
3	x	x	x	x	Similarity within Table 11	
4	-	x	x	x	Same material(s), methods and process conditions used for encapsulation of the circuit (Table 10)	

(Continued)

(Continuation)

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
5	x	x	x	x	Same material specifications and process methods for attachment and connection of added components to substrate and substrate to package (Tables 6, 7, 8, 9)	(1)
6	-	-	x	x	Same materials at peripheral and final seal faces and same method of making seals (Table 10)	
7	-	x	x	x	Same lead X-sectional dimensions at exit from package or seal (Table 10)	
8	x	-	-	-	Same lead X-sectional dimensions at point of mounting	
9	-	x	x	x	Same or greater lead length along minimum seal path (Table 10)	
10	-	x	x	x	Same method of external lead anchorage direct to substrate - if applicable (Table 10)	
11	-	x	-	-	Same basic materials and methods for connection from lead-throughs inside package to internal circuitry (Table 7)	
12	x	x	x	x	Same external lead material, plating/coating process, and material(s) (Table 10)	
13	x	x	-	-	Same basic substrate material (Table 5)	
14	x	x	-	-	Nominal substrate thickness within 10 % of nominal CQC (Table 5)	
15	-	x	x	x	Same or lesser range of material(s) and methods used for intra-connection links on or between substrates (Table 6)	
16	-	-	x	x	Same or less severe deflection of package base and lid under maximum specified acceleration (mathematical model acceptable) (Table 10)	
17	x	-	x	x	P_1 is the same or less where : $P_1 = \frac{\text{Weight of sub. assembly or component}}{\text{Min.spec X-sect. of attachment joint(s)}}$	(2)
18	x	-	x	x	Same design rules relating intra-connection (wire or tape) unsupported lengths and clearances	(1)
19	x	x	x	x	Mass and dimensions within the limits of Table 12	
20	x	x	x	x	Same package mounting method used for tests	(1)
21	x	x	x	x	Same lead hardness specification (Table 10)	
22	-	-	x	x	Same filling, if non gaseous (Table 9)	(1)
23	x	x	x	x	Same or lesser range of added passive component generic type (Table 9)	

(Continued)

(Continuation)

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
24	x	x	x	x	Same or lesser range of added semi-conductor component generic type (Table 8)	
25	x	x	x	x	Same or lesser range of basic film materials (Table 6)	
26	x	x	x	x	Same basic film process (Table 6)	
(1) Applicable only to circuits intended to be mounted by the leads. (2) Applicable to assembled substrate including any added components attached to cavity package base and also to individual added components attached to substrate.						
<u>APPLICABLE TEST TABLE</u> : - Resistance to soldering heat - Resistance to solvents <u>Group 2</u> - Change of temperature <u>Sub-Group C3</u> - Damp heat, steady state						
1	x	x	x	x	Same or less severe test schedule and/or conditions	
2	-	x	x	x	Same package style/material and construction method (Table 10)	
3	-	x	x	x	Similarity within Table 11	
4	-	x	x	x	Same material(s), methods and process conditions used for encapsulation of the circuit (Table 10)	
5	x	x	x	x	Same material specification(s) and process methods for attachment and connection of added components to substrate and substrate to package (Table 10)	
6	-	-	x	x	Same materials at peripheral and final seal faces and same method of making seals (Table 10)	
7	-	x	x	x	Same lead X-sectional dimensions at exit from package or seal (Table 10)	
8	x	x	x	x	Same or greater basic lead spacing within any row of leads (Table 10)	
9	x	x	x	x	Same method of external lead anchorage direct to substrate - if applicable (Table 10)	
10	-	x	-	-	Same basic materials and methods for connection from lead-throughs inside package to internal circuitry (Table 10)	(1)
11	x	x	x	x	Same external lead material, plating/coating process and material(s) and thickness of plating/coating (Table 10)	
12	x	x	x	x	Same basic substrate material (Table 5)	
13	-	x	-	-	Nominal substrate thickness within $\pm 10\%$ of nominal CQC (Table 5)	(1)

(Continued)

(Continuation)

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
14	-	x	x	x	Same or greater insulation surface distance at exit of lead(s) from seal (Table 10)	
15	-	x	x	x	Same or lower mean voltage gradient across the insulation surface at exit of lead(s) from seal, as identified from rated electrical conditions of use (Table 10)	
16	-	x	-	-	Same or greater thickness of embedding plastic(s) over critical interfaces (Table 10)	
17	x	x	x	x	Same marking materials system and method of application (Table 10)	
18	-	x	x	x	Same or greater lead length along minimum seal path (Table 10)	
19	x	x	x	x	Same or lesser range of basic film materials (Table 6)	
20	x	x	x	x	Same basic film process (Table 6)	
21	-	x	-	-	Same design rules relating intra-connections (wire or tape), free lengths and clearances (Tables 7, 9)	
22	x	x	x	x	Same or lesser range of added passive component generic types (Table 9)	
23	x	x	x	x	Same or lesser range of added semi-conductor component generic types (Table 7)	
(1) These requirements can be collectively waived by demonstrating that the circuit structure is such that, compared to the CQC, the same or lower temperature rise at comparable material interfaces occurs during the solder heat test						
<u>APPLICABLE TEST TABLES</u> : - Solderability - Tensile <u>Group 3</u> - Bending <u>Sub-Group D2</u> - Thrust						
1	-	x	x	x	Same package style/material and construction method (Table 10)	
2	-	x	x	x	Similarity within Table 11	(1)
3	-	x	x	x	Same material(s), methods and process conditions used for encapsulation of the circuit (Table 10)	
4	-	x	x	x	Same lead X-sectional dimensions at exit from package or seal (Table 10)	
5	-	x	x	x	Same lead hardness specification (Table 10)	
6	-	x	x	x	Same or greater basic lead spacing within any row of leads (Table 10)	(1)

(Continued)

(Continuation)

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
7	x	x	x	x	Same external lead material, plating/ coating process and material(s) (Table 10)	(2)
8	-	x	x	x	Same method of external lead anchorage direct to substrate, if applicable (Table 10)	
9	-	x	x	x	Same or greater lead length along minimum seal path (Table 10)	
10	-	-	x	x	Same insulation (basic) material used for lead seals (Table 10)	(3)
11	-	x	x	x	Same or greater minimum external X-sectional area of individual leads (Table 10)	
12	-	x	x	x	Same or less meniscus height permitted on leads at exit from seal surface plane	
13	x	x	x	x	Same solderability assessment method and equipment used.	
(1) Applicable to bending (row) only. (2) Applicable only to cavity packages with metal bodies. (3) Applicable to tensile and bending (wire/strip) only.						
APPLICABLE TEST TABLES : - Cold storage <u>Group 4</u> - Dry heat storage <u>Sub-Group C4</u>						
1	x	x	x	x	Same or less severe test schedules/and or conditions	
2	-	x	x	x	Same package style/material and construction method (Table 10)	
3	x	x	x	x	Similarity within Table 11	
4	-	x	-	-	Same material(s), methods and process conditions used for encapsulation of the circuit (Table 10)	
5	x	x	x	x	Same material specification(s) and process methods for attachment and connection of added components to substrate and substrate to package (Tables 7 to 10)	
6	-	-	x	x	Same materials at peripheral and final seal faces and same method of making seals (Table 10)	
7	-	-	x	x	Same internal gas or other filling, including any impurity and water content specifications (Table 10)	
8	x	x	x	x	Same basic substrate material (Table 5)	
9	x	x	x	x	Same or lesser range of added passive component generic types (Table 9)	

(Continued)

(Continuation)

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
10	x	x	x	x	Same or lesser range of added semi-conductor component generic types (Tables 7 and 8)	
11	x	x	x	x	Comparable requirements in the stability of film and added circuit elements (Dry heat only) (Tables 5 to 9)	
12	x	x	x	x	Same or lesser range of basic film materials (Table 6)	
13	x	x	x	x	Same basic film process (Table 6)	
APPLICABLE TEST TABLES : - Endurance 1000 h Group 5 - Endurance 2000 h Sub-Group D1						
1	x	x	x	x	Same or less severe test schedules and/or conditions	
2	-	x	x	x	Same package style/material and construction method (Table 9)	
3	-	x	x	x	Similarity within Table 11	
4	-	x	x	-	Same material(s), methods and process conditions used for encapsulation of the circuit (Table 10)	
5	x	x	x	x	Same material specification(s) and process methods for attachment and connection of added components to substrate and substrate to package (Tables 7 to 10)	
6	-	-	x	x	Same materials at peripheral and final seal faces and same method of making seals (Table 10)	
7	-	-	x	x	Same internal gas or other filling, including any impurity and water content specifications (Table 10)	
8	x	x	x	x	Same basic substrate material (Table 5)	
9	x	x	x	x	Same or lesser range of added passive component generic types (Table 9)	
10	x	x	x	x	Same or lesser range of added semi-conductor component generic types (Tables 7 and 8)	
11	x	x	x	x	Same or lower maximum temperature at comparable material interfaces under rated electrical conditions of use	
12	x	x	x	x	Comparable or lesser requirements in the stability of the film and added circuit elements (Tables 6 to 8)	
13	x	x	x	x	Same or lesser range of basic film materials (Table 6)	
14	x	x	x	x	Same basic film process (Table 6)	

(Continued)

(Continuation)

No	Unen- cap- sula- ted	Em- bed- ded	Cavi- ty (Orga- nic Seal)	Cavi- ty (Inor- ga- nic Seal)	Criteria	Notes
15	x	x	x	x	Same geometrical, electrical and thermal design rules applied to film layout (Table 6)	
16	x	x	x	x	Same trimming process applied to film elements (Table 6)	

APPENDIX D

MINIMUM CONTENTS OF A MANUFACTURER'S CAPABILITY MANUAL FOR THIN FILM CIRCUITS

D.1 SCOPE

This appendix establishes the requirements for the capability manual for thin film hybrid integrated circuits. It does not apply to thick film or semiconductor integrated circuits.

The term hybrid is defined in 2.3.10 of CECC 63 000 and the scope of this appendix includes the use of any of the added components in association with the basic thin film technology.

Note : In addition to the requirements stated herein the manufacturer may include additional information for example on process control and inspection schedules, which he considers necessary for the full control of his capability.

For ease of reference the capability manual shall give information under the headings given below as appropriate. Under item 1 of the capability manual, the manufacturer shall declare the entire scope of his capability and state which assessment level applies. Where the procedure under 3.2 of CECC 63 000 is invoked the capability manual shall make reference to the surveillance of those stages which are not carried out under the direct surveillance of an approved Chief Inspector.

D.2 CUSTOMER PARTICIPATION IN THE LAYOUT

The manufacturer shall declare whether he permits customer participation in the technological design and layout of circuits. In the case of a device manufactured to this standard where the customer has provided the design and layout, it shall be the responsibility of the manufacturer to ensure that his approved design data and layout rules have been followed.

D.3 CAPABILITY ABSTRACT

The statement of basic technology in addition to the details required in 1.2 of CECC 63 000 for thin film integrated circuits shall include the following which shall be used in the QPL:

- Type of substrate, for example glass, alumina
- Method of film deposition, for example vacuum evaporation, sputtering
- Method(s) of pattern formation, for example photolithography, spark erosion, ion etching
- Range of film elements, for example conductors, resistors, capacitors, and so on
- Methods of trimming of film elements, for example laser, spark erosion, etching

- Types of added components, for example chip capacitors, discrete semiconductor devices, semiconductor dice, and related methods of attachment
- Methods of interconnecting added components within the film circuits according to type, for example bonding, soldering
- Methods of lead attachment to the substrate, for example soldering
- Basic encapsulation method, for example hermetic, plastic
- (Not for integral substrate packages) Methods of attaching substrate to package (for example eutectic bond, organic bond, etc...)
- Boundaries of capability - Range of values/tolerance, matching where appropriate, conductors, resistors, capacitors, etc...

Note : It may not be possible to achieve all the limits of the capability in combination.

D.4 MATERIALS AND ADDED COMPONENTS

This section of the capability manual shall :

- Identify and provide evidence of the existence of purchasing specifications for the materials which are critical for the quality of the products
- Describe the methods used to verify the suitability of materials for production and identify the documentation necessary to ensure consistent quality of the specified materials
- Indicate the inspection methods for added components to be incorporated. See 3.6.2 of CECC 63 000.

D.4.1 Materials purchasing specifications.

The manual shall identify the relevant purchasing specifications under the appropriate headings as listed below. The "specification contents" column lists the data which shall be included in the purchasing specifications but such data is not required in the capability manual. The list of items included in each sub-clause is intended for guidance and is not exhaustive. Items are applicable where relevant to the particular process technology.

(1) Materials in circuit and package

	<u>Specification contents</u>
- Substrates	Types of material, composition and characteristics, thermal and mechanical characteristics.
- Deposited materials	Types, composition and characteristics.

Specification contents

- | | |
|---------------------------------------|---|
| - Assembly materials | Types of materials, for example lead frames, adhesives, solders, leads and terminations, varnishes. |
| - Added components | Types, specification numbers or other reference data of the added components approved for use. Information on preferred types of components. In addition the capability manual shall provide details of an appropriate purchasing system and inspection and testing requirements for added components. |
| - Package and encapsulation materials | Types of materials, for example cases, caps, lids, finishes, platings, mouldings, thermo-setting resins, varnishes, coatings, identification and marking.
Material combinations, for example Kovar-glass, glass-ceramic.
Type of plastic used for plastic or part-plastic encapsulations.
List of standard packages used, or reference to control of drawings for non-standard packages. |

(2) Materials used in processing

- | | |
|------------------------|---|
| - Artwork | Types and characteristics of materials used in circuit design and artwork, for example dimensional stability, durability. |
| - Pattern forming | Types and characteristics of photographic plates, emulsions, masks, electrodes, etchants. |
| - Processing materials | Types of materials, chemicals used in circuit preparation, adjustment, trimming. |
| - Assembly materials | Types and characteristics of materials used as aids to assembly, for example fluxes, cleaning agents. |

D.4.2 Material verification

The manual shall describe the methods for the verification of the suitability of the above materials for production and other documentation necessary to ensure consistent quality of those materials which are critical to the quality of products.