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Harmonized system of quality assessment for electronic components — Generic specification: Monolithic integrated circuits —

Addendum 1. Screening

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National foreword

This addendum to BS CECC 90000:1982 issue 2 has been prepared under the direction of the Electronic Components Standards Committee. It is identical with **4.10** and Appendix A of CECC 90000 “*Harmonized system of quality assessment for electronic components. Generic specification: Monolithic integrated circuits*” which were issued separately by CENELEC Electronic Components Committee (CECC) in 1983. The Note on page 3 of issue 2 of BS CECC 90000 refers to **4.10**, and the page numbers given to the new clause and appendix in this addendum are continuous from the page numbers given in BS CECC 90000. For general information on terminology, quality assessment procedures, measurement conditions and related documents reference should be made to the national foreword in BS CECC 90000.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, pages 1 to 44, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

4.10 Screening

This clause gives details of the screens or test sequences appropriate to different classes of screening for integrated circuits.

Such screens or test sequences are to be used when prescribed by the DS and in accordance with the general requirements of the relevant SS. The screening sequences shall be as given in **4.10.1**.

All screening tests precede the normal Group A, B, and C tests. The result from any Group A, B or C tests on devices which have been subject to screening tests shall be recorded separately, and shall not be included in CTR data for the corresponding inspection category.

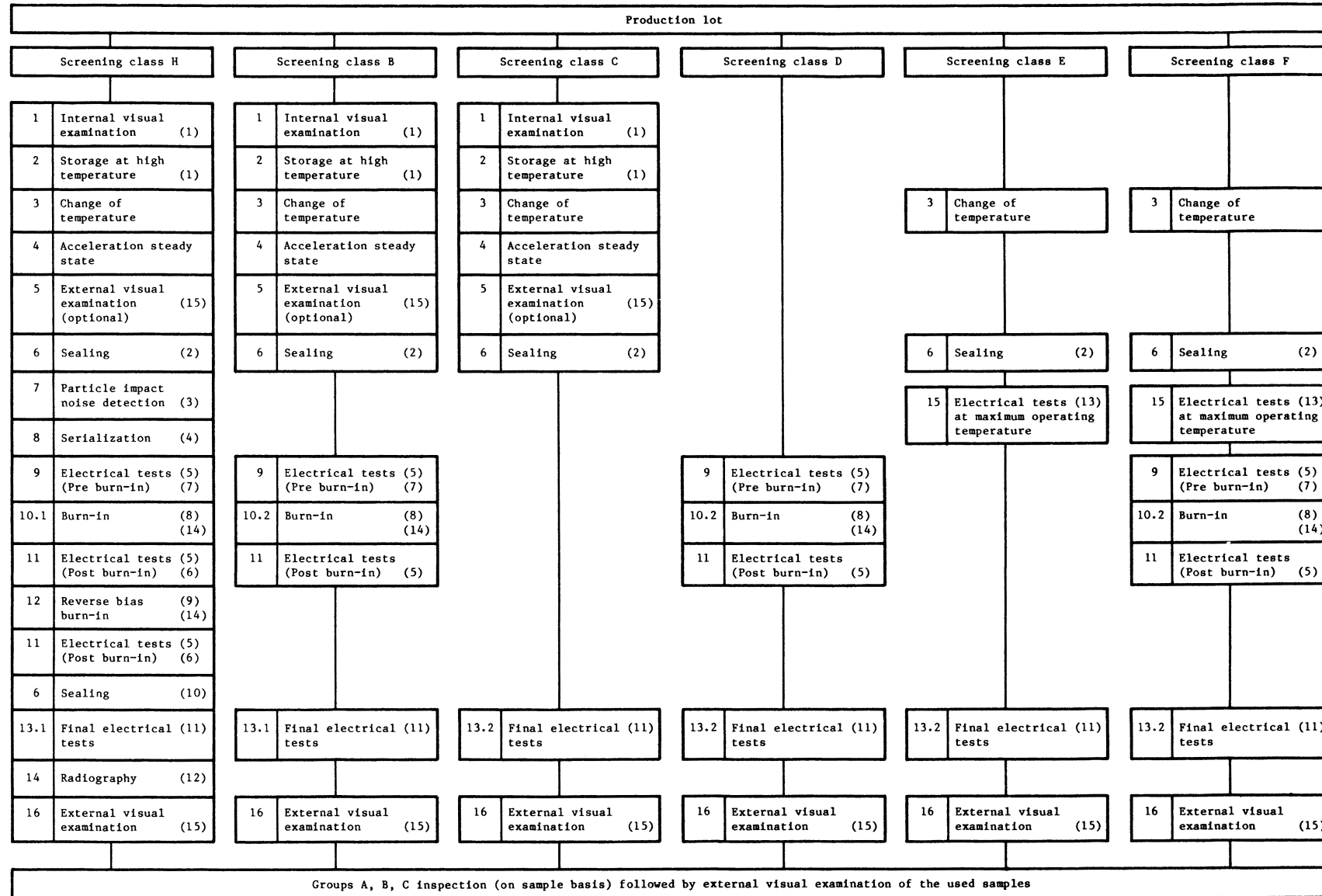
For the purposes of Group A, B, and C tests, an inspection lot is not formed until screening has been completed.

Production lots submitted to burn-in screen shall be rejected if more than 10 % of the devices fail to pass all tests up to and including final electrical tests.

4.10.1 Screening procedures

The following diagrams give the screens or test sequence applicable to each class of screening. They shall be read in conjunction with the notes which follow.

Screening procedures: flow diagrams
(Screen or test number at left of each block)



NOTES:

(1) The storage at high temperature is used as stabilization and shall be applied to devices using molybdenum-gold multilayered conductors immediately prior to performing internal visual examination.

For cavity devices using metallurgical systems other than molybdenum-gold, it shall be permissible to divide the total minimum stabilization time between pre-seal and post-seal stabilization as long as the total stabilization time equals or exceeds 24 h, the post-seal stabilization time equals or exceeds 16 h, and the pre-seal stabilization occurs immediately prior to sealing.

(2) The sealing test

- applies only for cavity devices
- is optional at this stage for class H devices
- for classes B, C, E or F devices, shall be performed in any sequence after the last thermal or mechanical screen and before final electrical tests, but after completion of all forming and shearing operations on the terminals.

(3) The particle impact noise detection (PIND) test may be performed in any sequence after acceleration, steady state screen and before the last post burn-in electrical tests. Until the test method has been agreed, this test may be omitted from the screening sequence.

(4) The serialization operation

- applies only for class H devices, unless otherwise specified in the DS
- is performed before the pre burn-in electrical tests
- is defined as the completion of devices general marking by an own number allotted and recorded by the certifying Chief Inspector, following a unity step increasing sequence for each device's type.

(5) The pre burn-in and post burn-in electrical tests shall be performed to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criterion when a PDA is applicable.

These tests need not include all specified device parameters but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

(6) The results of pre burn-in and post burn-in electrical tests of each class H device shall be read and recorded.

(7) The pre burn-in electrical tests are optional for classes B, D or F devices, at the manufacturer's discretion except when delta limits measurements are required.

When delta limits measurements are required, they shall be specified in the DS and shall be included as pre burn-in and post burn-in electrical tests.

All devices shall be tested for those parameters requiring delta calculations and the maximum permitted deviations for each parameter shall be specified.

The procedure for device traceability shall be specified if other than by serialization or agreed between the Chief Inspector and the ONS.

(8) A burn-in acceleration method

- shall never be applied to class H devices
- this method may be used for screening classes B, D, or F provided a temperature-time equivalence has been demonstrated to the satisfaction of the ONS. This requires a demonstration that there is a predominant failure mechanism with an established value of activation energy.

If a burn-in acceleration method is used on devices having an aluminium-gold metallurgical system, the acceleration steady state screen shall be performed subsequent to burn-in and before final electrical tests.

(9) The reverse bias burn-in is a requirement only when specified in the relevant DS and is recommended only for certain MOS, linear or other circuits where surface sensitivity may be of concern.

When reverse bias burn-in is not required, the preceding post burn-in electrical tests are omitted.

The order of performing the burn-in and the reverse bias burn-in may be inverted.

(10) The sealing test

- applies only for cavity devices
- applies only for class H devices
- shall be performed in any sequence after the last post burn-in electrical tests and before the last external visual examination but after completion of all forming and shearing operations on the terminals.

(11) The final electrical tests ensure that all the devices meet the electrical requirements of the relevant DS and shall include, as minimum, all parameters, limits and conditions of test which are specifically identified in the DS as final electrical requirements. Final electrical test requirements that are duplicated in the last post burn-in electrical tests need not be repeated as final electrical tests.

(12) The radiographic screen may be performed in any sequence after serialization. Until the test method has been agreed, this test may be omitted from the screening sequence.

(13) The electrical tests at maximum operating temperature apply only for non-cavity devices.

(14) Burn-in test. The integrated circuits shall be subjected to the burn-in screen by operating them in accordance with one of the specified test conditions given in the SS.

The units shall be cooled down under bias conditions to an estimated junction temperature not exceeding 35 °C. Alternatively, natural, or convected cooling may be applied after removal of bias, provided that no more than 30 min elapse between removal and the time that junction temperatures drop to an estimated 35 °C maximum.

(15) This external visual examination, at the manufacturers option, may be conducted after any of the thermal/mechanical screens, after the sequence or after the seal test.

Specified conditions. The following shall be prescribed by the DS:

- general procedures if other than that specified in the relevant SS
- the maximum allowable deviations in electrical test results
- electrical conditions to be applied to all terminals.

4.10.2 Screens and tests description

The screens and tests are defined as below, referring to the screen or test numbers and notes of clause 4.10.1.

Screen or test number	Screen or Test	Reference to CECC 90000 unless otherwise stated	Conditions	See Note
1	Internal visual examination	4.2.1	See Appendix A of CECC 90000	(1)
2	Storage at high temperature	4.6.1(1)	$T = T_{\text{stg max.}}$ $t = 24 \text{ h min.}$ No final measurement	(1)
3	Change of temperature	4.6.8(1)	$T_{\text{min}} = T_{\text{stg min.}}$ $T_{\text{max.}} = T_{\text{stg max.}}$ 10 cycles No final measurement	
4	Acceleration steady state	4.6.7	Acceleration = $294\,000 \text{ m/s}^2$ ($30\,000 g_n$) unless otherwise specified Direction = Y_2 No final measurement	
5	External visual examination (optional)	4.2.2	4.2.2	
6	Sealing a : tracer gas method with mass spectrometer b : gross leak	4.6.9(1) 4.6.9(2)	$4,96 \times 10^{-8}$ $\frac{\text{Pa} \cdot \text{m}^3}{\text{s}}$ unless otherwise specified 4.6.9(2)	(2) (10)
7	Particle impact noise detection	under consideration	under consideration	(3)
8	Serialization	—	—	(4)
9	Electrical tests (pre burn-in)	CECC 90100	As for Sub-Groups A2 and A3 of relevant DS unless specified	(5) (6) (7)
10.1	Burn-in	—	$T = \text{max.}$ operating temperature $t = 240 \text{ h min.}$ Electrical conditions as specified in the DS	(8) (14)

Screen or test number	Screen or Test	Reference to CECC 90000 unless otherwise stated	Conditions	See Note
10.2	Burn-in		$T_{amb} = 125\text{ }^{\circ}\text{C}$ unless otherwise limited by the technology when a lower limit is specified in the family or DS $t = 168_{-8}^{+0}\text{ h}$ or any equivalent combination of it Electrical conditions as specified in the DS	(8) (14)
11	Electrical tests (post burn-in)	—	As for Sub-Groups A2 and A3 of relevant DS unless otherwise specified The DS will prescribe the maximum deviations allowable from the results recorded in the preceding electrical tests	(5) (6)
12	Reverse bias burn-in	—	$T_{amb} = 150\text{ }^{\circ}\text{C}$ unless otherwise limited by the technology when a lower limit is specified in the family or DS $t = 72\text{ h min.}$ Electrical conditions as specified in the DS	(9) (14)
13.1	Final electrical tests	—	As for Sub-Groups A2, A3, A4a, A4b and A5 of the relevant DS	(11)
13.2	Final electrical tests	—	As for Sub-Groups A2 and A3 of the relevant DS	(11)
14	Radiographic	Under consideration	Under consideration	(12)
15	Electrical tests at max. operating temperature	—	As for Sub-Groups A4a of the relevant DS unless otherwise specified	(13)
16	External visual examination	4.2.2	4.2.2	(15)

Appendix A to CECC 90000 Issue 2

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Preface

Appendix A the generic specification (GS) for monolithic integrated circuits CECC 90000 was prepared by CECC WG 9 "Integrated Circuits".

The text of this Appendix was circulated to the CECC for voting in document CECC(Secretariat)862 in November 1979 and was formally approved by the CECC for printing as a CECC specification.

The text is printed in Appendix form to provide a self contained document are readily suitable for inspection.

The text of this Appendix was circulated to the CECC for voting in the documents listed below:

Document	Date of Voting	Report on the Voting
CECC (Secretariat) 862	November 1979	CECC (Secretariat) 956

Conversion of dimensions from inches into μm

The following table converts the original mil (1 mil = 0.001 in) figures into specified values of μm required for this appendix.

Original values (in mil)	Computed values (in μm)	Specified values (in μm)
0,1	2,54	2,5
0,25	6,35	6
0,50	12,7	12
1	25,4	25
2	50,8	50
3	76,2	75
3,5	88,9	90
5	127	125
10	254	250

A.1 Purpose

The purpose of these tests is to check that the internal materials, construction, and workmanship of microcircuits comply with the requirements of the applicable specification.

These tests will normally be used prior to capping or encapsulation on a 100 % inspection basis to detect and eliminate devices with internal defects, that could lead to device failure in use. They may also be employed on a sampling basis prior to capping to determine the effectiveness of the manufacturer's quality control and handling procedures for microelectronic devices.

Complex microcircuits may require substitution of alternate screening procedures for visual inspection requirements pertaining to metal coverage, oxide, and diffusion faults that are difficult or impractical to perform. These alternate screening methods and procedures are documented in the applicable detail specification (DS) and their use shall be on an optional basis.

A.2 Apparatus

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gauges, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions concerning the acceptability of the device being examined. Adequate fixing or mounting arrangements shall be provided for handling devices during examination to permit efficient operation without inflicting damage to the units.

A.3 Procedures

A.3.1 Introduction

A.3.1.1 General

The device shall be examined in a sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable specification. The inspections and requirements in this method shall be required inspections for all devices and locations to which they are applicable. Where the criterion is intended for a specific device process or technology, It has been indicated.

A.3.1.2 Sequence of inspection

The order in which requirements are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Visual requirements specified in **A.3.2.1.2**, **A.3.2.1.5**, **A.3.2.1.7**, **A.3.2.2**, **A.3.2.7** 5) and 6), **A.3.2.8**, **A.3.2.9** 1) to 4), and **A.3.3.1.2**, **A.3.3.1.5**, **A.3.3.1.7**, **A.3.3.2**, **A.3.3.7** 5) and 6), **A.3.3.8**, **A.3.3.9** 1), 2) and 4) may be examined prior to die attachment. Visual requirements specified in **A.3.2.6.2**, **A.3.2.6.3**, **A.3.3.6.2** and **A.3.3.6.3** may be examined prior to bonding without re-examination after bonding. Visual requirements specified in **A.3.3.1.1** and **A.3.3.3** may be examined prior to die attachment at "high magnification" provided they are re-examined after die attachment at "low magnification". When inverted mounting techniques are employed the inspection requirements contained herein that cannot be performed after mounting shall be conducted prior to attachment of the die.

A.3.1.3 Air cleanliness classes

The two classes defined by this specification are given below. Classifications are based on particle count with a maximum allowable number of particles per unit volume 0,5 µm and larger or 5,0 µm and larger. Particle size is expressed as the apparent maximum linear dimension or diameter of the particle (while measurements from light scattering equipment may vary some from maximum linear dimension this variation is not usually considered significant for normal clean room monitoring requirements). Particle counts are to be taken at specified intervals during work activity periods at a location which will yield the particle count of the air as it approaches the work location. The preferred location for the particle count is at work level height with the sampling probe pointed into the airstream.

Other classifications (for example 35,350) may be used for particle count levels when special conditions dictate their use.

A.3.1.3.1 Class 3,5: Particle count not to exceed a total of 3,5 particles per litre of a size 0,5 µm and larger or 0,35 particle per litre of a size 5 µm and larger.

A.3.1.3.2 Class 3 500: Particle count not to exceed a total of 3 500 particles per litre of a size 0,5 µm and larger or 25 particles per litre of a size 5 µm and larger.

A.3.1.4 Inspection control

In all cases, examination prior to final preseal inspection shall be performed under the same quality programme that is required at the final preseal inspection. Care shall be exercised after inspections to **A.3.1.2**, to ensure that defects created during subsequent handling are detected and rejected at final preseal inspection. During the time interval between visual inspection and preparation for sealing, devices shall be stored in a controlled environment.

Devices examined to **A.3.2** requirements shall be inspected and prepared for sealing in a class 3,5 environment and devices examined to **A.3.3** shall be inspected and prepared for sealing in a class 3 500 environment. The maximum allowable relative humidity in either environment shall not exceed 65 %. Devices shall be in covered containers when transferred from one controlled environment to another.

A.3.1.5 Magnification

“High magnification” inspection shall be performed perpendicular to the die surface with the device under illumination normal to the die surface.

“Low magnification” inspection shall be performed with either a monocular, binocular, or stereo-microscope, and the inspection performed within an angle of 30 degrees from the perpendicular to the die surface with the device under suitable illumination. The inspection requirements of **A.3.2.4**, **A.3.3.4** and **A.3.3.6.1** may be examined at “high magnification” at the manufacturer’s option.

A.3.1.6 Definitions

- 1) Active circuit area includes all kinds of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.
- 2) Controlled environment shall be in accordance with the requirements of class 3,5 environment for air cleanliness. The maximum allowable relative humidity shall not exceed 50 %. The use of an inert gas environment such as nitrogen shall satisfy the requirements for storing in controlled environment.
- 3) Diffusion tub is an isolated volume of semiconductor material, either “P” or “N” type, surrounded by isolation material.
- 4) Foreign material is as any material that is foreign to the microcircuit or any non-foreign material that is displaced from its original or intended position within the microcircuit package. It shall be considered attached when it cannot be removed by a nominal gas blow (approximately 140 kPa). Conductive foreign material is defined as any substance that appears opaque under conditions of lighting and magnification used in routine visual inspection. Particles shall be considered embedded in the glassivation when there is evidence of colour fringing around the periphery of the particle.
- 5) Functional circuit elements are diodes, transistors, crossunders, capacitors and resistors.
- 6) Gate oxide bridge is the area lying between the drain and source diffusion of MOS structures. References to the metallization covering the gate oxide bridge shall include all materials that are used for the gate electrode.
- 7) Glassivation is the layer of transparent insulating material that covers the active circuit area including metallization, except bonding pads and beam leads. Cracking is the presence of minute cracks in the glassivation
- 8) Junction is the outer edge of a passivation step that delineates the boundary between “P” and “N” type semiconductor material
- 9) Multilayered metallization (conductors) is two or more layers of metal or any other material used for inter-connections that are not isolated from each other by a grown or deposited insulating material. The term “underlying metal” shall refer to any layer below the top layer of metal
- 10) Multilevel metallization (conductors) is two or more layers of metal or any other material used for inter-connections that are isolated from each other by a grown or deposited insulating material
- 11) Operating metallization (conductors) is metal or any other material used for inter-connection except metallized scribe lines, test patterns, unconnected functional circuit elements, unused bonding pads, and identification markings
- 12) Organic polymer (epoxy) vapour residue is the material that is emitted from the polymer, that forms on an available surface
- 13) Original width is the width dimensions or distance that is intended by design (for example original metal width, original diffusion width, original beam width, etc.)

14) Passivation step is a change in thickness of the passivation for metal to metal or metal to silicon inter-connection, by design, excluding lines on the surface where passivation layers have been removed as a result of normal device processing

15) Passivation is the silicon oxide, nitride or other insulating material that is grown or deposited directly on the die prior to the deposition of metal

16) Peripheral metal is metal that lies immediately adjacent to or over the scribe grid.

17) Thick film is a conductive/resistive/dielectric system that is a film having greater than 5 μm in thickness

18) Thin film is a conductive/resistive/dielectric system that is a film equal to or less than 5 μm in thickness

19) Substrate is the supporting structural material into and/or upon which the passivation, metallization and circuit elements are placed.

A.3.1.7 Interpretations

For inspection performed in the range of 75X to 100X magnification, the requirements of “2,5 μm of passivation, or metal” can be satisfied by a “line of separation” or a “line of metal”. Reference herein to “that exhibits” shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present and shall not require confirmation by any other method of testing. If other methods of test are to be used to confirm that a reject condition does not exist, they shall be approved by the Chief Inspector.

A.3.2 Test Condition “A”

Internal visual examination as required in A.3.2.1 to A.3.2.6 shall be conducted on each microcircuit and each circuit chip. In addition, the applicable requirements contained in A.3.2.7 to A.3.2.9 shall be used for the appropriate microcircuit areas where glassivation, dielectric isolation or film resistors are used. The “high magnification” inspection shall be within the range of 100X to 200X, the “low magnification” within the range of 30X to 60X.

A.3.2.1 Metallization defects (high magnification)

No device shall be acceptable that exhibits the following defects in the operating metallization.

A.3.2.1.1 Metallization scratches: a scratch is any tearing defect including probe marks in the surface of the metallization.

- 1) Scratch in the metallization excluding bonding pads and beam leads that leaves less than 50 % of the original metal width undisturbed (see Figure 1)
- 2) Scratch in the metallization over a passivation step that leaves less than 75 % of the original metal width at the step undisturbed
- 3) Scratch in the bonding pad or fillet area that reduces the metallization patch width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization strip width. If two or more stripes enter a bonding pad, each shall be considered separately
- 4) Scratch in the metallization, over the gate oxide bridge (see Figure 3) (applicable to MOS structures)
- 5) Scratch in multilayered metallization excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 75 % of the original metal width undisturbed (see Figure 1)
- 6) Scratch, probe mark(s), etc. in the bonding pad area that exposes underlying passivation over more than 25 % of the original unglassivated metallization area

A.3.2.1.2 Metallization voids: a void is any region in the metallization where underlying metal or passivation is visible that is not caused by a scratch.

- 1) Void(s) in the metallization that leave less than 75 % of the original metal width undisturbed (see Figure 2)
- 2) Void(s) in the metallization over the gate oxide bridge that leave less than 75 % of the metallization length (L) and width (W) between source and drain diffusion undisturbed (see Figure 3) (applicable to MOS structures)
- 3) Void(s) that leave less than 75 % of the metallization area over the gate oxide bridge undisturbed (applicable to MOS structures)

- 4) Void(s) in the bonding pad area that leave less than 75 % of its original unglassivated metallization area undisturbed
- 5) Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 75 % of the narrowest entering interconnect metallization stripe width (see Figure 4)
- 6) Void(s) in the metallization area of a thin film capacitor that reduces the metallization area by more than 25 %.

A.3.2.1.3 Metallization corrosion: metallization having any localized discoloured area shall be closely examined and rejected unless it is demonstrated to be harmless film, glassivation interface, or other obscuring effect.

A.3.2.1.4 Metallization adherence: any metallization lifting, peeling or blistering.

A.3.2.1.5 Metallization probing: requirements contained in A.3.2.1.1 shall apply as limitations on probing damage.

A.3.2.1.6 Metallization bridging: any metallization bridging where the separation between any two metallization paths is reduced to less than 50 % of the original separation or 25 µm whichever is greater. In no case shall this separation be less than 2,5 µm.

A.3.2.1.7 Metallization alignment:

- 1) Contact window that has less than 75 % of its area covered by metallization
- 2) Contact window that has less than a continuous 50 % of its perimeter covered by metallization
- 3) Contact window that has less than 75 % of its perimeter on two adjacent sides covered by metallization (applicable to MOS structures)

NOTE When by design, metal is completely contained in a contact window, requirements A.3.2.1.7 2) and 3) perimeter coverage can be deleted.

- 4) The minimum acceptable separation between metallization and adjacent contact window which is not intended to cover is 2,5 µm or 50 % of the design separation width, whichever is the greater
- 5) Any exposure of the gate oxide bridge from source to drain diffusion (applicable to MOS structures) (see Figure 5)
- 6) Any exposure of the gate oxide bridge that leaves less than 75 % of the metallization coincident with the source and drain diffusion junction line undisturbed (applicable to MOS structures)
- 7) Gate metallization not coincident with or extending over the diffused guard ring

NOTE Requirement A.3.2.1.7 7) applies to MOS structures containing a diffused guard ring. MOS devices that do not have a diffused guard ring shall have gate metallization extending not less than 2,5 µm beyond the gate oxide bridge (see Figure 3 and Figure 5).

A.3.2.2 Diffusion and passivation layer(s) faults (high magnification)

No device shall be acceptable that exhibits the following:

A.3.2.2.1 Diffusion faults:

- 1) Any diffusion fault that allows bridging between diffused areas (see Figure 6)
- 2) Any isolation diffusion that is discontinuous or any other diffused area with less than 25 % (50 % for resistors) of the original diffusion width that remains (see Figure 6).

A.3.2.2.2 Passivation faults:

- 1) Either multiple lines or a complete absence of passivation visible at the edge and continuing under the metallization (see Figure 7)

NOTE Double or triple lines at the edge of the defect indicate it can have sufficient depth to penetrate down to bare silicon.

- 2) Active junction not covered by passivation, unless in accordance with the design specification
- 3) Contact window that extends across a junction, unless in accordance with the design specification.

A.3.2.3 Scribing and die defects (high magnification)

No device shall be acceptable that exhibits:

- 1) Less than 6 µm of passivation visible between operating metallization or bond periphery and edge of the die

NOTE Requirements of A.3.2.3 1) can be excluded for beam leads and peripheral metallization including bonding pads where the metallization is at the same potential as the die.