

Specification for Harmonized system of quality assessment for electronic components

Family specification

Digital integrated HC MOS circuits series HC/HCT/HCU

Système harmonisé d'assurance de la qualité des composants électroniques

Spécification de famille

Circuits intégrés digitaux HC MOS series HC/HCT/HCU

Harmonisiertes Gütebestätigungssystem für Bauelemente der Elektronik

Familien-Spezifikation

Digitale integrierte HC MOS-Schaltungen Serien HC/HCT/HCU

8611-9

ECL/17

BS CECC 90109 : 1986

National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with CENELEC Electronic Components Committee (CECC) 90109 : 1986 'Family specification : Digital integrated HC MOS circuits series HC/HCT/HCU'.

This standard is a harmonized specification within the CECC System.

Terminology and conventions. The text of the CECC specification has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards; attention is drawn especially to the following.

The comma has been used as a decimal marker. In British Standards it is current practice to use a full point on the baseline as the decimal marker.

Cross-references. The British Standard which implements CECC 00100 is BS 9000: 'General requirements for a system for electronic components of assessed quality Part 2 : 1983 'Specification for national implementation of CECC basic rules and rules of procedure'.

<u>International standards*</u>	<u>Corresponding British Standards</u>
CECC 90000 : 1985	BS CECC 90000 : 1985 Harmonized system of quality assessment for electronic components. Generic specification : monolithic integrated circuits (Identical)
CECC 90100 : 1986	BS CECC 90100 : 1986 Harmonized system of quality assessment for electronic components. Sectional specification : digital monolithic integrated circuits (Identical)

The Technical Committee has reviewed the provisions of IEC 747, to which reference is made in the text, and has decided that they are acceptable for use in conjunction with this standard.

Scope. This standard lists the ratings, characteristics and inspection requirements which shall be included as mandatory requirements in accordance with BS CECC 90100 in any detail specification for these devices.

Detail specification layout. The front page layout of detail specifications released to BS CECC family or blank detail specifications will be in accordance with BS 9000 Circular letter No. 15.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

* Undated in text.

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

English version

Harmonized System of Quality Assessment for
Electronic Components

FAMILY SPECIFICATION:
DIGITAL INTEGRATED
HC MOS CIRCUITS
Series HC/HCT/HCU

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION DE FAMILLE:
CIRCUITS
INTEGRES DIGITAUX HC MOS
Séries HC/HCT/HCU

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

FAMILIEN-SPEZIFIKATION:
DIGITALE INTEGRIERTE
HC MOS-SCHALTUNGEN
Serien HC/HCT/HCU



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Issue
Edition
Ausgabe

CECC 90 109

Documents
AVA 1386 Document Sharing Hub

FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thoroby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for HC MOS DIGITAL INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom,

PREFACE

This family specification was prepared by CECC WGS "INTEGRATED CIRCUITS".

It is based, whorover possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

It contains general information on HC MOS digital integrated circuits and defines the common characteristics for this family of integrated circuits.

Together with the device type detail specification (DS) of a component usually prepared nationally, this family specification forms a complete detail specification.

The text of this specification was circulated to the CECC for voting in the documents indicated below and was ratified by the President of the CECC for printing as a CECC Specification.

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat) 1608	March 1985	CECC(Secretariat) 1725

In accordance with the decision of the CECC Management Committee this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

Specification available from :	CECC 90 109 ISSUE 1 - 1986  Page 2 Total number of pages : 27	
ELECTRONIC COMPONENTS OF ASSESSED QUALITY IN ACCORDANCE WITH : CECC 90 000 : Generic specification for Monolithic integrated circuits (GS) CECC 90 100 : Sectional specification for Digital monolithic integrated circuits (SS)	(National number, date of issue)	
OUTLINE AND DIMENSIONS (See DS for the specific type) TERMINAL CONNECTIONS (See DS for the specific type)	FAMILY SPECIFICATION FOR HC MOS DIGITAL INTEGRATED CIRCUITS 54/74 HC 54/74 HCT 54/74 HCU	
	TYPICAL CONSTRUCTION : Silicon complementary MOS, silicon gate buffered types (HC, HCT) or unbuffered types (HCU), cavity or non-cavity packages (*). (*) A buffered device has 2 or more active logic stages between inputs or outputs. NOTE : HCT is compatible with TTL levels	
	CAUTION : These are electrostatic sensitive devices ASSESSMENT LEVELS : P, Y, L	
CONTENTS 1 - LIMITING CONDITIONS OF USE FOR THE FAMILY 2 - RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS FOR THE FAMILY 3 - INSPECTION REQUIREMENTS		
Information about manufacturers who have components qualified to a detail specification written in accordance with this family specification is available in the current CECC 00 200 : Qualified Products List.		

1 LIMITING CONDITIONS OF USE FOR THE FAMILY
(Not for inspection purposes)

1.1 Maximum supply voltage positive

$$V_{CC} = + 7 \text{ V}$$

1.2 Maximum supply voltage negative

$$V_{CC} = - 0,5 \text{ V}$$

1.3.1 Maximum DC input protection diode current

$$I_{IK} = \pm 20 \text{ mA}$$

$$V_I < 0, V_I > V_{CC}$$

OR (whichever is the worst case)

1.3.2 Maximum input voltage

$$V_I = V_{CC} + 0,5 \text{ V}^*$$

$$V_I = - 0,5 \text{ V}^*$$

NOTE : Except for transient energy (see 2.14.2)

1.4.1 Maximum DC output diode current

$$I_{OK} = \pm 20 \text{ mA}$$

$$V_O < 0, V_O > V_{CC}$$

OR (whichever is the worst case)

1.4.2 Maximum output voltage

$$V_O = V_{CC} + 0,5 \text{ V}^*$$

$$V_O = - 0,5 \text{ V}^*$$

1.5 Maximum DC output source or sink current per output pin I_O

$$\pm 25 \text{ mA (standard outputs)}^*$$

$$\pm 35 \text{ mA (bus driver outputs)}^*$$

1.6 Maximum DC, V_{CC} or Ground pin current I_{CC} or I_{GND}

$$\pm 50 \text{ mA (standard outputs)}^*$$

$$\pm 70 \text{ mA (bus driver outputs)}^*$$

1.7 Ambient operating temperature range T_{amb}

$$74 \text{ HC} : - 40 \text{ }^{\circ}\text{C to } + 85 \text{ }^{\circ}\text{C}$$

$$54 \text{ HC} : - 55 \text{ }^{\circ}\text{C to } + 125 \text{ }^{\circ}\text{C}$$

1.8 Storage temperature range T_{stg}

$$- 65 \text{ }^{\circ}\text{C to } + 150 \text{ }^{\circ}\text{C}$$

* Unless otherwise specified in detail specification.

2 RECOMMENDED OPERATING CONDITIONS AND ASSOCIATED CHARACTERISTICS FOR THE FAMILY
(Not for inspection purposes)

These conditions apply over the operating temperature range, unless otherwise specified in the DS.

All voltages are referenced to ground.

HC SERIES : Operating supply voltages $V_{CCB} = 2 \text{ V}$ to $V_{CCA} = 6 \text{ V}$

PARAMETERS	SYMBOL	V _{CC} (V)	T _{amb}						UNIT
			54/74 HC (1)		74 HC (2)		54 HC (3)		
			min.	max.	min.	max.	min.	max.	
2.1 Quiescent supply current V _I = 0 or V _{CC} I _O = 0 - S.S.I. - FF (Bistable) - MSI	I _{CCA}								
		6		2		20		40	μA
		6		4		40		80	μA
		6		8		80		160	μA
2.2 High level input voltage	V _{IHB}	2 4,5 6	1,5 3,15 4,2		1,5 3,15 4,2		1,5 3,15 4,2		V V V
2.3 Low level input voltage	V _{ILA}	2 4,5 6		0,3 0,9 1,2		0,3 0,9 1,2		0,3 0,9 1,2	V V V
2.4 High level output voltage V _I = V _{IHB} or V _{ILA} 2.4.1 I _O = - 20 μA 2.4.2 I _O = - 4 mA (standard outputs) I _O = - 6 mA (bus driver outputs) I _O = - 5,2 mA (standard outputs) I _O = - 7,8 mA (bus driver outputs)	V _{OHB}	2 4,5 6 4,5 6	1,9 4,4 5,9 3,98 5,48		1,9 4,4 5,9 3,84 5,34		1,9 4,4 5,9 3,7 5,2	V V V V V	
2.5 Low level output voltage V _I = V _{IHB} or V _{ILA} 2.5.1 I _O = + 20 μA 2.5.2 I _O = + 4 mA (standard outputs) I _O = + 6 mA (bus driver outputs) I _O = + 5,2 mA (standard outputs) I _O = + 7,8 mA (bus driver outputs)	V _{OLA}	2 4,5 6 4,5 6		0,1 0,1 0,1 0,26 0,26		0,1 0,1 0,1 0,33 0,33		0,1 0,1 0,1 0,4 0,4	V V V V V
(1) 25 °C									

HC SERIES (continued)

PARAMETERS	SYMBOL	V _{CC} (V)	T _{amb}						UNIT
			54/74 HC (1)		74 HC (2)		54 HC (3)		
			min.	max.	min.	max.	min.	max.	
2.6 Input leakage current V _I = 0 or V _{CC}	I _{I(A)}	6		0,1		1		1	μA
2.7 Analogue switch off-state current per channel V _I = V _{IHB} or V _{I(LA)} V _S = V _{CC} or V _{CC} - V _{EE} (4)	I _{I(SA)}	6		0,1		1		1	μA
2.8 3 state output off-state current V _I = V _{IHB} or V _{I(LA)} V _O = 0 or V _{CC}	I _{O(ZA)}	6		0,5		5		10	μA
2.9 Capacitance 2.9.1 Input capacitance (5) 2.9.2 Output capacitance 3 state outputs (6)	C _{IA} C _{OZ}	4,5		10		10		10	pF
2.10 Noise margin at low level output (V _{I(LA)} - V _{O(LA)}) I _O = + 20 μA	V _{NLB}	2 4,5 6	0,2 0,8 1,1		0,2 0,8 1,1		0,2 0,8 1,1		V V V
2.11 Noise margin at high level output (V _{O(HB)} - V _{I(HB)}) I _O = - 20 μA	V _{NHB}	2 4,5 6	0,4 1,25 1,7		0,4 1,25 1,7		0,4 1,25 1,7		V V V
2.12 Input rise and fall time (except for Schmitt inputs)	t _r , t _f	2 4,5 6	0 0 0	1 000 500 400	0 0 0	1 000 500 400	0 0 0	1 000 500 400	ns ns ns

(1) 25 °C

(2) - 40 °C to + 85 °C

(3) - 55 °C to + 125 °C

(4) V_{EE} : additional negative supply voltage for some analogue switches, to be specified in the DS.

(5) Unless otherwise specified in the DS.

(6) If specified in the DS.