



Specification for Harmonized system of quality assessment for electronic components Blank detail specification

Digital microprocessor integrated circuits

Système harmonisé d'assurance de la qualité des composants électroniques
Spécification particulière cadre

Microprocesseurs logiques à circuits intégrés

Harmonisiertes Gütebestätigungssystem für Bauelemente der Elektronik
Vordruck für Bauartspezifikation

Integrierte Mikroprozessor-schaltungen

Copyright

Users of British Standards are reminded that copyright subsists in all BSI publications. No part of this publication may be reproduced in any form without the prior permission in writing of BSI. This does not preclude the reproduction and free use of the pro forma pages in the course of preparing BS/CECC detail specifications. Enquiries should be addressed to the Publications Manager, British Standards Institution, Linford Wood, Milton Keynes MK14 6LE. (Telephone 0908 320033; Telex 825777).

British Standards Institution

2 Park Street, London W1A 2BS

8705-9-0.25k-B

BS CECC 90110 : 1987

National Foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with CENELEC Electronic Components Committee (CECC) 90110 : 1986 'Harmonized system of quality assessment for electronic components. Blank detail specification : Digital microprocessor integrated circuits'.

This standard is a harmonized specification within the CECC System.

Terminology and conventions. The text of the CECC specification has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards; attenuation is drawn especially to the following.

The comma has been used as a decimal marker. In British Standards it is current practice to use a full point on the baseline as the decimal marker.

Cross-references. The British Standard which implements CECC 00100 is BS 9000: 'General requirements for a system for electronic components of assessed quality Part 2 : 1983 'Specification for national implementation of CECC basic rules and rules of procedure'.

International standards*

IEC 68-2-30 : 1980

CECC 90000 : 1985

CECC 90100 : 1986

Corresponding British Standards

BS 2011 Basic environmental testing procedures
Part 2.1 Db : 1981 of Test Db and guidance.
Damp heat cyclic (12 + 12 hour cycle)
(Identical)

BS CECC 90000 : 1985 Harmonized system
of quality assessment for electronic
components. Generic specification :
monolithic integrated circuits
(Identical)

BS CECC 90100 : 1986 Harmonized system
of quality assessment for electronic
components. Sectional specification :
digital monolithic integrated circuits
(Identical)

The Technical Committee has reviewed the provisions of IEC 747, to which reference is made in the text, and has decided that they are acceptable for use in conjunction with this standard.

Scope. This standard lists the ratings, characteristics and inspection requirements which shall be included as mandatory requirements in accordance with BS CECC 90100 in any detail specification for these devices.

Detail specification layout. The front page layout of detail specifications released to BS CECC family or blank detail specifications will be in accordance with BS 9000 Circular letter No. 15.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

* Undated in text.

Förderverein für Elektrotechnische Normung (FEN) e. V.
Cenelec Electronic Components Committee

CECC

English version

Harmonized System of Quality Assessment for
Electronic Components

**BLANK DETAIL SPECIFICATION:
DIGITAL MICROPROCESSOR
INTEGRATED CIRCUITS**

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

**SPECIFICATION PARTICULIERE CADRE:
MICROPROCESSEURS LOGIQUES
A CIRCUITS INTEGRES**

Harmonisiertes Gütebestätigungssystem für
Baulemente der Elektronik

**VORDRUCK FÜR
BAUARTSPEZIFIKATION:**

**INTEGRIERTE
MIKROPROZESSOR-
SCHALTUNGEN**



1

Issue
Edition
Ausgabe

CECC 90110

FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for DIGITAL MICROPROCESSOR INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom,

PREFACE

This blank detail specification (BDS) was prepared by CECC WG9 "Integrated circuits".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

The text of this BDS was circulated to the CECC for voting in the documents indicated below and was ratified by the President of the CECC for printing as a CECC specification.

<u>Documents</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC (Secretariat) 1335	September 1983	CECC (Secretariat) 1490
CECC (Secretariat) 1556	July 1984	CECC (Secretariat) 1677

It is recognized that the layout proposed cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

In accordance with the decision of the CECC Management Committee this specification is published initially in English and French. The German text will follow as soon as it has been prepared.

GENERAL

The following information is given for guidance.

Scope

This BDS relates to digital microprocessors in accordance with IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

Related documents

See 2.1 of CECC 90 100 and 2.2 of CECC 90 000

Structure of Detail Specifications

Clause numbering of DS shall be in accordance with that of this document.

Units, symbols and terminology

See 2.3 of CECC 90 100 and 2.3 of CECC 90 000

Application of Quality Assessment Procedures

See 3 of CECC 90 100 and CECC 90 000.

FRONT PAGE

The front page of the DS shall be laid out as shown on page 3.

The numbers between square brackets correspond to the following indications which shall be given :

- Identification of the DS and of the component :

- [1] The name of the National Standards Organization under whose authority the DS is published and, if applicable, the organization from whom the DS is available.
- [2] The CECC Symbol and the CECC number allotted to the DS by the CECC General Secretariat.
- [3] The number and issue number of the CECC generic or sectional specification as relevant ; also national reference if different.
- [4] If different from the CECC number, the national number of the DS, date of issue and any further information required by the national system, together with any amendment numbers.
- [5] Type number, a short description of the type by :
 - function
 - performance, for example variants based on speed, temperature, power etc.

[6] Information on typical construction

- material and type of construction (silicon, monolithic, bipolar, MOS)

For [5] and [6] the text to be given in the DS should be suitable for an entry in CECC 00 200 (QPL) and CECC 00 300 (Library List).

- [7] An outline drawing with main dimensions which are of importance for interchangeability, and/or reference to the appropriate national or international document for outlines. Alternatively, this drawing may be given in an annex to the DS.

[8] Quality assessment level(s)

- [9] Reference data giving information on the most important properties of the component, which allow comparison between the various component types intended for the same, or for similar, applications.

The DS shall give a brief description including the following :

- Technology
- Use (if applicable)
- Number, type and length of registers
- Number, type and width of buses
- Word length
- Addressable memory
- Number of terminals
- Supply voltage
- Any other special feature

- Identification of the component and supplementary information :

Description of the materials for the package (for example, glass, ceramic, metal, plastic) and information relating to the mounting (welding, soldering), lead material and finish.

Inside the sketch of the package, the terminal connections to the inputs, outputs or other important points of the circuit shall be identified. This can be shown by a functional block diagram.

Description of the numbering of the terminals with the identification of pin number 1.

Marking on the device in accordance with the GS (see 2.5 of CECC 90 000).

2 OPERATING CHARACTERISTICS

The following characteristics shall apply over the full operating temperature range and the supply voltage range unless otherwise specified.

2.1 General description

The following characteristics shall be given if they are not adequately defined in clause 1.

2.1.1 Internal architecture

Simplified block diagram, with explanatory comments.

2.1.2 Hardware description

- The main features relating to system design and operation shall be given.
- Clock requirements.

2.1.3 Memory organization

Total number of words and total number of bits of the word addressed in each type of memory.

This may be given in the form of a diagram (memory map).

2.1.4 Software main features

2.1.4.1 Addressing modes

List of addressing modes.

2.1.4.2 Arithmetic and logic operations, operations on registers

Number of bits involved in the operation.

2.1.5 Designation of the terminals

The terminals shall be designated in a table as follows :

Symbol	Function	Category

The following categories of terminals apply :

- Supply terminals
- Input terminals/output terminals
- Input/output terminals (bidirectional terminals)
- Three state output terminals

2.2 External components

Characteristics of external components essential to the correct operation of the microprocessor shall be specified (for example clock circuitry)

2.3 Detailed functional specifications

2.3.1 Power supply and initialisation sequences

- power supplies sequencing
- microprocessor initialisation procedure

2.3.2 Block diagram

A block diagram for the microprocessor integrated circuit shall be given. It shall be sufficiently detailed to enable the individual functional units within the microprocessor that are affected by the execution of the instructions to be identified, including any functional blocks that are user programmable. The main data paths between the functional units, and the identification of their external connections shall be shown.

2.3.3 Input and output detailed functions and signals

The function of each input and output signal shall be stated.

The signals may be presented in the following groups :

- DATA signals
- ADDRESS signals
- CONTROL signals (including STATUS).

If necessary explanatory diagrams should be given.

2.3.4 Description of registers

A detailed description including number, types and sizes in bits, of internal register(s) program addressable, or otherwise directly affecting the operation of the microprocessor shall be given.

A schematic representation shall also be given for example as follows :

bit n	bit 0	
-----		General purpose register(s)
-----		Index and stack pointer register(s)
-----		Program counter(s) and flag register(s)
-----		Specific register(s)

2.3.5 Addressing mode(s)

The different possible addressing modes (for example immediate, direct, relative, indexed and indirect) shall be described in detail. Each description shall include a schematic representation of the mechanism of the addressing mode. For more complex modes a table may be necessary.