
British Standard

**Harmonized system of quality
assessment for electronic components:
Sectional specification: Analogue
monolithic integrated circuits**

Système harmonisé d'assurance de la qualité des composants électroniques
Spécification intermédiaire: Circuits intégrés monolithiques analogiques

Harmonisiertes Gütebestätigungssystem für Bauelemente der Elektronik
Rahmenspezifikation: Analoge monolithische integrierte Schaltungen

National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Committee. It is identical with CENELEC Electronic Components Committee (CECC) 90200 : 1987 'Harmonized system of quality assessment for electronic components : Sectional specification : Analogue monolithic integrated circuits'. It supersedes BS CECC 90200 : 1983, which is withdrawn. It should be noted that the withdrawal of BS CECC 90200 : 1983 does not affect the validity of approvals which make reference to that standard.

This standard gives the terminology, quality assessment procedure, test and measurement procedure applicable to the sub-family of analogue monolithic integrated circuits. It also includes the common blank detail specification for analogue monolithic integrated circuits.

This standard is a harmonized specification within the CECC system and should be read in conjunction with BS CECC 90000.

This standard specifies the use of substances and/or test procedures that may be injurious to health if adequate precautions are not taken. It refers only to technical suitability and in no way absolves either the supplier or the user from statutory obligations relating to health and safety at any stage of manufacture or use.

The BSI prescribed layout for a harmonized detail specification will in due course be incorporated in the revised BS 9000 : Part 1 : 1981, by amendment.

This second issue of BS CECC 90200 results from amendments and additions which have been agreed since the first issue was published in 1983.

Terminology and conventions. The text of the CECC specification has been approved as suitable for publication as a British Standard without deviation. Some terminology and certain conventions are not identical with those used in British Standards; attention is drawn especially to the following.

The comma has been used as a decimal marker. In British Standards it is current practice to use a full point on the baseline as the decimal marker.

Cross-references

International standard	Corresponding British Standard
IEC 68-2-30 : 1980	BS 2011 Basic environmental testing procedures Part 2.1Db : 1981 Test Db and guidance: Damp heat, cyclic (12 + 12 hour cycle) (Identical)
IEC 148 : 1969	BS 3363 : 1980 Specification for letter symbols for semiconductor devices and integrated microcircuits (Identical)
IEC 617-13 : 1978	BS 3939 Guide for graphical symbols for electrical power, telecommunications and electronics diagrams Part 13 : 1985 Analogue elements (Identical)
IEC 747-1 : 1983	BS 6493 Semiconductor devices: discrete devices and integrated circuits Part 1 Discrete devices Section 1.1 : 1984 General (Identical)
IEC 747-10 : 1984	BS 9970 Harmonized system of quality assessment for electronic components: Semiconductor devices Part 0 : 1985 Generic specification (Identical)
IEC 748-1 : 1984	BS 6493 Semiconductor devices : discrete devices and integrated circuits Part 2 Integrated circuits Section 2.1 : 1985 General (Identical)
IEC 748-3 : 1986	BS 6493 Semiconductor devices Part 2 Integrated circuits Section 2.3 : 1987 Recommendations for analogue integrated circuits (Identical)
CECC 90000 : 1985	BS CECC 90000: 1985 Harmonized system of quality assessment for electronic components Generic specification : Monolithic integrated circuits (Identical)
CECC 90100 : 1986	BS CECC 90100 : 1986 Harmonized system of quality assessment for electronic components Sectional specification : Digital monolithic integrated circuits (Identical)

Amendment No.1
published and effective from 15 August 1994
to BS CECC 90200 : 1988

Harmonized system of quality assessment for
electronic components Sectional specification:
Analogue monolithic integrated circuits

NOTE. This amendment implements Amendment No.1 to CECC 90200, Issue 2 (1987). The national foreword has been amended accordingly.

Revised text

National foreword

In line 3, after the title of CECC 90200, insert 'as amended by Amendment No.1 published in 1994'.

AMD 8292/August 1994

Instructions for amendment and insertion of new and revised pages

Delete pages 1/2 and substitute revised pages 1/2.

AMD 8292/August 1994

Clause 1. Scope

Delete line 4 entirely, i.e. - structural similarity procedures.

AMD 8292/August 1994

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Clause 3.1. Structurally similar circuits

Retain the title of the clause but delete the text of the clause entirely.

AMD 8292/August 1994

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Delete pages 13/14 and insert new pages 13/14.

AMD 8292/August 1994

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Delete pages 17/18 and insert new pages 17/18.

AMD 8292/August 1994

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Delete pages 19 to 26 entirely.

AMD 8292/August 1994

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- B L A N K P A G E -

(2) Additional methods

The following methods shall be used, pending publication of IEC methods.

Method Reference number	Parameter		Annex A
	Designation	Symbol	Clause n°
S-01	Verification of the function		A4.1
S-02	ON-STATE Resistance	$R_{(ON)}$	A4.2
S-03	SWITCH-OFF Isolation	$a_{(OFF)}$	A4.3
S-04	Harmonic distortion of analogue signal	D	A4.4
S-05	Crosstalk attenuation between any two channels	a_{ct}	A4.5
S-06	Feedthrough between control input and any analogue output	ΔV_O	A4.6
S-07	Dynamic characteristics . TURN-ON time . TURN-OFF time . transition time . propagation time	$t_{(ON)}$ $t_{(OFF)}$ t_T t_P	A4.7
S-08	MAKE-BEFORE-BREAK and BREAK-BEFORE-MAKE switching times	t_{MBB} t_{BBM}	A4.8

4.2 Electrical endurance testing

See GS/4.8.

5 COMMON BLANK DETAIL SPECIFICATION FOR ANALOGUE MONOLITHIC INTEGRATED CIRCUITS

5.1 Introduction

The blank detail specification given in this section describes the requirements for technical content and format of DS for devices intended to be CECC approved, except that, in particular conditions described below, the requirements are included in, and may be modified by, a particular BDS or Family DS which shall be published separately.

5.3 Identification of the component and supplementary information

5.3.1 Detail drawing with dimensions with reference to IEC or National Standards

5.3.2 Description of the materials for the package (for example, glass, ceramic, silicone) and information relating to the mounting (welding, soldering), lead material and finish.

5.3.3 Inside the sketch of the package, the terminal connections to be inputs, outputs or other important points of the circuit shall be identified. This can be shown by a functional block diagram.

5.3.4 Description of the numbering of the terminals with the identification of pin number 1.

5.3.5 Marking on the device in accordance with the GS (see 2.5 of CECC 90 000).

5.3.6 Function

A schematic circuit may be given.

5.4 Ratings (limiting values) -(not for inspection purposes)

Values of the limiting conditions of use shall be given as follows :

- the limiting values of positive and/or negative voltages at each terminal referred to a common terminal and any other interterminal voltages as appropriate, unless implied by limiting values of currents. Any instructions on the switching sequence of supply voltages, as appropriate, shall be prescribed ;
- the limiting values of positive and negative currents into each terminal, unless implied by limiting values of voltages. If these voltages and currents may be exceeded for transient overload the permissible excesses and their durations shall be specified ;
- the limiting ambient and/or case operating temperatures (min. and max.) ;
- the limiting storage temperatures (min. and max.) ;
- any limiting mechanical or environmental conditions. The conditions under which they apply shall be specified ;
- any interdependence of limiting conditions shall be specified ;
- if externally connected elements have an influence on the values of the ratings, the ratings shall be prescribed for the integrated circuit with the elements connected ;
- any cautionary statement peculiar to a particular integrated circuit, shall be included, for example the handling of MOS circuits ;
- power dissipation, maximum and where appropriate, typical value, reference to a power derating curve with temperature, where appropriate.

5.5 Recommended conditions of use and associated characteristics (not for inspection purposes)

The recommended conditions of use and associated characteristics shall apply over the full ambient operating temperature range unless otherwise specified. Where the specified performance of the circuit varies over the ambient operating temperature range, the values of the input and output voltages and their associated currents shall be prescribed at 25 °C and at the extremes of the operating temperature ranges. Values of current and voltage shall be prescribed for each functionally different type of input and/or output. Timing information shall be prescribed for all inputs or combinations as necessary for the declared application.

Where correct operation is obtained or operation is modified by connection of external elements, the ranges of values of these elements shall be prescribed. Where appropriate, the recommended conditions of use and associated characteristics shall be prescribed with these elements connected.

Current and voltage values may be either positive or negative depending on the type of circuit.

The applicable recommended conditions of use and associated characteristics shall be given in the relevant BDS. Those characteristics which are indicated as "where appropriate" are applicable to specific device types. Additionally, other characteristics may be required to specify the circuits fully.

5.6 Supplementary information

The following additional information shall be specified as minimum design data:

- diagram(s) showing basic features of operation of the circuit;
- basic element circuit diagram(s) or, where applicable, a statement of technology, information regarding input and output circuits;
- variation of propagation or other critical times with temperature, where appropriate;
- additional frequency dependant characteristics, where appropriate;
- curves or data indicating the effect of externally connected components which are required for normal operation.

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FOREWORD

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This specification has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue national harmonized specifications for ANALOGUE MONOLITHIC INTEGRATED CIRCUITS. It should be read in conjunction with the current regulations for the CECC System.

At the date of printing of this specification the member countries of the CECC are Austria, Belgium, Denmark, Finland, France, Germany, Ireland, Italy, the Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.

PREFACE

This sectional specification (SS) was prepared by CECC WG 9 "Integrated circuits".

It is based, wherever possible, on the Publications of the International Electrotechnical Commission and in particular on IEC 747 : Semiconductor devices : Discrete devices and integrated circuits, IEC 748 : Semiconductor devices : Integrated circuits, IEC 749 : Semiconductor devices : Mechanical and climatic test methods.

The text of this second Issue consists of the text of CECC 90 200 Issue 1 (1983) and Amendment 1 (1985) amended in accordance with the ratified new material introduced by the following document.

<u>Document</u>	<u>Date of Voting</u>	<u>Report on the Voting</u>
CECC(Secretariat) 1947	September 1986	CECC(Secretariat) 2008

In accordance with the decision of the CECC Management Committee this specification is published initially in French and English. The German text will follow as soon as it has been prepared.

EFFECTIVE DATE

This second Issue shall become effective for all new qualification approvals from 1 July 1987.

Issue 1 will remain valid for existing qualification approvals until further notice, but it is recommended that current qualifications should be modified in accordance with Issue 2 during a transition period of 2 years.

1 SCOPE

This specification applies to analogue monolithic integrated circuits listed in section 4 and shall be read in conjunction with CECC 90 000.

It defines :

- structural similarity procedures
- electrical measurement methods
- electrical endurance tests.

The common blank detail specification (BDS), contained in this SS, comprises those requirements which are common for all analogue circuits.

2 GENERAL

2.1 Related documents

In each case the latest issue of the documents prior to the date of issue of this document is valid.

IEC 148 : Letter symbols for semiconductor devices and integrated microcircuits. (Chapter XI).

IEC 617 : Graphical symbols for diagrams.

IEC 617-13 : Part 13 : Analogue elements.

IEC 747 : Semiconductor devices - Discrete devices and integrated circuits.

IEC 747-1 : Part 1 : General.

IEC 747-10 : Part 10 : Generic specification for discrete devices and integrated circuits.

IEC 748 : Semiconductor devices - Integrated circuits.

IEC 748-1 : Part 1 : General.

IEC 748-3 : Part 3 : Analogue integrated circuits.

CECC 90 000 : GS : Monolithic integrated circuits.

2.2 Preferred voltages for analogue monolithic integrated circuits.

Preferred values are given in IEC 748-1 Chapter IV, sub-clause 6.1.b.

2.3 Symbols and terminology.

2.3.1 Letter symbols

The letter symbols shall be used in accordance with IEC 148, Chapter XI.

To indicate a defined value of an electrical quantity denoted by a basic letter, the following system shall be used :

- A for the most positive (least negative) value of the range.
- B for the least positive (most negative) value of the range.

Examples (see Fig. 1).

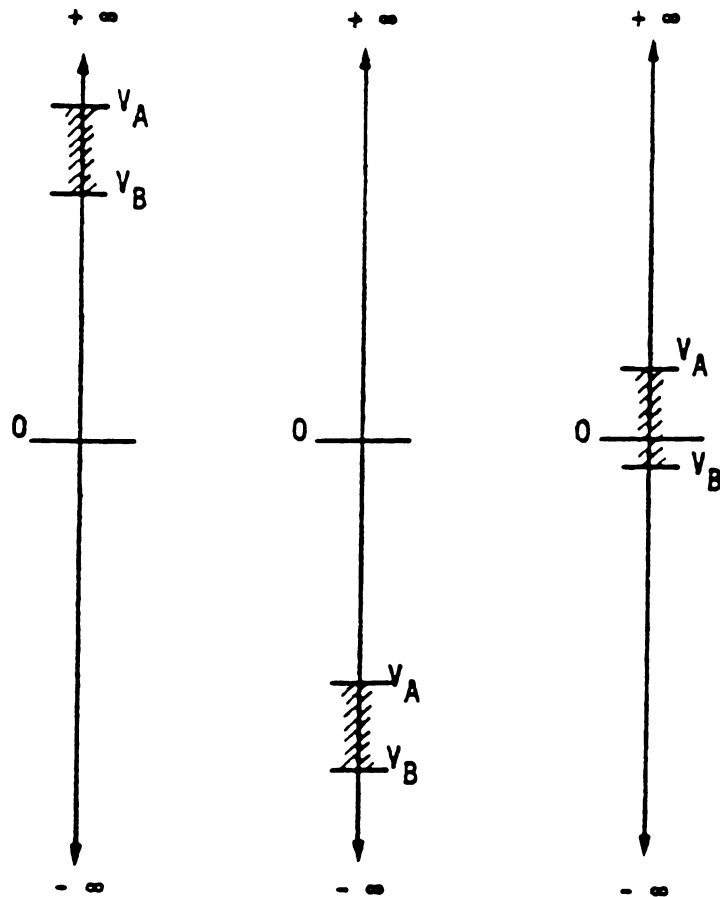


Fig. 1

2.3.2 Graphical symbols

Graphical symbols shall be used in accordance with IEC 617-13.

2.3.3 Terminology

For terminology, IEC 748-1 shall be used, and in particular Chapter IV.

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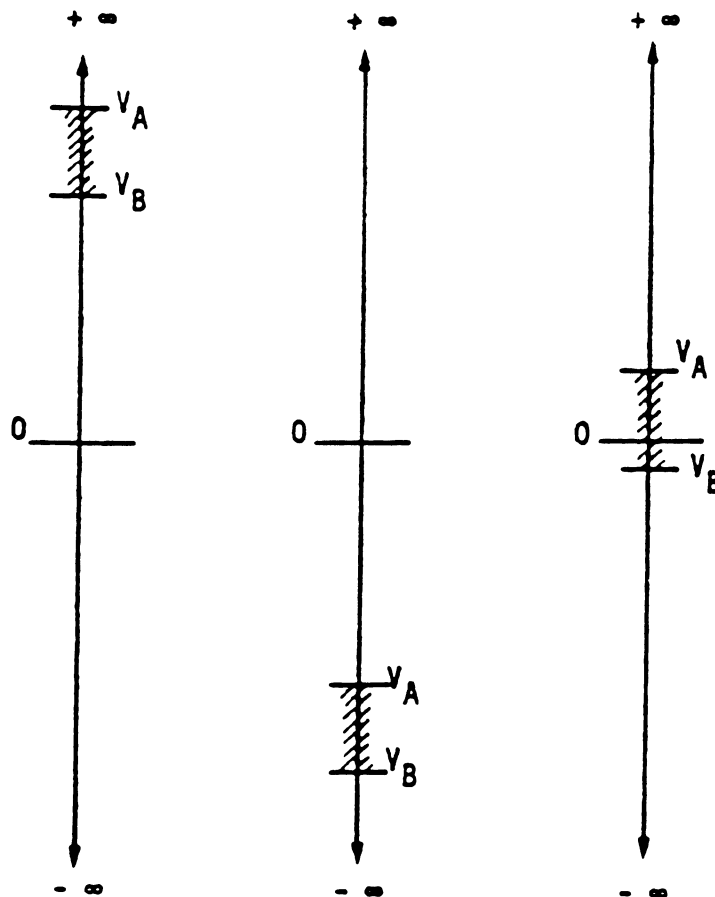


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3 QUALITY ASSESSMENT PROCEDURES

3.1 Structurally similar circuits (see 3.2 of CECC 90 000)

The grouping of types due to structural similarity is as follows :

3.1.1 For testing of Sub-Groups :

- B1 - dimensions
- B2 - solderability
- C1 - dimensions not included in B1
- C2 - immersion in cleaning solvents
- C3 - robustness of terminations
- C13 - salt mist

The devices are structurally similar provided that they have identical packages, and that they come from the same assembly and encapsulation line using the same assembly techniques and piece parts.

3.1.2 For testing of Sub-Groups :

- B3 - sealing test
- B4 - change of temperature
- C4 - resistance to soldering heat followed by change of temperature
- C5 - shock, vibration, acceleration
- C6, C7 - damp heat, steady state

The devices are structurally similar provided that they have identical packages, and that they come from the same assembly and encapsulation line using the same assembly techniques and piece parts and that the maximum ratio in chip area should not exceed 2.

3.1.3 For testing of Sub-Groups :

- B5 - electrical endurance (168 h)
- C8 - electrical endurance (1 000 h)

The devices are structurally similar even if the chip lay-out differs, provided that all the following criteria are satisfied :

- they operate at the same recommended operating voltage(s) applied to equivalent terminal(s) including "open-terminal" (for example open collector or drain) devices and a power dissipation within a 20 % range ;
- they have been designed to the same design rules ;
- they have been manufactured on the same production line including identical packages, using the same technical processes starting from the primary stage ;
- the devices with the highest power dissipation and recommended operating temperature shall be chosen.

3.1.4 For testing of Sub-Groups :

C9 - storage, dry heat
C10 - storage, cold

The devices are structurally similar provided that all the following criteria are satisfied :

- they have been designed to the same design rules ;
- they have been manufactured on the same production line including identical packages, using the same technical processes starting from the primary stage.

3.1.5 For testing of Sub-Group D1 - electrical endurance (8 000 h)

Integrated circuits produced concurrently in the same production line up to and including final sealing in their encapsulations using the same types of machines and apparatus and using the same integrated circuit design rules may be grouped together for the purpose of obtaining samples. The claim for grouping shall be declared in the qualification approval test report to the satisfaction of the ONS.

Integrated circuits may be grouped together for the purpose of obtaining samples for electrical endurance tests under the same or similar test conditions, provided that the same basic design rules (for example, element geometry, spacing, thickness of the chip, etc.) and internal sub-circuits (for example, multi-emitter input, phase splitter, totem pole output, etc.) are used.

When the above conditions apply, manufacturers may take a single sample of any one type to assess the lot if it can be demonstrated to the satisfaction of the ONS that the characteristic(s) being tested are not significantly dependent upon the selection. If there is a significant difference, the type selected for the common electrical endurance tests shall be represented by the more complex circuit or that with a critical rating giving the greatest risk of failure.

3.2 Certified test records

Certified test records shall give the following information, unless otherwise specified :

- attributes information for tests in Sub-Groups : B2, B3, B4, B5, C3, C4, C5, C6, C7, C8, C9, C10 ;
- measurement information before and after endurance test : C8 and D1.

4 TEST AND MEASUREMENT PROCEDURES

4.1 Electrical measurement procedures (see 4.1 and 4.5 of CECC 90 000)

4.1.1 Measuring methods for linear amplifiers (including operational amplifiers)

(1) IEC methods :

The hereafter listed electrical measuring methods, with reference to the relevant IEC documents, shall be used when required by the relevant DS and as prescribed in this document :

Method Reference number	Parameters Designation	Symbol	IEC 748-3	
			Chapter IV Clause n°	Section 2 Method n°
A-01	Power supply currents	I_S	2	22
A-02	Small signal input impedance	Z_i	3	23
A-03	Output impedance	Z_o	4	24
A-04	Input offset voltage of a differential input integrated linear amplifier <u>and</u>	V_{IO}	5	25, 26
	Bias voltage of a single-ended input integrated linear amplifier	V_{IB}		
A-05	Input offset current	I_{IO}	6	27
A-06	Input bias current	I_{IB}	7	28
A-07	Input offset voltage temperature coefficient	α_{VIO}	8	29
A-08	Input offset current temperature coefficient	α_{IIO}	9	30
A-09	Open-loop voltage amplification	A_V	10	31
A-10	Cut-off frequency (frequencies)	f_a, f_b	11	32
A-11	Common mode rejection ratio	k_{CMR}	12	33
A-12	Supply voltage rejection ratio	k_{SVR}	13	34
A-13	Output voltage range for differential amplifiers (d.c. measurement only)	V_{OPP}	14	35
A-14	Response times		15	39
	delay time	t_d		
	rise time	t_r		
	fall time	t_f		
	ripple time	t_{rip}		
	total response time	t_{tot}		