

Specification for

Harmonized system of quality assessment for electronic components — Blank detail specification —

Single gate field-effect transistors

The European Standard EN 150012:1991 has the status of a
British Standard

Amendments issued since publication

Amd. No.	Date of issue	Comments
7593	February 1993	Indicated by a sideline in the margin

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Contents

	Page
National foreword	ii
Foreword	iii
Text of CECC 50012	1

National foreword

This British Standard has been prepared under the direction of the Electronic Components Standard Committee. It is identical with CENELEC Electronic Components Committee (CECC) CECC 50012 “*Harmonized system of quality assessment for electronic components. Blank detail specification: Single gate field-effect transistors*”.

This standard is a harmonized specification within the CECC system.

In 1991 the CENELEC Electronics Components Committee (CECC) accepted CECC 50012:1980 as European Standard EN 150012:1991.

It is recognized that the layout proposed herein cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

Terminology and conventions. The text of the CECC specification has been approved as suitable for publication, without deviation, as a British Standard. Some terminology and certain conventions are not identical with those used in British Standards; attention is especially drawn to the following.

The comma has been used throughout as a decimal marker. In British Standards it is current practice to use a full point on the baseline as the decimal marker.

Cross-references. The British Standard harmonized with CECC 00100 is BS 9000 “*General requirements for electronic components of assessed quality*”.

The following International Standards are referred to in the text and for each there is a corresponding British Standard; these are as listed below:

International Standard	Corresponding British Standard
IEC 191-2	BS 3934 <i>Dimensions of semiconductor devices</i> (Technically equivalent)
CECC 50000	BS CECC 50000 <i>Harmonized system of quality assessment for electronic components: Generic specification: Discrete semiconductor devices</i> (Identical)

Scope

This standard lists the ratings, characteristics and inspection requirements which shall be included as mandatory requirements in accordance with BS CECC 50000 in any detail specification for these devices.

Detail specification layout

In the event of conflict between the requirements of this specification and the provisions of section 3 of BS 9000-2 the latter shall take precedence except the front page layout shall be in accordance with BS 9000 Circular letter no. 15 dated August 1977.

A British Standard does not purport to include all the necessary provisions of a contract. Users of British Standards are responsible for their correct application.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, page 2, the CECC title page, pages ii to iv, pages 1 to 58 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

UDC:

Descriptors: Quality, electronic components, transistors

English version

Blank Detail Specification: Single gate field-effect transistors

Spécification Particulière Cadre:
Transistors à effet du champ à grille unique

Vordruck für Bauartspezifikation:
Feldeffekt-Transistoren mit einer
Gate-Elektrode

This European Standard was approved by the CENELEC Electronic Components Committee (CECC) on 25 November 1991. The text of this standard consists of the text of CECC 50012 Issue 2 1980 of the corresponding CECC Specification. CENELEC members are bound to comply with CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the General Secretariat of the CECC or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CECC General Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and United Kingdom. The membership of the CECC is identical, with the exception of the national electrotechnical committees of Greece, Iceland and Luxembourg.

CECC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

English version

Harmonized System of Quality Assessment for
Electronic Components

BLANK DETAIL SPECIFICATION:
**SINGLE GATE FIELD-EFFECT
TRANSISTORS**

Système Harmonisé d'Assurance de la Qualité
des Composants Electroniques

SPECIFICATION PARTICULIERE CADRE:
**TRANSISTORS A EFFET DE
CHAMP A GRILLE UNIQUE**

Harmonisiertes Gütebestätigungssystem für
Bauelemente der Elektronik

VORDRUCK FÜR
BAUARTSPEZIFIKATION:
**FELDEFFEKT-
TRANSISTOREN MIT EINER
GATE-ELEKTRODE**



CECC 50012

1977

Contents

	Page
Foreword	iii
Section 1. Low frequency amplification	
1 Mechanical description	2
2 Electrical application	2
3 Levels of quality assessment	2
4 Limiting values	2
5 Characteristics	3
6 Test conditions and inspection requirements	4
Section 2. High frequency amplification	
1 Mechanical description	12
2 Electrical application	12
3 Levels of quality assessment	12
4 Limiting values	12
5 Characteristics	13
6 Test conditions and inspection requirements	14
Section 3. Switching applications	
1 Mechanical description	22
2 Electrical application	22
3 Levels of quality assessment	22
4 Limiting values	22
5 Characteristics	23
6 Test conditions and inspection requirements	24
Section 4. Chopper applications	
1 Mechanical description	32
2 Electrical application	32
3 Levels of quality assessment	32
4 Limiting values	32
5 Characteristics	33
6 Test conditions and inspection requirements	34
Section 5. Voltage-controlled resistor (VCR) applications	
1 Mechanical description	41
2 Electrical application	41
3 Levels of quality assessment	41
4 Limiting values	41
5 Characteristics	42
6 Test conditions and inspection requirements	43
Section 6. Low level d.c. amplifier applications	
1 Mechanical description	50
2 Electrical application	50
3 Levels of quality assessment	50
4 Limiting values	50
5 Characteristics	51
6 Test conditions and inspection requirements	52

Foreword

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby accepted by all member countries without further testing.

This document has been formally approved by the CECC, and has been prepared for those countries taking part in the System who wish to issue detail specifications for FIELD-EFFECT TRANSISTORS. It should be read in conjunction with document CECC 00100: Basic Rules (1974).

At the date of printing of this document the member countries of the CECC are Belgium, Denmark, France, Germany, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom. Copies of this document can be obtained from the National Committees of the CENELEC in these countries.

Preface

This blank detail specification was prepared by CECC Working Group 5: "Semiconductor diodes and transistors".

It is one of a series of blank detail specifications for discrete semiconductor devices, all relating to the generic specification printed as CECC 50000.

The text of this specification was circulated to the CECC for voting in documents CECC (Secretariat) 463 and 584 in December 1975 and February 1977 respectively, and was ratified by the CECC for printing as a CECC Specification.

It is recognized that the layout proposed cannot be applied to all detail specifications based on this document. For instance, it may be preferable to indicate the limiting values in the form of a table when several similar devices appear in the same detail specification.

Contents

This blank detail specification is divided according to uses in a number of sections, as indicated hereafter. Each section is complete in itself in that all common parts have been repeated (e.g. limiting values).

<u>Section 1.</u>	Low frequency amplification	page 1
<u>Section 2.</u>	High frequency amplification	page 11
<u>Section 3.</u>	Switching	page 21
<u>Section 4.</u>	Chopper	page 31
<u>Section 5.</u>	Voltage-controlled resistor	page 40
<u>Section 6.</u>	Low level d. c. amplification	page 49

Section 1. Low frequency amplification

Numbers between square brackets on the next page correspond to the following indications which should be given:

Identification of the detail specification

- [1] The name of National Standards Organization under whose authority the detail specification is drafted
- [2] The CECC Symbol and the number allotted by the CECC General Secretariat to the completed detail specification
- [3] The number and issue number of the national generic and sectional specifications
- [4] The national number of the detail specification, date of issue and any further information required by the national system.

Identification of the component

- [5] A short description of the type of component
- [6] Information on typical construction (where applicable)
- [7] Outline drawing and/or reference to the relevant document for outlines
- [8] Application or group of applications covered (see note below)
- [9] Reference data on the most important properties, to allow comparison between the various component types.

NOTE When a device is so designed that it can satisfy several applications, this should be stated in the detail specification, in which case the characteristic and inspection requirements relevant to these applications should be met simultaneously (these may appear in different columns of a blank detail specification or in different blank detail specifications, as the case may be).

[1]	page: of:	CECC 50012 Section 1 LF AMPLIFICATION	[2]																																																							
ELECTRONIC COMPONENT OF ASSESSED QUALITY IN ACCORDANCE WITH:																																																										
[3]				[4]																																																						
DETAIL SPECIFICATION FOR: SINGLE GATE FIELD-EFFECT TRANSISTOR (S) TYPE-NUMBER (S): <u>CONSTRUCTION:</u> Polarity: N-channel/P-channel Device categories : Type A: junction-gate-type Type B: insulated-gate depletion type Type C: insulated-gate enhancement type Case material : glass/metal/plastic/other																																																										
1 Mechanical description Outline references (code A) from IEC 191-2: National: OR Base and case references (codes B + C) from IEC 191-2: National: AND/OR Outline drawing TERMINAL CONNECTIONS: including any connections between terminals, case and substrate, if necessary MARKING: letters and figures or colour code		2 Electrical application power : AMBIENT-RATED frequency : LOW use : AMPLIFICATION 3 Levels of quality assessment F – L																																																								
4 Limiting values (absolute maximum system) <u>COMMON TO ALL APPLICATIONS</u>																																																										
These apply over the operating temperature range, unless otherwise stated																																																										
<table border="1"> <thead> <tr> <th colspan="3"></th> <th colspan="3">Types</th> </tr> <tr> <th colspan="3"></th> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>4.1</td> <td>Minimum and maximum ambient operating temperatures</td> <td>T_{amb} max min</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>4.2</td> <td>Minimum and maximum storage temperatures</td> <td>T_{stg} max min</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>4.3</td> <td>Maximum drain-source voltage under specified conditions</td> <td> V_{DSX} } (or V_{DSS} } max (or V_{DSR} } </td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>4.4</td> <td>Maximum gate-source voltage (with $V_{DS} = 0$), reverse and, where appropriate, forward</td> <td> V_{GSR} max V_{GSF} max </td> <td>x</td> <td>x (x)</td> <td>x (x)</td> </tr> <tr> <td>4.5</td> <td>Maximum gate-drain voltage with source open-circuited</td> <td>V_{GDO} max</td> <td>x</td> <td>x</td> <td>x</td> </tr> <tr> <td>4.6</td> <td>Maximum forward gate current</td> <td>I_{GF} max</td> <td>x</td> <td>—</td> <td>—</td> </tr> <tr> <td>4.7</td> <td>Maximum drain current</td> <td>I_D max</td> <td>x</td> <td>x</td> <td>x</td> </tr> </tbody> </table>								Types						A	B	C	4.1	Minimum and maximum ambient operating temperatures	T_{amb} max min	x	x	x	4.2	Minimum and maximum storage temperatures	T_{stg} max min	x	x	x	4.3	Maximum drain-source voltage under specified conditions	V_{DSX} } (or V_{DSS} } max (or V_{DSR} }	x	x	x	4.4	Maximum gate-source voltage (with $V_{DS} = 0$), reverse and, where appropriate, forward	V_{GSR} max V_{GSF} max	x	x (x)	x (x)	4.5	Maximum gate-drain voltage with source open-circuited	V_{GDO} max	x	x	x	4.6	Maximum forward gate current	I_{GF} max	x	—	—	4.7	Maximum drain current	I_D max	x	x	x
			Types																																																							
			A	B	C																																																					
4.1	Minimum and maximum ambient operating temperatures	T_{amb} max min	x	x	x																																																					
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4.6	Maximum forward gate current	I_{GF} max	x	—	—																																																					
4.7	Maximum drain current	I_D max	x	x	x																																																					
See the relevant Qualified Products List for the availability of components qualified under this detail specification.																																																										

				Types		
				A	B	C
4.8	Power dissipation: Special requirements for ventilation/mounting should be specified					
4.8.1	Maximum total power dissipation as a function of temperature or:	$P_{\text{tot max}}$	vs T	x	x	x
4.8.2	Maximum virtual (equivalent) junction temperature and absolute limit of power dissipation	$T_{(V_j)}$ P_{tot}	} max	x x	x x	x x
4.9	For insulated-gate devices with separate source and substrate terminals: (In general devices that include gate-protection diodes do not require this to be specified)					
4.9.1	Maximum gate-substrate voltage under specified conditions	$V_{\text{GB}}(V_{\text{GU}})$	max	—	x	x
4.9.2	Maximum drain-substrate voltage under specified conditions	$V_{\text{DB}}(V_{\text{DU}})$	max	—	x	x
4.9.3	Maximum source-substrate voltage under specified conditions	$V_{\text{SB}}(V_{\text{SU}})$	max	—	x	x

5 Characteristics (See 6 for inspection)

The characteristics marked x shall be given at $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ unless otherwise stated.

Sign + indicates characteristic is verified under the inspection requirements.

Signs between brackets correspond to characteristics indicated “where appropriate”, or given as alternatives.

				Types		
				A	B	C
5.1	Leakage or cut-off currents:					
	Either: maximum leakage or cut-off current with source open-circuited, preferably at maximum rated gate-drain voltage V_{GDO}	I_{GDO} (1)		(x)	(x)	(x)
	or: maximum leakage or cut-off current with drain short-circuited to source, preferably at maximum rated gate-source voltage V_{GSR}	I_{GSS} (1)		(x)	(x)	(x)
	or: maximum gate-source leakage or cut-off current, at specified V_{DS} and specified V_{GS} or I_{D}	I_{GS}		(x)	(x)	(x)
5.2	Leakage or cut-off currents at high temperature:					
	Either: maximum leakage or cut-off current with source open-circuited, at V_{GD} preferably between 65 % and 85 % of maximum rated V_{GDO} and at a high temperature (see 4.3.3 of CECC 50000)	I_{GDO} (2)		(x)	(x)	(x)
	or: maximum leakage or cut-off current with drain short-circuited to source, at V_{GS} preferably between 65 % and 85 % of maximum rated V_{GSR} and at a high temperature (see 4.3.3 of CECC 50000)	I_{GSS} (2)		(x)	(x)	(x)
5.3	Minimum and maximum gate-source cut-off voltage at specified V_{DS} and I_{D} (preferably $\leq 1\text{ }\mu\text{A}$)	V_{GSoff}		x	x	—

				Types		
				A	B	C
+	5.4	Minimum and maximum drain current at $V_{GS} = 0$ and specified V_{DS} (d.c. or pulse as specified)	I_{DSS}	x	x	—
+	5.5	Minimum and maximum gate-source threshold voltage at specified V_{DS} and I_D	$V_{GS(TO)}$	—	—	x
+	5.6	Minimum and maximum drain current at specified V_{GS} and V_{DS}	I_D	—	—	x
+	5.7	Maximum short-circuit input capacitance at 1MHz, specified V_{DS} and specified V_{GS}	C_{11ss}	x	x	x
(+)	5.8	Where appropriate: Maximum short-circuit output conductance at specified frequency, specified V_{DS} and specified V_{GS} or I_D	g_{22ss}	(x)	(x)	(x)
+	5.9	Minimum and maximum short-circuit forward transconductance at specified frequency, specified V_{DS} and specified V_{GS} or I_D	y_{21s}	x	x	x
+	5.10	For low noise types only: Maximum noise voltage or noise factor in common-source configuration, under specified conditions of bias, source resistance, centre frequency and power bandwidth.	V_n or F	x	x	x
	5.11	When virtual junction temperature is quoted as a rating: maximum value of thermal resistance junction to ambient	$R_{th(j-amb)}$	x	x	x

6 Test conditions and inspection requirements

These are given in the following tables, where the values and exact conditions to be used should be specified as required in the detail specification relevant to a given type in line with the indications given in CECC 50000 for the relevant test.

The tables refer to two levels of quality assessment arbitrarily designated F and L, it being understood that there may be other levels in other blank detail specifications.

All references to part numbers are made with respect to CECC 50000 unless otherwise stated.

GROUP A — Lot-by-lot								
All tests are non destructive (3.5.6 of CECC 50000)					AQL = given in % ⊕ 1 % if more than 3 tests			
Examination or test	Ref.	Conditions at T _{amb} = 25 °C unless otherwise stated	Inspection requirements					
			Limits		Levels			
			Types A and B	Type C	F		L	
					IL	AQL	IL	AQL
<u>SUB-GROUP A1</u>					I	1,5	I	1,5
Visual inspection	4.2.1	4.2.1	4.2.1	4.2.1				
<u>SUB-GROUP A2</u>					II	0,65	II	0,65
<u>Leakage or cut-off current</u> (see 5.1 of this document)	4.3.4 T-071		max	max		⊕		⊕
Either:								
I_{GDO (1)}		V _{GD} = preferably V _{GDO} max I _S = 0						
or:								
I_{GSS (1)}		V _{GS} = preferably V _{GSR} max V _{DS} = 0						
or:								
I_{GS}		V _{DS} = specified V _{GS} or I _D = specified						
Gate-source cut-off voltage	4.3.4 T-074	V _{DS} = specified I _D = specified (preferably ≤ 1 μA)	max min	—				
Drain current	4.3.4 T-072	V _{DS} = specified V _{GS} = 0 d.c. or pulse as specified (note 1)	max min	—				
Gate-source threshold voltage	4.3.4 T-075	V _{DS} = specified I _D = specified	—	max min				
Drain current	4.3.4 T-072	V _{DS} = specified V _{GS} = specified	—	max min				

NOTE 1 If pulse measurement is used, the conditions should preferably be: pulse width $t_p = 300\text{ }\mu\text{s}$ duty factor $< 2\%$

[illegible]

GROUP B — Lot-by-lot								
Only tests marked: (D) are destructive (3.5.6 of CECC 50000)								
LSL = lower specification limit (Group A)					AQL = given in %			
USL = upper specification limit (Group A)					na = not applied			
Examination or test	Ref.	Conditions at T _{amb} = 25 °C unless otherwise stated	Inspection requirements					
			Limits		Levels			
			Types A and B	Type C	F		L	
IL	AQL	IL			AQL			
<u>SUB-GROUP B1</u>								
Dimensions	4.2.2	4.2.2/Appendix III	4.2.2	4.2.2	S2	2,5	S2	2,5
<u>SUB-GROUP B3</u>								
Lead bending (D) if applicable	4.4.9	4.4.9	4.4.9	4.4.9	S3	2,5	S2	2,5
<u>SUB-GROUP B4</u>								
Solderability	4.4.7	As specified	4.4.7	4.4.7	S4	2,5	S4	2,5
<u>SUB-GROUP B5</u>								
Change of temperature followed by: accelerated damp heat (D) or sealing	4.4.4 4.4.2 4.4.10	} As specified }	V _{GSoff} and leakage current (A2) within original limits	V _{GS (T0)}	S4	2,5	na	na
<u>SUB-GROUP B8</u>								
Electrical endurance (168 h)	4.5	4.5.2.10 Electrical operation or high temperature reverse bias, as specified	V _{GSoff} ≥ 0,8 LSL and ≤ 1,2 USL leakage current (A2): ≤ 10 USL I _{DSS} ≥ 0,9 LSL and ≤ 1,1 USL	V _{GS (T0)}	S4	1,5	na	na
<u>SUB-GROUP CTR</u>	Attributes information for B3, B4, B5 and B8							

GROUP C — Periodic

Only tests marked: (D) are destructive (3.5.6 of CECC 50000)

na = not applied

LSL = lower specification limit (Group A)

USL = upper specification limit (Group A)

P = periodicity in months

n = sample size

c = acceptance criterion

Examination or test	Ref.	Conditions at T _{amb} = 25 °C unless otherwise stated	Inspection requirements								
			Limits		Levels						
			Types A and B	Type C	F			L			
					P	n	c	P	n	c	
<u>SUB-GROUP C1</u>					3	8	1	3	8	1	
Dimensions	4.2.2	4.2.2/Appendix III	4.2.2	4.2.2							
<u>SUB-GROUP C2a</u>					3	13	1	3	13	1	
Short-circuit input capacitance C_{11ss}	4.3.4 T-076	f = 1MHz V _{DS} = specified V _{GS} = specified	max	max							
Where appropriate: Short-circuit output conductance g_{22ss}	4.3.4 T-077	f = specified V _{DS} = specified V _{GS} or I _D = specified	max	max							
<u>SUB-GROUP C2b</u>					3	18	1	3	18	1	
<u>Leakage current at high temperature:</u>	4.3.3	T _{amb} = <u>specified high</u> and	max	max							
Either: I _{GDO (2)}	4.3.4 T-071	V _{GD} = preferably between 65 % and 85 % of V _{GDO} max I _S = O									
or: I _{GSS (2)}	4.3.4 T-071	V _{GS} = preferably between 65 % and 85 % of V _{GSR} max V _{DS} = O									
<u>SUB-GROUP C3</u>					3	8	1	6	8	1	
Tensile (D), and/or Torque	4.4.9	4.4.9	4.4.9 or as specified								

GROUP C — Periodic					cont'd						
Only test marked: (D) are destructive (3.5.6 of CECC 50000)											
na = not applied					P = periodicity in months						
LSL = lower specification limit (Group A)					n = sample size						
USL = upper specification limit (Group A)					c = acceptance criterion						
Examination or test	Ref.	Conditions at T _{amb} = 25 °C unless otherwise stated	Inspection requirements								
			Limits		Levels						
			Types A and B	Type C	F			L			
					P	n	c	P	n	c	
<u>SUB-GROUP C4</u> Resistance to soldering heat (D)	4.4.8	4.4.8	V _{GSoff}	V _{GS (TO)} and leakage current (A2) within original limits	3	18	1	na	na	na	
<u>SUB-GROUP C5</u> Change of temperature followed by: accelerated damp heat (D) or sealing	4.4.4 4.4.2 4.4.10	As specified	V _{GSoff}	V _{GS (TO)} and leakage current (A2) within original limits	na	na	na	3	13	1	
<u>SUB-GROUP C6</u> — Shock or acceleration — Vibration	4.4.4 or 4.4.11 4.4.6	As specified	V _{GSoff}	V _{GS (TO)} and leakage current (A2) within original limits	3	8	1	6	8	1	
<u>SUB-GROUP C7</u> Damp heat (steady state) if applicable (D)	4.4.3	As specified	As specified		3	18	1	na	na	na	

GROUP C — Periodic

cont'd

Only tests marked: (D) are destructive (3.5.6 of CECC 50000)

na = not applied

P = periodicity in months

LSL = lower specification limit (Group A)

n = sample size

USL = upper specification limit (Group A)

c = acceptance criterion

Examination or test	Ref.	Conditions at $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise stated	Inspection requirements							
			Limits		Levels					
			Types A and B	Type C	F			L		
<u>SUB-GROUP C8</u> Electrical endurance (1 000 h min)	4.5	4.5.2.10 Electrical operation or high temperature reverse bias, as specified	V_{GSoff} $\geq 0,8 \text{ LSL and } \leq 1,2 \text{ USL}$ leakage current (A2): $\leq 10 \text{ USL}$ $0,9 \text{ LSL } \leq y_{21s} \leq 1,1 \text{ USL}$ I_{DSS} $\geq 0,9 \text{ LSL and } \leq 1,1 \text{ USL}$	$V_{GS(TO)}$	3	43	3	3	32	3
<u>SUB-GROUP C9</u> Storage at high temperature (D)	4.4.1	Min: 1 000 h at max T_{stg}	V_{GSoff} $\geq 0,8 \text{ LSL and } \leq 1,2 \text{ USL}$ leakage current (A2): $\leq 10 \text{ USL}$ $0,9 \text{ LSL } \leq y_{21s} \leq 1,1 \text{ USL}$ I_{DSS} $\geq 0,9 \text{ LSL and } \leq 1,1 \text{ USL}$	$V_{GS(TO)}$	3	43	3	na	na	na
<u>SUB-GROUP CTR</u>	Attributes information for C3, C5, C6 and C9 Measurement information for: V_{GSoff} or $V_{GS(TO)}$, leakage current (A2) and y_{21s} before and after C8									

Section 2. High frequency amplification

Numbers between square brackets on the next page correspond to the following indications which should be given:

Identification of the detail specification

- [1] The name of National Standards Organization under whose authority the detail specification is drafted
- [2] The CECC Symbol and the number allotted by the CECC General Secretariat to the completed detail specification
- [3] The number and issue number of the national generic and sectional specifications
- [4] The national number of the detail specification, date of issue and any further information required by the national system.

Identification of the component

- [5] A short description of the type of component
- [6] Information on typical construction (where applicable)
- [7] Outline drawing and/or reference to the relevant document for outlines
- [8] Application or group of applications covered (see note below)
- [9] Reference data on the most important properties, to allow comparison between the various component types.

NOTE When a device is so designed that it can satisfy several applications, this should be stated in the detail specification, in which case the characteristics and inspection requirements relevant to these applications should be met simultaneously (these may appear in different columns of a blank detail specification or in different blank detail specifications, as the case may be).