

**Harmonized system of quality
assessment for electronic components**

Film and hybrid integrated circuits —

**Part 2: Internal visual inspection and
special tests**

The European Standard EN 165000-2:1996 has the status of a
British Standard

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Committees responsible for this British Standard

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- Federation of the Electronics Industry
- Ministry of Defence
- National Supervising Inspectorate (BSI Product Certification)

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National foreword

This British Standard has been prepared by Subcommittee EPL/47/1 and is the English language version of EN 165000-2:1996, *Film and hybrid integrated circuits — Part 2: Internal visual inspection and special tests* published by the European Committee for Electrotechnical Standardization (CENELEC).

Cross-references

Publication referred to	Corresponding British Standard
	BS EN 165000 <i>Film and hybrid integrated circuits</i>
EN 165000-1:1996	BS EN 165000-1:1996 <i>Generic specification. Capability approval procedure</i>
EN 165000-3:1996	BS EN 165000-3:1996 <i>Self-audit checklist and report for film and hybrid integrated circuit manufacturers</i>
EN 165000-4:1996	BS EN 165000-4:1996 <i>Customer information, product assessment level schedules and blank detail specification</i>

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to ii, the EN title page, pages 2 to 26, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Film and hybrid integrated circuits Part 2: Internal visual inspection and special tests

This European Standard was approved by CENELEC on 1996-03-05. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

This European Standard was prepared by CLC/TC CECC SC 47AX (former CECC/WG 21), Film and hybrid integrated circuits.

The text of the draft was submitted to the Unique Acceptance Procedure and was approved by CENELEC as EN 165000-2 on 1996-03-05.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1997-03-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 1997-03-01

The present standard, EN 165000-2 *Film and hybrid integrated circuits — Part 2: Internal visual inspection and special tests* is intended to be read in conjunction with the other parts of EN 165000, which are:

- *Part 1: Generic specification — Capability approval procedure;*
- *Part 3: Self-audit checklist and report for film and hybrid integrated circuit manufacturers;*
- *Part 4: Customer information, product assessment level schedules and blank detail specification.*

Part 3 is primarily intended as a pro-forma for the manufacturer and is not considered *essential* for a customer *in this form*.

Part 4 is considered an essential document for all users; in particular it includes a helpful introductory section which is aimed at potential customers and seeks to explain the underlying philosophy upon which the whole standard is based.

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Section 1. Internal Visual inspection

1 General

1.1 Purpose

The purpose of these examinations is to check the internal materials, added components, construction and workmanship of film and hybrid integrated circuits.

These examinations will normally be used prior to capping or encapsulation to detect and eliminate the circuits with internal defects that could lead to device failure in normal application. Other acceptance criteria may be agreed upon with the purchaser or supplier respectively.

1.2 Sequence of inspection

The sequence which is presented is not a required order of examination and may be varied at the discretion of the manufacturer. Any aspect which may be obscured by a subsequent assembly process shall be examined before that process.

1.3 Inspection apparatus

The apparatus for this test shall include optical equipment capable of the specified magnification(s) and any visual standards (gauges, drawings, photographs, etc...) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined. Adequate fixtures shall be provided for handling devices during examination to promote efficient operation without inflicting damage to the units.

1.4 Inspection environment

Under consideration.

1.5 Magnification

“High magnification” (100 to 200 x) inspection is normally performed with a microscope perpendicular to the relevant surface with the device under illumination normal to the relevant surface.

“Low magnification” (10 to 100 x) inspection is normally performed with a monocular, a binocular or a stereomicroscope at an appropriate angle and illumination.

1.6 Definitions

1.6.1

active circuit area

all areas of functional circuit elements, operating metallization or any connected combinations thereof

1.6.2

multi-layer metallization (for conductors)

two or more layers of metal or any other material used for interconnections that are not isolated from each other

1.6.3

edge metallization

metallization that electrically connects different layers of metallization on or within a substrate at its edge

1.6.4

foreign material

any material not used in the manufacture of the microcircuit or any in-built material that is displaced from its original or intended position within the microcircuit package. Foreign material that appears opaque under those conditions of lighting and magnification used in routine visual inspection shall be considered as conductive

1.6.5

protective layer (passivation)

the layer of insulating material that protects part or all of the substrate area, including metallization, but excluding connecting pads, for example glassivation, solder resist, etc...

1.6.6

isolating layer

a layer used to isolate separate conductive or resistive levels

1.6.7

kerf

the slit or cut made by a material-removing process (for example laser or abrasive trimming)

1.6.8

multi-level metallization (for conductors)

two or more levels of metal or any other material used for interconnections that are isolated from each other by a grown or deposited insulating material and interconnected for example by vias or edge metallization

1.6.9

bond pad area

that area of exposed metallization which is not covered by passivation

1.6.10

compound bond

bonding of one bond on top of another bond

1.6.11

through hole metallization

metallization that electrically connects different levels of metallization on or within a substrate via a hole or holes

1.6.12 scratch

any tearing defect in the surface of a layer

1.6.13 cosmetic scratch

a shallow scratch which may extend completely across a layer and which does not expose or damage underlying layers, or laterally displace metallization beyond the edge of the conductor for example by mechanical deformation

1.6.14 void

any defect in a layer not caused by a scratch where underlying material is visible

1.7 Interpretation

Reference herein to “that exhibits” shall be considered satisfied when the visual image or visual appearance of the device under examination indicates a specific condition is present.

This shall not require confirmation by any other method of testing.

1.8 Alternative test methods

The visual examination requirements given below are not necessarily the only methods which can be used.

However the manufacturer shall satisfy the ONS that any alternative method will give equivalent assurance otherwise the specified method shall be used.

2 Substrate and processes

Low magnification

2.1 Substrate

No device shall be acceptable that shows the following:

- Holes through the substrate, except through lead holes, used or unused component mounting holes, or alignment holes.
- Any crack that exceeds 0,125 mm in length and points toward an operating portion of the circuit — see Figure 1.
- Any chip-out that reduces any active (metallized) circuit area — see Figure 2.
- Any crack that comes closer than 0,025 mm to an operating portion of the circuit — see Figure 3.
- Any substrate having attached portions of another substrate that exceed the substrate dimensions allowed by the assembly drawing — see Figure 4.

— Any substrate having a section broken out around any substrate mounting hole greater than 25 % of the mounting hole circumference when designed for substrate to post attachment — see Figure 5.

— Any crack that originates at an edge — see Figure 6.

2.2 Processes

2.2.1 Conductors

No device shall be acceptable that shows the following:

1) Metallization scratches

A scratch is any tearing effect, including probe marks, in the surface of the metallization.

— Scratch in the metallization excluding bonding pads that exposes the substrate or underlying dielectric anywhere along its length and leaves less than 50 % of the metal width undisturbed — see Figure 7.

— Scratch in multilayered metallization that exposes the underlying metal anywhere along its length and leaves less than 50 % of the top layer metal width undisturbed — see Figure 8.

— Scratch in the bonding pad or fillet area that exposes the underlying dielectric or substrate and reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately — see Figure 9.

2) Metallization voids

— Void(s) in the metallization except for wire or beam lead bonding pads that leaves less than 50 % of the metal width undisturbed — see Figure 7.

— Void(s) in the wire or beam lead bonding pad area that leaves an area less than twice the maximum allowable bond size undisturbed.

— Void(s) in the wire or beam lead bonding pad, including fillet area, that reduces the metallization path width connecting the bond to the interconnecting metallization to less than 50 % of the narrowest entering interconnect metallization stripe width — see Figure 9

NOTE If two or more stripes enter a bonding pad, each shall be considered separately.

3) Metallization corrosion

Any metallization corrosion — see Figure 10.

4) Metallization adherence