

BS EN 16602-30-11:2014



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Space product assurance — Derating — EEE components

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National foreword

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The UK participation in its preparation was entrusted to Technical Committee ACE/68, Space systems and operations.

A list of organizations represented on this committee can be obtained on request to its secretary.

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English version

Space product assurance - Derating - EEE components

Assurance produit des projets spatiaux - Derating des
composants EEE

Raumfahrtproduktsicherung - Herabsetzen/Unterlastung
von EEE-Komponenten

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Foreword

This document (EN 16602-30-11:2014) has been prepared by Technical Committee CEN/CLC/TC 5 "Space", the secretariat of which is held by DIN.

This standard (EN 16602-30-11:2014) originates from ECSS-Q-ST-30-11C Rev 1.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by March 2015, and conflicting national standards shall be withdrawn at the latest by March 2015.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

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Introduction

This Standard specifies derating requirements applicable to electronic, electrical and electromechanical components.

Derating is a long standing practice applied to components used on spacecrafts. Benefits of this practice are now proven, but for competitiveness reasons, it becomes necessary to find an optimized reliability. Too high a derating can lead to over-design, over-cost and over-sizing of components, the direct consequence being excess volume and weight. The aim is to obtain reliable and high performance equipment without over-sizing of the components. For this reason and if possible, this Standard provides derating requirements depending on mission duration and mean temperature, taking into account demonstrated limits of component capabilities.

1

Scope

This Standard applies to all parties involved at all levels in the realization of space segment hardware and its interfaces.

The objective of this Standard is to provide customers with a guaranteed performance and reliability up to the equipment end-of-life. To this end, the following are specified:

- Load ratios or limits to reduce stress applied to components;
- Application rules and recommendations.

This standard may be tailored for the specific characteristics and constraints of a space project, in accordance with ECSS-S-ST-00.

2

Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system - Glossary of terms
EN 16602-60	ECSS-Q-ST-60	Space product assurance - Electrical, electronic and electromechanical (EEE) components
	ESCC 2269010	Evaluation test programme for monolithic microwave integrated circuits (MMICS)
	ESCC 2265010	Evaluation Test Programme for Discrete Microwave Semiconductors

Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 ambient temperature

temperature surrounding a component

3.2.2 case temperature

temperature on the component package surface

3.2.3 derating

process of designing a product such that its components operate at a significantly reduced level of stress to increase reliability and to insure useful life and design margins.

3.2.4 hot spot temperature

highest measured or predicted temperature within any component

3.2.5 junction temperature

highest measured or predicted temperature at the junction within a semiconductor or micro-electronic device

NOTE Predicted temperature can be taken as $T_{\text{case}} +$
thermal resistance between junction and case times
actual power (Watt) of the device.

3.2.6 load ratio

permissible operating level after derating has been applied; given as a percentage of a parameter rating

3.2.7 operating conditions

parameter stress and environment (temperature, vibration, shock and radiation) in which components are expected to operate

3.2.8 *term "performance" deleted*

3.2.9 **RadPack**

package designed to provide some form of radiation protection

3.2.10 **rating**

maximum parameter value specified and guaranteed by the component manufacturer and component procurement specification

NOTE Rating is considered as a limit not to be exceeded during operation and constitutes in most cases the reference for derating.

3.2.11 **surge**

strong rush or sweep

[Collins dictionary and thesaurus]

3.2.12 **transient**

brief change in the state of a system

[Collins dictionary and thesaurus]

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
A/D	analog to digital
ASIC	application specific integrated circuit
C	capacitance
DRAM	dynamic random access memory
EEPROM	electrical erasable programmable read only memory
EPROM	erasable programmable read only memory
ESCC	European Space Component Coordination
ESR	equivalent series resistance
f	frequency
FET	field effect transistor
GaAs	gallium arsenide
ISO	International Organization for Standardization
InP	indium posphide
LED	light emitting diode
MOS	metal on silicon

Abbreviation	Meaning
MIL (spec)	specification of the US Department of Defense
MMIC	monolithic microwave integrated circuit
NASA	National Aeronautics and Space Administration
P	power
PROM	programmable read only memory
RadHard	radiation hardened
Ri	insulation resistance
RF	radio-frequency
SEBO	single event burn-out
SEGR	single event gate rupture
Si, SiGe	silicon, silicon germanium
SOA	safe operating area
SRAM	static random access memory
T _j	junction temperature
T _{jmax}	absolute maximum rated junction temperature
T _{op}	operating temperature
V _{CE}	collector-emitter voltage

4

User responsibility

- a. The user of this Standard shall verify that the ordered assurance level of procured components is compatible with the intended application.

5

Derating

5.1 Overview

The term derating refers to the intentional reduction of electrical, thermal and mechanical stresses on components to levels below their specified rating. Derating is a means of extending component life, increasing reliability and enhancing the end-of-life performance of equipment.

Derating participates in the protection of components from unexpected application anomalies and board design variations.

The load ratios or limits given in clause 6 were derived from information available at the time of writing this Standard and do not preclude further derating for specific applications.

This Standard also defines how to handle transients.

5.2 Principles of derating

The component parameter strength defines the limits and the performance component technology in the particular application and varies from manufacturer to manufacturer, from type to type, and from lot to lot and can be represented by a statistical distribution. Likewise, component stress can be represented by a statistical distribution. Figure 5-1 illustrates the strength of a component and the stress applied at a given time, where each characteristic is represented by a probability density function.

A component operates in a reliable way if its parameter strength exceeds the parameter stress. The designer should ensure that the stress applied does not exceed the component parameter strength. This is represented by the intersection (shaded area) in Figure 5-1. The larger the shaded area, the higher the possibility of failure becomes.

There are two ways, which may be used simultaneously, in which the shaded area can be decreased:

- Decrease the stress applied (which moves the stress distribution to the left).
- Increase the component parameter strength (by selecting over-sized components) thereby moving the strength distribution to the right.

The goal is to minimize the stress-to-strength ratio of the component. Derating moves the parameter stress distribution to the left while the selection processes applied to the components for space applications contribute to moving the

parameter strength distribution to the right. The selection processes also reduce the uncertainty associated with the component parameter strength.

Derating reduces the probability of failure, improves the end-of-life performance of components and provides additional design margins.

Another effect of derating is to provide a safety margin for design. It allows integrating parameter distribution from one component to another, and from one procurement to another.

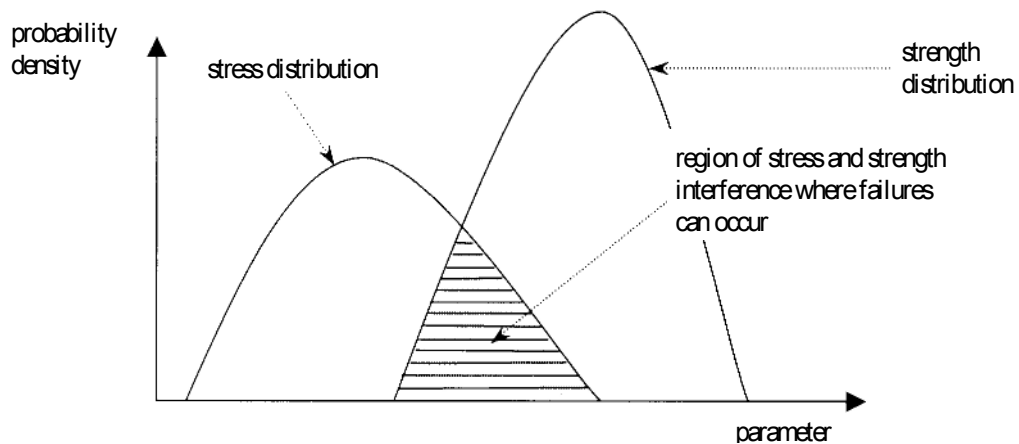


Figure 5-1: Parameter stress versus strength relationship

5.3 Applicability and component selection

5.3.1 Overview

This Standard applies to all components, selected for space applications, that are used for a significant duration. The meaning of “significant duration” is a period that contributes to the component life, for instance, one month is considered to be a significant duration. These requirements apply to screened components procured in accordance with approved space specifications.

This Standard only applies to approved components for which quality was proven after rigorous testing in accordance with ECSS-Q-ST-60.

Derating applies on normal operational conditions, where “normal” is opposed to “fault” and “Operational” indicates all functional modes of the unit.

Derating analysis is performed at the equipment maximum hot acceptance temperature, unless otherwise specified.

5.3.2 Requirements

- Derating shall be applied in consideration of temperature limits recommended by the manufacturer.
- The derating requirements of this Standard shall not be used as a justification to upgrade the quality level of components.

- c. The derating requirements shall be taken into account at the beginning of the design cycle of an equipment for any consequential design trade-off to be made. Specific attention shall be paid to, for example, breadboards and engineering models where parameter derating was not considered.
- d. Component families and groups excluded in this Standard are due to the lack of experimental data and failure history. For these components, the user shall consult a component design and reliability specialist to apply the requirements of this Standard.
- e. Components may be excluded from this Standard if they are used for short durations of less than one month provided the device ratings are not exceeded; for example, components used in solar generator deployment systems, redundancy commutation and launchers (except in some specific cases, noted family by family). In these cases, the designer shall ensure that the applied stress level does not exceed the component maximum rating.
- f. The derating requirements are not applicable to test conditions (e.g. circuit or equipment level qualification and EMC) for which the maximum ratings shall not be exceeded.
- g. Derating requirements are not applicable to fault conditions, for which the maximum rating shall not be exceeded, with the exception defined in 5.3.2h.
- h. Where components are required to operate in protection mode or in fail-safe mode in order to prevent failure propagation (e.g. short-circuit protection), the components concerned shall meet the derating requirements and application rules when performing the protection or fail-safe function under the worst failure case (i.e. highest stress applied to the components that can last throughout the mission).

5.3.3 Requirements ESCC exceptions

- a. For a particular type or manufacturer, when a specific derating rule is defined in the appendix of the approved ESCC detail specification issued by the ESCC Executive, it shall take precedence over the generic requirement of this standard.
- b. Users shall check for application the actual status of the ESCC Derating exceptions on the following ESCC web site page: [ESCC Derating deviations](#)

NOTE A list of the ESCC detail specifications applicable at the time of publication and containing deviations to general derating requirements of this standard is available in informative Annex B.

- c. Users shall clearly identify in the Parts Stress Analysis document the list of the ESCC Derating exceptions taken into consideration in their analysis.

5.4 Derating parameters

5.4.1 Overview

Derating requirements are provided in clause 6 for each component family.

For each category, the parameters to be derated are identified. The main parameters to be derated are:

- junction or case temperature;
- power (rating, dissipation);
- voltage;
- current.

The parameters to be derated depend on component type.

A stress balancing concept offers flexibility between one stress versus another (voltage and temperature). In some cases, e.g. resistors, derating has a direct impact on component performance.

5.4.2 Requirements for transient and surge conditions

- a. For transient or surge conditions, if ratings are provided, the same derating figures as for steady-state equivalent parameters shall be used.
- b. For transient or surge conditions, if ratings are not provided, then it shall be assured that the transient or surge values are below the steady-state specified maximum ratings.
- c. For all periodic signals or transient conditions which are repeated or made incessant, the steady-state derating figures shall apply.
- d. <<deleted>>
- e. As an exception in case clause 5.4.2c is not compatible for specific repeated and incessant transient use conditions, for the parts types and parameters listed, load ratio shall not exceed the steady state derated values +10 % or 80 % of the steady state rated values, whichever is lower:
 1. Connectors: voltage, current
 2. Ceramic Capacitors: voltage
 3. Resistors: current
 4. Diodes: current
 5. Transistors_ bipolar , MOSFETs, power FETs: current.

5.5 Additional rules and recommendations

5.5.1 Overview

In addition to strict derating requirements, some application rules and recommendations are given in this Standard to achieve the suitable reliability. This additional application rules and recommendations are listed separately in the clauses titled “Additional requirements not related to derating”. This disposition is valid until other adequate ECSS documents can host these additional clauses.

5.5.2 Additional requirements not related to derating

- a. Where radiation sensitive components are identified, it is the user's responsibility that the chosen component technologies are suitable and that the mitigation factors, such as shielding, meet the customer's requirement. The electrical derating shall be in accordance with this Standard.

6

Tables for load ratios or limits

6.1 Overview

This clause provides the load ratios or limits.

They are also available on the World Wide Web at the following address:

<https://escies.org>

Abbreviations used in the tables are explained in clause 3.

Annex A contains a complete listing of the family and group codes for parts that are referred to in this Standard.

Annex B contains ESCC exceptions at date of publication of this standard.

6.2 Capacitors: ceramic - family-group code: 01-01 and 01-02

6.2.1 General

- The capacitor stress sum value of steady-state voltage, AC voltage shall not exceed the load ratios specified hereunder. For transients refer to clause 5.4.
- Multilayer capacitors with a DC voltage rating less than 100 V may be used in low voltage (less than 10 V) continuous applications provided they have been submitted to a low voltage (1,5 V) 85 % humidity at 85 °C test or other approved method.
- <<deleted>>
- Internal heating due to ESR can increase ageing and should be taken into account by applying a margin in temperature. Where ESR is not known at the frequency of a ripple current, an extrapolation of the ESR value and resonance (from manufacturer's or test data) should be made where possible.

6.2.2 Derating

- Parameters of capacitors from family-group code 01-01 and 01-02 shall be derated as per Table 6-1.

Table 6-1: Derating of parameters for capacitors family-group code 01-01 and 01-02

Parameters	Load ratio or limit
Voltage	

6.2.3 Additional requirements not related to derating

- The dV/dt rating capability of the capacitors shall be respected.