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BSI Standards Publication

Space product assurance — Design rules for printed circuit boards



National foreword

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Space product assurance - Design rules for printed circuit boards

Assurance produit des projets spatiaux - Règles de
conception des circuits imprimésRaumfahrtproduktsicherung - Designregeln für
Leiterplatten

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European foreword

This document (EN 16602-70-12:2016) has been prepared by Technical Committee CEN-CENELEC/TC 5 “Space”, the secretariat of which is held by DIN.

This European Standard (EN 16602-70-12:2016) originates from ECSS-Q-ST-70-12C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by April 2017, and conflicting national standards shall be withdrawn at the latest by April 2017.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

Introduction

PCBs are used for the mounting of electronic components to produce PCB assemblies that perform electrical functions. The PCBs are subjected to thermo-mechanical stress during assembly such as soldering of components, rework and repair under normal terrestrial conditions. In addition the assembled PCBs are exposed to the launch and space environment. The reliability of the circuit depends on the robustness of the design, among other factors. Moreover, PCB design with high technological complexity enables the use of complex components with advanced functionality.

1

Scope

This European Standard specifies the requirements for the supplier and PCB manufacturer for PCB design.

This European Standard is applicable for all types of PCBs, including sequential, rigid and flexible PCBs, HDI and RF PCBs.

This European Standard can be made applicable for other products combining mechanical and electrical functionality using additive or reductive manufacturing processes, as used in PCB manufacturing. Examples of such products are slip rings and bus bars.

This European Standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

2

Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

EN reference	Reference in text	Title
EN 16602-00-01	ECSS-S-ST-00-01	ECSS system – Glossary of terms
EN 16602-70-02	ECSS-Q-ST-70-02	Space product assurance - Thermal vacuum outgassing test for the screening of space materials
EN 16602-70-08	ECSS-Q-ST-70-08	Space product assurance - Manual soldering of high-reliability electrical connections
EN 16602-70-10	ECSS-Q-ST-70-10	Space product assurance - Qualification of printed circuit boards
EN 16602-70-11	ECSS-Q-ST-70-11	Space product assurance - Procurement of printed circuit boards
EN 16602-70-38	ECSS-Q-ST-70-38	Space product assurance -High-reliability soldering for surface-mount and mixed technology
EN 16603-20	ECSS-E-ST-20	Space engineering – Electrical and electronic
EN 16603-20-06	ECSS-E-ST-20-06	Space engineering - Spacecraft charging
	IPC-2152, August 2009	Standard for determining current carrying capacity in printed board design
	IPC-4101D, April 2014	Specification for base materials for rigid and multilayer printed boards
	IPC-4562A, April 2008	Metal foil for printed wiring applications

Terms, definitions and abbreviated terms

3.1 Terms from other standards

- a. For the purposes of this document, the terms and definitions from ECSS-S-ST-00-01 apply, and in particular for the following terms:

1. **supplier**

NOTE In the context of this European Standard the supplier is also responsible for the design of the PCB.

3.2 Terms specific to the present standard

3.2.1 annular ring

ring of copper pad surrounding the drilled hole

NOTE The measurement of annular ring is different on internal and external layers. See Subclause 6.3.1 from ECSS-Q-ST-70-11.

3.2.2 area array device (AAD)

surface mount package wherein the solder terminations are formed in a grid on the bottom of the package

NOTE BGA and CGA are specific types of AAD.

3.2.3 artwork

graphical representation of individual layers

NOTE Examples of artwork are: conductive layers, solder mask, silk screen, selective finishes, heat sink.

3.2.4 as-designed

state of the PCB in the design phase

NOTE This typically refers to dimensions associated with the designed PCB, which does not take into account manufacturing tolerances.

3.2.5 as-manufactured

state of the PCB after manufacturing

NOTE This typically refers to dimensions measured on the manufactured PCB, the final product. The dimensions are measurements that include manufacturing tolerances.

3.2.6 as-manufactured hole

hole in as-manufactured PCB after all process steps

NOTE In case of a plated through-hole, an as-manufactured hole includes plating and surface finish.

3.2.7 aspect ratio

ratio of the as-designed thickness of the build-up and the diameter of the drilled hole

3.2.8 assembled PCB

PCB with all its electronic and mechanical components mounted, having undergone all the manufacturing operations

NOTE Examples of manufacturing operations are wiring, soldering, wire-bonding, gluing, screwing, potting and conformal coating.

3.2.9 assembly house

company performing assembly of PCB

3.2.10 back-drilled hole

via with part of its metallisation removed on one side by depth controlled mechanical drilling with a larger diameter drill

3.2.11 ball grid array (BGA)

surface mount package wherein the solder balls for terminations are formed in a grid on the bottom of the package

NOTE BGA is a specific type of AAD.

3.2.12 basic copper

copper foil layer that excludes etching and plating steps

3.2.13 blind via

type of via exposed only on one side of the PCB

NOTE One method to manufacture a blind via can be by depth controlled drilling. A second method can be by sequential lamination of minimum 2 half-stacks.

3.2.14 bondply

type of cover layer with adhesive on both sides for the purpose of bonding flex laminate

NOTE Bondply is a trademark manufactured by DuPont.

3.2.15 build-up

technical representation of individual conductive layers and dielectric materials of the specific PCB design

NOTE Examples of a build-up are given in Figure 3-1 and Figure A-4

3.2.16 buried via

type of via connecting internal layers without being exposed on either surface

3.2.17 column grid array (CGA)

surface mount package wherein the columns for terminations are formed in a grid on the bottom of a package

NOTE CGA is a specific type of AAD.

3.2.18 conductive layer

electrically conductive parts of a PCB on the same layer

NOTE The conductive layer can contain tracks, planes or pads.

3.2.19 conductor

conductive elements within the PCB

NOTE Elements within the conductive layer and vias are conductors.

3.2.20 critical net

conductive circuit with a specific functionality that requires redundant solutions to avoid loss of functionality in case of any credible single failure

NOTE Redundant solutions can be double insulation, increased copper cross section, multiple vias.

3.2.21 critical track

track that is part of a critical net

3.2.22 double insulation

barrier between tracks or elements of an electronic circuit that provides insulation of tracks or elements of an electronic circuit in case of any credible single failure

3.2.23 drilled hole

hole after drilling and before plating

NOTE In case of a plated through-hole, drilled hole excludes plating and surface finish

3.2.24 electrical field

voltage per insulation distance between two conductors

NOTE This is a simplified representation of electrical field applicable for PCB design.

3.2.25 fine pitch

spacing of tracks or pads that is more dense than for normal pitch

NOTE The exact perimeter of fine pitch on external and internal layers is described in Subclause 7.4.

3.2.26 FR4

type of laminate and prepreg with a specific epoxy resin

3.2.27 half-stack

sequence of laminated layers that are included in further lamination sequences to form the finished PCB

3.2.28 heat sink

layer of thick metal with the purpose of thermal dissipation internal or external of the PCB

NOTE Term “thermal drain” is synonymous with the word “heat sink”.

3.2.29 high density interconnect (HDI)

technology on PCB related to the pattern that allows a smaller pitch in the footprint on the surface pattern and a higher density of internal signal routing than for conventional PCBs

NOTE 1 The exact perimeter of HDI technology is described in Clause 11.

NOTE 2 This technology can be required for assembly of AAD.

NOTE 3 An example of HDI build-up is shown in Figure 3-1.

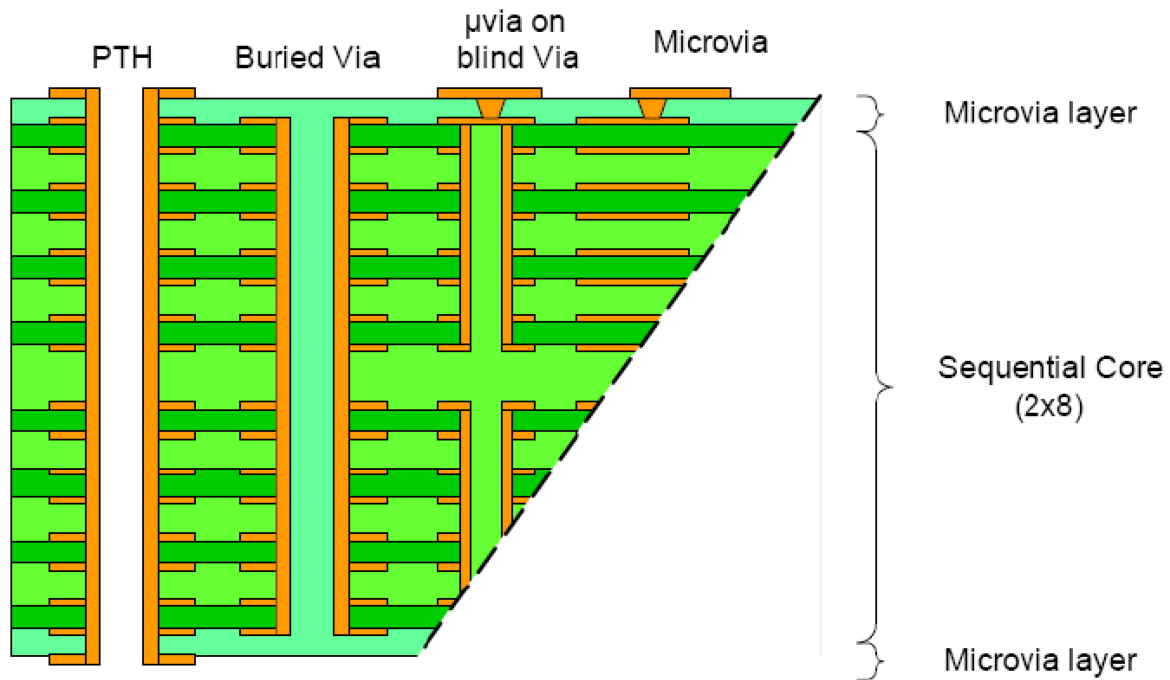


Figure 3-1: Simplified build-up of HDI PCB

3.2.30 high speed signal

electronic functionality that requires specific design precautions to maintain time dependant signal integrity

NOTE This is further specified in IPC-2251 and IPC-2141A.

3.2.31 hole wall pull away

adhesion defect between copper of the hole wall and resin

3.2.32 HTE

grade of copper foil with the grade designation "high temperature elongation electrodeposited"

NOTE This is specified in IPC-4562A.

3.2.33 intralayer

within the same layer in X,Y direction

3.2.34 interlayer

in between two superpositioned layers in Z direction

3.2.35 JTC

grade of copper foil

NOTE This grade of copper foil is produced by GOULD Electronics GmbH.

3.2.36 laminate

sheets of fully cured, C-stage, resin with copper cladding

NOTE Rigid laminate includes reinforcement, for example by woven glass fibres or non-woven aramid fibres.

3.2.37 microvia

blind via manufactured by laser ablation with a diameter smaller than conventional vias.

NOTE 1 Microvias are required for routing internal signals in HDI PCBs.

NOTE 2 Example of microvia configuration is shown in Figure 3-1.

3.2.38 microvia layers

layers of conductive pattern that contain microvias

NOTE microvia layers are layers 1 and 2 and opposite layers

3.2.39 mil

unit of length equal to 25,4 μm

NOTE The unit mil is in some cases customary in PCB design and therefore preferred above the SI unit.

3.2.40 no-flow prepreg

type of prepreg that has a reduced flow of resin during press cycle

NOTE The term "low-flow prepreg" is synonymous with the word "no-flow prepreg". The terms do not specify the exact amount of flow.

3.2.41 non-functional pad

pad on internal copper layer without electrical connection

3.2.42 non-plated hole

hole in a PCB that does not contain plating or other type of conductive reinforcement

3.2.43 normal pitch

standard spacing of tracks and pads

NOTE See "fine pitch" for another category of pitch.

3.2.44 number of layers

number of layers in a PCB containing conductive elements

NOTE For example, the numbering convention is from top to bottom layer: L1, L2, ..., Ln-1, Ln.

3.2.45 panel

area of laminated layers that contains PCBs and coupons processed as a single unit

3.2.46 PCB manufacturer

entity that manufactures the PCB

3.2.47 peelable

areas of photo resist or copper that have poor adhesion to underlying substrate because of a tapered shape with a narrow dimension on one end

3.2.48 plated through-holes (PTH)

metal-plated holes drilled through all the layers used for assembly of components

3.2.49 printed circuit board (PCB)

product resulting from the process of selectively etching unwanted copper from surfaces of copper clad insulating substrates to form a desired circuitry pattern which is metal-plated and laminated

NOTE Examples of specific PCB technologies are rigid, flexible, rigid-flex, double sided, multilayer, sequential, RF and HDI PCBs

3.2.50 prepreg

sheets of partly cured, B-stage, resin with reinforcement

NOTE Examples of reinforcement are woven glass fibres and non-woven aramid fibres.

3.2.51 RF elements

conductive pattern on PCB with specific RF functionality

NOTE For example filters, combiners, splitters, couplers. RF elements do not have voltage ratings or solder connections.

3.2.52 resin starvation

region in a PCB that has an insufficient amount of resin to wet out completely the reinforcement

NOTE This is shown by low gloss, dry spots or exposed fibres.

3.2.53 review item

design feature to be included into the PCB definition dossier and reviewed during the PCB design review

3.2.54 projected peak-to-peak insulation distance

worst-case minimum thickness of dielectric material that includes thickness tolerance of the laminate core and the maximum roughness of copper surface treatment

NOTE Figure 3-2 specifies how this is measured.

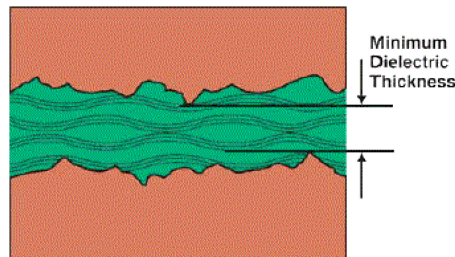


Figure 3-2: Projected peak-to-peak insulation distance

3.2.55 serialization

process of numbering of each unique PCB by the PCB manufacturer for traceability

3.2.56 sliver

pieces of photo resist or copper that have poor adhesion to underlying substrate because of the small surface area.

NOTE For example, a surface area below 0,01 mm²

3.2.57 soldering pad

conductive part intended for soldering components on the PCB

3.2.58 spacing

insulation distance

NOTE The term “gap” is synonymous with the word “spacing”, but this term is not used in the present standard.

3.2.59 stack

assembly comprising of one sequence of laminated layers

NOTE Half-stack identifies the sub-assembly.

3.2.60 test pad

pad that is dedicated for electrical testing on the PCB

3.2.61 track

conductive part routing the electrical connection between the pads

NOTE The term “line” and the term “conductive track” are synonyms with the word “track”

3.2.62 via

metal-plated hole drilled through all layers, only used for interconnection between layers

NOTE A via is not used for assembly

3.2.63 X,Y direction

orientation in the plane of the PCB, along length and width of the PCB

3.2.64 Z direction

orientation perpendicular to the plane of the PCB, along height of the PCB

3.3 Abbreviated terms

For the purposes of this document, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
AC	alternating current
AOI	automated optical inspection
BGA	ball grid array
CAD	computer aided design
CAE	computer aided engineering
CGA	column grid array
CIC	Copper – Invar - Copper
CoC	certificate of conformance
CRC	cyclic redundancy check
CTE	coefficient of thermal expansion
Cu	copper (element)
DC	direct current
DRD	document requirements definition
DWV	dielectric withstanding voltage
GND	electrical signal to ground
EMC	electromagnetic compatibility
FAI	first article inspection
FP	flat pack
FR4	type of epoxy resin for PCBs
HDI	high density interconnect
i.a.w.	in accordance with

Abbreviation	Meaning
I/O	input/output
LCC	leadless chip carrier
LF	low frequency
MRR	manufacturing readiness review
PCB	printed circuit board
PID	process identification document
ppm	parts per million (10^{-6})
PTH	plated through hole
PTFE	polytetrafluoroethylene
QFP	quad flat pack
RF	radio frequency (high frequency)
SOIC	small outline integrated circuits
SPF	single point failure
sq	square (in unit Ω/sq)
TDR	time domain reflectometry
Tg	temperature of glass transition
Th	thickness
Vcc	power supply voltage
Vrms	voltage root mean square

4

Principles

4.1 Qualified PCBs

Qualified PCBs for space application meet the following conditions:

- b. PCB is procured in conformance with requirements of ECSS-Q-ST-70-11,
- c. PCB is procured from a PCB manufacturer that is qualified in conformance with requirements of ECSS-Q-ST-70-10,
- d. the PCB technology is qualified in conformance with requirements of ECSS-Q-ST-70-10 for that PCB manufacturer,
- e. the PCB design is in conformance with the requirements of ECSS-Q-ST-70-12, and
- f. the PCB design, the manufacturing process and materials are in conformance with the PID of the PCB manufacturer.

PA requirements of space projects use this European Standard as applicable document. Based on their heritage, suppliers can propose the re-use of existing PCB designs that are “recurrent” and that are not in compliance with all design requirements of this European Standard. The possible acceptability of those cases is reviewed by the project on case by case basis. The PCB design is “recurrent” only when no changes are made in the artwork, routing, lay-out, build-up, material selection.

4.2 Manufacturing tolerances

Dimensional measurements of PCBs are “as-designed” except when explicitly mentioned “as-manufactured”.

Design values are affected by the manufacturing tolerances. The minimum value on the PCB as-manufactured equals the design value subtracted with the manufacturing tolerance. See definition of terms in Subclause 3.2.

4.3 Reliability of design

Specific design features of PCBs are recorded as Review Items in the PCB definition dossier. This is done when the design features include a higher technological complexity that can affect manufacturability or (thermal) reliability. These design features are specifically evaluated by qualification prior to inclusion in the PID.

Requirements in this European Standard generally state minimum dimensions permitted. It is good practice to use minimum dimensions only when necessary to achieve the desired functionality and to design with margin when possible. For instance, it is recommended to implement minimum insulation distance between tracks only when space limitations prevent larger insulation distance. It is recommended to implement fan out of tracks which allows for larger insulation distances where more space is available.

The robustness of the PCB can be affected when combining multiple design features at the limit of the requirement or recorded as Review Item. The PCB manufacturer and the supplier evaluate this risk during the design review and provide formal approval during the MRR. The reliability of the manufactured PCB is evaluated by inspection on representative coupons.

Design review and MRR

5.1 Overview

This clause specifies the iterative process of designing a PCB in collaboration with the PCB manufacturer and specifies associated documentation for the formal authorization for manufacture.

5.2 Documentation

- a. The supplier shall issue the PCB definition dossier in conformance with the DRD in Annex A.
- b. The supplier shall list design features as Review Items in conformance with Subclause A.2.1<7> from the DRD of the Annex A.
- c. The supplier may list other design features as Review Items .
- d. The supplier shall submit the PCB definition dossier to the PCB manufacturer for the design review.
- e. The supplier should submit to the PCB manufacturer the draft PCB definition dossier or a list of specific Review Items specified in the requirement 5.2b in the design phase, when those Review Items are at the limit of the PID capability.

NOTE Examples of Review Items that can be on the limit of PID capability are: dimensions, number of layers, maximum aspect ratio, number of sequences, material selection or a combination of these. Consultation with PCB manufacturer at this early design stage is recommended to avoid unnecessary risks. Multiple iterations can be performed to achieve an agreed PCB definition dossier.

- f. The PCB manufacturer shall review the PCB definition dossier including Review Items for compliance with the PID.
- g. As a result of the design review, the PCB manufacturer may identify to the supplier additional Review Items in the PCB definition dossier.

NOTE Review Items can exist for PCB designs even within the capability of the PID. These Review Items and methods to mitigate them are

specified in this European Standard as best practices and recommendations.

- h. The PCB manufacturer shall provide the PCB manufacturing dossier in conformance with DRD in the Annex B.
- i. The PCB manufacturer shall issue to the supplier a MRR checklist, which is part of the PCB manufacturing dossier, in conformance with the DRD in the Annex B.

NOTE An example of a MRR checklist is given in Annex G.

- j. During the MRR, supplier and PCB manufacturer shall approve the PCB manufacturing dossier, the PCB definition dossier and all Review Items.

NOTE The approvals are recorded in the MRR checklist.

- k. The MRR shall provide authorisation for manufacture to the PCB manufacturer.

6

General design and production requirements

6.1 Reliability of design

- a. The supplier shall design the PCB with margin.

NOTE This is also described in Subclause 4.3.

6.2 Choice of materials and build-up

6.2.1 Overview

For the selection of materials for PCB a number of physical properties are important, such as Tg, Young's modulus, dielectric constant, CTE, hygroscopy. Table 6-1 provides an overview of some commonly used materials and their physical properties. The CTE of the as-manufactured PCB depends on the total copper thickness, which has a CTE of about 16 ppm/K.

It is important that for the selection of the technology for the PCB design the following is taken into account:

- CTE mismatch between devices and PCB,
- moisture sensitivity of PCB function,
- interconnection constraints,
- lay-out constraints.

Rigid-flex boards can be preferred to reduce the interconnection constraints.

Polyimide and epoxy are the most commonly used materials. Polyimide has an advantage over epoxy because it is more thermally stable and outperforms epoxy in thermal cycling and assembly. At the same time, polyimide is more hygroscopic than epoxy, which affects PCB ground use and assembly. Epoxy is available with different glass transition temperatures (Tg). Higher glass transition temperature is recommended for epoxy because it provides better thermal stability. Thermal expansion of resin in Z direction below and above Tg is typically higher than expansion of copper. Therefore it is beneficial for thermal endurance to use materials with low CTE in Z direction. Flame retardants in base materials are commonly required for ground based applications but are not necessary for space based PCBs.

For high frequency performance typically PTFE based materials are used. These materials require special lamination cycles as adhesion is generally poorer compared to polyimide and epoxy.

IPC-4121 provides a comparison of various properties for core constructions as function of resin and glass type.

Table 6-1: Characteristics of some example dielectric materials for laminates

Type of material	Dielectric constant		Dissipation Factor		T _g (°C)	water absorption (%)	Volume density (g/cm ³)	CTE (ppm/K) below T _g			CTE (ppm/K) above T _g			Thermal conductivity (W/m.K)	Example
	at 1 MHz	at 10 GHz	at 1 MHz	at 10 GHz				X	Y	Z	X	Y	Z		
Epoxy HTg	4,24	3,92	0,015	-	180	0,15	-	13 - 14	13 - 14	45	14 - 17	14 - 17	230	0,4	370 HR (Isola)
	4,24	3,92	0,015	-	170	0,15	-	13 - 14	13 - 14	45	14 - 17	14 - 17	230	0,4	IS420 (Isola)
Polyimide / Glass	4,2	-	0,01	-	> 250	0,26	1,6	16	16	51	-	-	158	0,2	35N (Arlon)
	4,2	-	0,01	-	250	0,27	1,6	16	16	55	-	-	149	0,2	85N (Arlon)
Polyimide / Aramid	3,6	-	0,014	-	250	0,6	1,37	6 - 9	6 - 9	93	-	-	279	0,2	85NT (Arlon)
Polyimide flex laminate	3,4	3,3	0,003	-	220	0,8	-	25	25	-	-	-	-	-	AP (DuPont)
Ceramic reinforced PTFE	-	2,94	-	0,0012	-	0,02	2,1	16	16	24	-	-	-	0,6	RT/Duroid 6002 (Rogers)
Hydrocarbon and ceramic reinforced glass	-	3,38	-	0,0027	> 280	0,06	1,79	11	14	46	-	-	-	0,71	RO 4003 (Rogers)
Glass reinforced PTFE	2,20	2,20	0,0004	0,0009	-	0,02	2,2	31	48	237	-	-	-	0,2	RT/Duroid 5880 (Rogers)
Ceramic thermoset	-	9,8	-	0,002	-	0,16	2,77	19	19	20	-	-	-	0,76	TMM10i (Rogers)

6.2.2 Material selection

- a. Selection of the base laminate materials shall be performed in compliance with the requirements from the Subclause 5.2.1 of the ECSS-Q-ST-70-11.
- b. The material selection for all types of PCBs shall be in compliance with the requirements from the clauses 7.1 to 7.6 of the ECSS-Q-ST-70-11.

NOTE Examples of types of PCBs are: single sided, double sided, multilayer, sequential, rigid, rigid-flex, flexible, sculptured flex, HDI, RF.

- c. The as-manufactured PCB shall be in conformance with the outgassing requirements of the Subclause 5.5.3 from the ECSS-Q-ST-70-02 or project specific requirements on cleanliness.

NOTE The outgassing requirements are CVCM<0,1% and RML<1,0%.

6.3 Selection of the PCB manufacturer

- a. The supplier shall procure PCBs from a PCB manufacturer with a qualification approval for an identified technology in conformance with the requirements from the Clause 5 to Clause 9 of the ECSS-Q-ST-70-10.
- b. The supplier shall procure the PCBs in conformance with the requirements from the Clause 5 to Clause 7 of the ECSS-Q-ST-70-11.

6.4 Traceability and marking

- a. The PCB shall be marked with part number and revision number from the PCB definition dossier as given by the supplier.
- b. All individual PCBs within the panel shall be identified by a serial number.
- c. The serialization of the PCB shall be established before the start of the fabrication.
- d. The serial number shall identify the position of the PCB on the panel.
- e. The serial number methodology shall be identified in the PID of the PCB manufacturer.

7

Rigid PCBs

7.1 PCB build-up

7.1.1 General

- a. The build-up of the PCB and each sub-assembly should be symmetric.

NOTE This is done to avoid warp and twist.
- b. The supplier shall record asymmetric build-up as a Review Item in the PCB definition dossier.

NOTE The build-up includes the copper thickness and its distribution.

- c. In case Molybdenum or CIC layers are used, they shall be included in the build-up and recorded as a Review Item in the PCB definition dossier.

NOTE 1 Specific requirements for the build-up are listed in the PCB definition dossier in A.2.1<5>a.3(h).

NOTE 2 On external layers, copper clad laminate typically achieves better peel strength whereas copper foil achieves better registration.

7.1.2 Copper styles

- a. The thickness of the copper cladding on both sides of the laminate should be equal except on outer layers of the PCB or half-stack.

NOTE Equal copper thickness is needed when laminate is etched in same process steps, as is the case for internal layers. The exception on outer layers is made because each side is etched in different process steps and because thin copper on external layers decreases the total thickness after plating.

- b. In case the thickness of the copper cladding on the laminate is asymmetric, this asymmetric build-up of the PCB shall be recorded as a Review Item in the PCB definition dossier.

NOTE 17/70 copper thickness is more risky than 17/35 or 35/70 copper thickness. The presence of fine pitch tracks in combination with asymmetric copper further increases the difficulty to process.

- c. Except the case specified in the requirement 11.4.1e, the external and internal layers shall use basic copper thickness 70 μm , 35 μm or 17 μm .

NOTE 1 Copper layers can be implemented as copper clad laminate or as separate copper foils.

NOTE 2 Requirement 11.4.1e specifies microvia layers on HDI PCBS.

- d. Copper distribution within a layer should be homogeneous.

NOTE This is done to ensure even pressure distribution during lamination, which can cause filling voids, cracks or glass compression.

- e. Balancing of copper should be performed by including dummy non-functional copper.

NOTE This is more important for partial planes on thick copper layers such as 70 μm .

- f. Signal tracks should not be routed on copper plane layers.

- g. In case the total as-designed thickness of copper is above 700 μm , this shall be recorded as a Review Item in the PCB definition dossier.

NOTE High layer count in combination with thick copper layers can have significant impact on manufacturability and long-term reliability.

- h. Copper quality "HTE" shall be used for copper clad laminate.

NOTE Type HTE can be procured in conformance with IPC-4562 Type E, grade 3.

- i. Copper quality "JTC" or "HTE" shall be used for copper foils.

- j. The values from the Table 7-1 should be used in the design calculations for copper foil thickness.

NOTE The values indicated in Table 7-1 are minimum as-manufactured thickness for the specified as-designed foil thickness.

Table 7-1: As-designed versus as-manufactured copper foil thickness

As-designed foil thickness (μm)	Minimum as-manufactured thickness for non-plated inner layers (μm)	Minimum as-manufactured thickness for plated layers with $\geq 25 \mu\text{m}$ plating (μm)
9	6	31
12	9	34
17	11	38
35	25	53
70	56	84

7.1.3 Dielectric thickness

- A minimum of two sheets of prepreg shall be used for insulation between two layers.
- A minimum of two sheets of glass should be used in glass-reinforced laminates.
- In case a single sheet of glass is used in a glass-reinforced laminate it shall be recorded as Review Item in the PCB definition dossier.

NOTE Two sheets of glass reinforcement are specified to mitigate the risk of reduced insulation caused by contamination. This is also specified for laminates for class 3/A in accordance with IPC-6012 Appendix A. In case a single reinforcement in laminate is used, it is recommended to implement other means to mitigate the risk of contamination in laminate. IPC-4121 provides various properties, such as resin-to-glass ratio, for core laminate constructions.

- The insulation distance as-designed between two layers in rigid laminate or prepreg in Z direction should be in conformance with the values from Table 13-7.

NOTE This table specifies a minimum distance of 100 μm .

- Except the case specified in the 11.4.1h, the insulation distance as-manufactured between two layers in rigid laminate or prepreg in Z direction shall be in conformance with the values from Table 13-7.

NOTE 1 This table specifies a minimum projected peak-to-peak distance of 70 μm .

NOTE 2 Requirement 11.4.1h specifies microvia layers on HDI PCBs..

- f. Double-sided copper clad laminate with a thickness as-designed of 4 mil ($\sim 100\ \mu\text{m}$) shall not be used unless:
1. the voltage is less than 30V,
 2. the copper foil thickness on both sides of the laminate is 17 μm or 35 μm ,
 3. the laminate batch is screened by the PCB manufacturer to have a nominal thickness of the etched laminate of $\geq 3,8$ mil,
 4. the insulation distance as-manufactured is verified by the PCB manufacturer to be in compliance with requirement 7.1.3e, and
 5. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 Requirement 7.1.3f.1 is in compliance with the values from Table 13-3.

NOTE 2 The nominal thickness of etched laminate from the requirement 7.1.3f.3 can be read from the CoC. However, this does not indicate worst-case thickness as mentioned in the requirement 7.1.3e. Therefore the use of 4 mil laminate on the lower end of the tolerance between 3,5 mil and 3,8 mil is prohibited by this requirement.

NOTE 3 The precautions specified in this requirement are defined to prevent a worst-case insulation value of less than 70 μm due to high tolerances with rough copper surface treatment as indicated in Table 7-2.

- g. Double-sided copper clad laminate with a thickness as-designed of 5 mil ($\sim 125\ \mu\text{m}$) shall not be used above 30 V unless:
1. the thickness of laminate as-manufactured is in conformance with the Table 13-3,
 2. the laminate batch is screened by the PCB manufacturer to have a nominal thickness of the etched laminate of $\geq 4,8$ mil,
 3. the as-manufactured insulation distance is verified by the PCB manufacturer to be in compliance with requirement 7.1.3g.1,
 4. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 The thickness value of the requirement 7.1.3g.1 is $\geq 100\ \mu\text{m}$.

NOTE 2 This value specified in the requirement 7.1.3g.2 can be read from the CoC. It does not indicate worst-case thickness as mentioned in the requirement 7.1.3g.1. This prohibits the use of 5 mil laminate on the lower end of the tolerance between 4,5 mil and 4,8 mil.

NOTE 3 Precautions specified in this requirement are defined to prevent a worst-case insulation value of less than 100 μm due to high tolerances with rough copper surface treatment as indicated in Table 7-2.

- h. For insulation distance in Z direction of a laminate, the minimum projected peak-to-peak insulation distance specified in the requirement 7.1.3i shall be used.
- i. The minimum projected peak-to-peak insulation distance shall include the thickness tolerance of the laminate core and the maximum roughness of copper surface treatment.

NOTE Projected peak-to-peak insulation distance is specified in Figure 3-1 of IPC-4101.

- j. If available, laminates should be class D in conformance with requirements from the IPC-4101 except the cases specified in the requirement 7.1.3k.

NOTE 1 Class D guarantees a minimum projected peak-to-peak insulation distance.

NOTE 2 Typically used materials can be unavailable in class D even though this specification exists.

- k. In case other laminate classes are used, the PCB manufacturer shall calculate minimum projected peak-to-peak insulation distance in conformance with requirement 7.1.3i.

NOTE An example of this is shown in Table 7-2 for class C laminate and commonly used copper profiles.

- l. The PCB manufacturer shall define laminate and prepreg styles and amount to achieve the insulation distances as designed by the supplier in conformance with requirements of the Subclause 13.8.

NOTE The supplier is responsible to design insulation distances required to meet design voltages in conformance with the requirement 13.8.2c.

Table 7-2: Example of worst case as-manufactured insulation distance for laminate with double-sided copper cladding

As-designed laminate thickness	Laminate thickness tolerance i.a.w. IPC4101 Table3.7 class C.	Copper foil 18 or 35 μm		Copper foil 70 μm	
		"Very low profile" i.a.w. IPC4562 Table3.1	Worst-case as-manufactured projected peak-to-peak insulation distance	"Low profile" i.a.w. IPC4562 Table3.1	Worst-case as-manufactured projected peak-to-peak insulation distance
101,6 μm (4 mil)	$\pm 13 \mu\text{m}$	5,1 μm	78,4 μm	10,2 μm	68,2 μm
127 μm (5 mil)	$\pm 18 \mu\text{m}$	5,1 μm	98,8 μm	10,2 μm	88,6 μm
152 μm (6 mil)	$\pm 18 \mu\text{m}$	5,1 μm	123,8 μm	10,2 μm	113,6 μm
203 μm (8 mil)	$\pm 25 \mu\text{m}$	5,1 μm	167,8 μm	10,2 μm	157,6 μm
254 μm (10 mil)	$\pm 25 \mu\text{m}$	5,1 μm	218,8 μm	10,2 μm	208,6 μm

7.2 PCB dimension

The maximum dimensions of the PCB depend on the panel dimensions used and qualified by the PCB manufacturer. A typical large panel size is 45x60 cm (18x24 inch). Not all surface area of the panel is available for the PCB design as mandatory coupons are included in the panel.

7.3 Thickness of PCB

7.3.1 General

- a. PCB thickness shall be measured from bottom insulation to top insulation.

NOTE 1 The manufacturing tolerance is provided by the PCB manufacturer.

NOTE 2 It is important to include the manufacturing tolerance of 10% in conformance with the requirement 7.6.b.2 from the ECSS-Q-ST-70-11.

NOTE 3 Tolerances on individual copper clad laminate of 100 μm is about $\pm 18 \%$. Tolerance on the total PCB stack is typically lower.

NOTE 4 Specific requirements for maximum thickness over metal surface finish are specified in the PCB definition dossier.

7.3.2 Polyimide PCB

- a. The thickness as-manufactured of a rigid and rigid-flex polyimide PCB shall be $\leq 4,0$ mm.
- b. The as-designed thickness of a rigid and rigid-flex polyimide PCB should be $\leq 3,6$ mm, except the case specified in the requirement 7.3.2c.
- c. The as-designed thickness of a rigid and rigid-flex polyimide PCB may be $> 3,6$ mm in case:
 - 1. the thickness as-manufactured is in conformance with requirement 7.3.2a,
 - 2. the manufacturing tolerance is $< 10\%$, and
 - 3. it is recorded as a Review Item in the PCB definition dossier.

7.3.3 Epoxy PCB

- a. The thickness as-manufactured of a rigid and rigid-flex epoxy PCB shall be $\leq 2,4$ mm.
- b. The as-designed thickness of a rigid and rigid-flex epoxy PCB should be $\leq 2,2$ mm, except the case specified in the requirement 7.3.3c.
- c. The as-designed thickness of a rigid and rigid-flex epoxy PCB may be $> 2,2$ mm in case:
 - 1. the thickness as-manufactured is in conformance with requirement 7.3.3a,
 - 2. the manufacturing tolerance is $< 10\%$, and
 - 3. it is recorded as a Review Item in the PCB definition dossier.

7.3.4 Number of copper layers in PCB

- a. Number of copper layers for polyimide PCB shall be ≤ 26 .
- b. Number of copper layers for epoxy PCB shall be ≤ 20 .

7.3.5 Aspect ratio of vias

- a. Except the case specified in the requirement 11.5.6a, the aspect ratio of vias on a rigid and rigid-flex PCB shall be ≤ 7 .

NOTE 1 There is no additional requirement for the minimum diameter of plated via in case the diameter conforms to the aspect ratio of ≤ 7 .

NOTE 2 Requirement 11.5.6a specifies aspect ratio for AAD with 1 mm pitch on HDI PCBs.

7.4 Track width and spacing

7.4.1 General

- a. A verification should be performed to prevent non-functional changes of direction of tracks.

NOTE Some automated routing software can cause unnecessary changes of direction that have no function.

7.4.2 Manufacturing tolerances for width and spacing

- a. The relative manufacturing tolerances on the track width and spacing of internal and external layers shall be as specified in Table 7-3.
- b. The maximum absolute manufacturing tolerances on the track width and spacing of internal and external layers shall be as specified in Table 7-3.

NOTE 1 For example, an internal track width of 400 μm on 35 μm copper thickness has a relative tolerance of $\pm 20\%$, i.e. 80 μm , which is limited by the maximum absolute tolerance of 50 μm .

NOTE 2 The tolerance applies to as-designed dimensions. For example, a spacing as-designed of 200 μm with a tolerance of $\pm 20\%$ results in a spacing as-manufactured of 160 μm - 240 μm . Typically, the minimum spacing of 160 μm is important for PCB design.

- c. The use of planarization, copper reduction or surface preparation processes shall be excluded in the definition of the total copper thickness.

NOTE 1 Plating of sequential half stacks can be done with different plating methods, like panel plating, selective pattern plating or a combination and can include copper surface reduction processes to reduce copper surface thickness and give best options for fine pitch etching.

NOTE 2 The plated copper thickness as-designed is 25 μm . This can be a thicker layer as-manufactured.

Table 7-3: Tolerance on track width and spacing of internal and external layers

Thickness category [μm]	Basic Cu [μm]	Plated Cu [μm]	Total Cu thickness [μm]	Relative tolerance on track width and spacing	Maximum absolute tolerance on track width and spacing
Th≤17	≤ 17	0	≤ 17	± 20 % FOR 11.5.5a.5: -10% to +20%	± 30 μm
17<Th≤60	≤ 17	1x25	≤ 42	± 20 %	± 50 μm
	35	0	35		
	35	1x25	60		
60<Th≤70	≤ 17	2x25	≤ 67		± 50 μm
	70	0	70		
70<Th≤95	35	2x25	85		± 70 μm
	70	1x25	95		
Note: Explanation of "FOR" is given in Table 13-1.					

7.4.3 External layers

- a. The as-manufactured track width and spacing as a function of copper thickness for external layers of rigid PCB shall be in conformance with the values specified in the Table 7-4.
- b. The as-designed track width and spacing for external layers of rigid PCB should be in conformance with the values specified in the Table 13-7 except the case specified in the requirement 7.4.3c.
- c. In case the as-designed track width and spacing for external layers of rigid PCB is less than the values specified in the requirement 7.4.3b, the following conditions shall be met:
 1. the manufacturing tolerances as specified in the PID are smaller than as specified in Table 7-3,
 2. the as-manufactured dimensions specified in Table 7-4 and Table 13-7 are met, and
 3. it is recorded as a Review Item in the PCB definition dossier.
- d. Tracks should not be routed on external layers.
- e. In case tracks are routed on external layers they should not be routed under components.
- f. The basic copper foil thickness of fine pitch shall be 17 μm.

- g. Fine pitch track width and spacing may be used in case:
1. fine pitch tracks are used to route to the footprint of a fine pitch component,
 2. the length of fine pitch tracks is ≤ 20 mm from the solder pad,
 3. conformal coating is applied on fine pitch tracks or pads in conformance with the requirement 13.8.4b,
 4. the voltage is ≤ 30 V, and
 5. it is recorded as a Review Item in the PCB definition dossier.

NOTE A long fine pitch track can cause solder pearls.

- h. Spacing and width of pads shall be in conformance with the requirements for tracks specified in 7.4.3a, 7.4.3b, 7.4.3c, 7.4.3f and 7.4.3g.

Table 7-4: Minimum as-manufactured track width and spacing for external layers as a function of copper thickness

Basic Cu [μ m]	Plated Cu [μ m]	Thickness category [μ m]	Pitch	As-manufactured	
				width [μ m]	spacing [μ m]
17	1x 25	17<Th $\leq$ 60	fine/normal	120/160	120/160
17	2x 25	60<Th $\leq$ 70	fine/normal	120/160	120/160
35	1x25	17<Th $\leq$ 60	normal	160	160
35	2x25	70<Th $\leq$ 95	normal	240	240
70	1x25	70<Th $\leq$ 95	normal	240	240

7.4.4 Normal pitch tracks on internal layers

- a. The as-manufactured track width and spacing as a function of copper thickness for internal layers of rigid PCB shall be in conformance with the values specified in the Table 7-5.
- b. The as-designed track width and spacing for internal layers of rigid PCB should be in conformance with the values specified in the Table 13-7 except the case specified in the requirement 7.4.4c.
- c. In case the as-designed track width and spacing for internal layers of rigid PCB is less than the values specified in the requirement 7.4.4b, the following conditions shall be met:
 1. the manufacturing tolerances as specified in the PID are smaller than as specified in Table 7-3,
 2. the as-manufactured dimensions specified in Table 7-5 and Table 13-7 are met, and
 3. it is recorded as a Review Item in the PCB definition dossier.
- d. The thickness category of copper on internal layers shall be as specified in Table 7-3.

**Table 7-5: Minimum as-manufactured track width and spacing for internal layers
as a function of copper thickness**

Thickness category [μm]	Pitch	As-manufactured	
		width [μm]	spacing [μm]
Th≤17	fine/normal	80/104	96/104
17<Th≤60	normal	120	120
60<Th≤70	normal	160	160
70<Th≤95	normal	240	240

7.4.5 Fine pitch tracks on internal layers

- a. Except the case specified in the requirement 11.5.5a, the track width and spacing for fine pitch on internal layers shall be in conformance with the as-manufactured dimensions specified in Table 7-5.

NOTE Requirement 11.5.5a specifies track width and spacing for impedance controlled routing to AAD with 1 mm pitch on HDI PCBs .

- b. In case fine pitch tracks are used, this shall be recorded as a Review Item in the PCB definition dossier.
- c. Fine pitch shall be limited to the functionality of impedance control or signal routing to AAD.
- d. Fine pitch tracks shall be limited to ≤ 30 V.
- e. For routing to AAD, fine pitch tracks shall fan out to normal pitch as soon as they are outside the AAD footprint.
- f. In case no other circuitry is adjacent that requires the use of fine pitch, the routing of fine pitch tracks shall increase the insulation distance and track width as specified for normal pitch in the Table 7-5.

NOTE 1 CAD software can implement different minimum insulation distances and track widths in areas with different space available.

NOTE 2 The Figure 7-1 shows examples of possible improvements in routing.

- g. Fine pitch shall be manufactured by using 17 μm basic copper thickness without plating steps.

7.4.6 Routing to AAD footprint on internal layers

- a. Tracks in AAD footprint shall be placed equidistant between pads to increase insulation distance to both pads.

NOTE See example of nonconformance indicated by blue arrow in Figure 7-1.

- b. Tracks shall exit from AAD footprint before changing direction to keep the insulation distance to the pad in compliance with normal pitch as specified in Table 7-5.

NOTE See example of nonconformance indicated by green arrow in Figure 7-1.

- c. Widening of tracks shall occur close to AAD footprint to provide a wider track where no other circuitry is adjacent that requires the use of fine pitch.

NOTE See example of nonconformance indicated by yellow arrow in Figure 7-1.

- d. Changing of direction of track should be in compliance with the requirement 7.4.1a.

NOTE See example of nonconformance indicated by white arrow in Figure 7-1

- e. Pads of AAD footprint may be designed with teardrop reinforcement

NOTE Pads in Figure 7-1 are not designed with teardrop reinforcement.

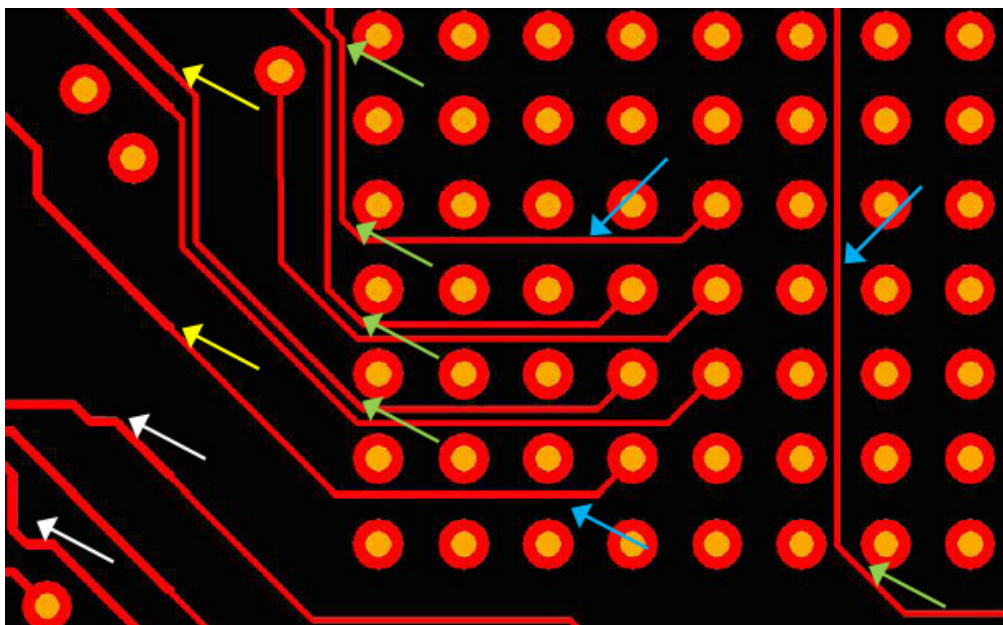


Figure 7-1: Example of automated fine pitch routing and possible improvements

7.5 Pad design

7.5.1 Non-functional pad removal

- a. Non-functional pads shall be present on all layers, except two cases specified in the requirement 7.5.1b.

NOTE The presence of non-functional pads reduce the risk of hole wall pull-away and reduce the risk of cracks in resin-rich areas.

- b. Non-functional pads may be removed:
1. when the presence of the pads degrade the electrical performance, they can be removed by the supplier, or
 2. to prevent high pressure area during lamination that cause resin starvation in the prepreg, the pads can be removed by the PCB manufacturer.

NOTE Removal of non-functional pads is approved by supplier and PCB manufacturer during MRR in conformance with the requirement 7.5.1c.6

- c. When non-functional pads are removed as specified in the requirement 7.5.1b, the following conditions shall be met:
1. non-functional pads are present on all copper plane layers,
 2. non-functional pads are present on flex laminate,
 3. maximum half of the non-functional pads in the pad stack are removed,
 4. non-functional pads are removed on maximum two consecutive layers,
 5. non-functional pads are removed on maximum one side of a laminate, and
 6. it is recorded as a Review Item in the PCB definition dossier.
- d. Non-functional pads should not be removed on layer 2 and n-1.

7.5.2 Pad dimensions

- a. Except the case specified in the requirement 11.5.2a, the annular ring as-manufactured on internal layers shall be in conformance with the requirement 9.5.b.15(d) of ECSS-Q-ST-70-10.

NOTE 1 This requirement specifies 50 µm.

NOTE 2 Requirement 11.5.2a specifies annular ring of internal pads for fine pitch footprint on HDI PCBs.

- b. The annular ring as-manufactured on component side of external layers shall be in conformance with the requirement 9.5.b.15(b) of ECSS-Q-ST-70-10.

NOTE This requirement specifies 100 µm.

- c. Except the case specified in the requirement 7.5.3b.2, the annular ring as-manufactured on solder side of external layers shall be in conformance with the requirement 9.5.b.15(a) of ECSS-Q-ST-70-10.

NOTE This requirement specifies 200 μm

- d. For component holes on solder side the minimum diameter of external pads should be the diameter of as-manufactured hole plus $\geq 0,8 \text{ mm}$.
- e. For component holes on solder side the minimum diameter of external pads may be the diameter of as-manufactured hole plus $\geq 0,6 \text{ mm}$ in case:
 - 1. the as-manufactured annular ring as specified in the requirement 7.5.2c,
 - 2. the component holes are a footprint for a nano D connector,
 - 3. it is recorded as Review Item in the PCB definition dossier.
- f. For via holes and component holes on component side the diameter of external pads should be the diameter of as-manufactured hole plus $\geq 0,6 \text{ mm}$.
- g. For via holes and component holes on component side the diameter of external pads may be the diameter of as-manufactured hole plus $\geq 0,5 \text{ mm}$ in case:
 - 1. the as-manufactured annular ring as specified in the requirement 7.5.2b, and.
 - 2. it is recorded as a Review Item in the PCB definition dossier.
- h. The diameter of internal pads should be the diameter of drilled hole plus $\geq 0,3 \text{ mm}$.

NOTE 1 The drilled diameter is typically 0,2 mm larger than the as-manufactured minimum hole diameter.

NOTE 2 It is important to consider the number of drilling and lamination sequences and the PCB manufacturing tolerances for the design of the diameter of the pads.

- i. The diameter of pads may be the diameter of the drilled hole plus $< 0,3 \text{ mm}$ in case this is recorded as a Review Item in the PCB definition dossier.

NOTE Tear drop reinforcement of pads to tracks can be used for a more robust design and to mitigate the risk of a smaller designed diameter.

7.5.3 Non-circular external pads

- a. Pads for component holes on external layers shall be circular, except cases specified in the requirement 7.5.3b.
- b. Non-circular pads may be used for component holes, in case the following conditions are met:
 1. the surface area of the oblong pad is not smaller than the surface area of the circular pad as specified in the requirements from the Subclause 7.5.2,
 2. the oblong pad meets the requirement for annular ring of 100 μm as-manufactured, and
 3. it is recorded as a Review Item in the PCB definition dossier.

NOTE 1 For the requirement 7.5.3b.1 $A_{(\text{oblong})}$ in Figure 7-2 is the surface area of the oblong pad and $A_{(\text{circular})}$ in Figure 7-2 is the surface area of a circular pad

NOTE 2 For the requirement 7.5.3b.2 see Annular ring_(oblong) in Figure 7-2

NOTE 3 The design in the requirement 7.5.3b.2 is a deviation of the requirement 7.5.2c (and ECSS-Q-ST-70-10 requirement 9.5b.15.a) of 200 μm annular ring for pads on solder side (see Annular ring_(circular) in Figure 7-2) in one direction, compensated by a larger annular ring in the other direction.

NOTE 4 Other non-circular pad designs are possible and typically used on external layers for AAD and SMT components. Dog-bone shapes or key hole shapes can be used for the verification of solder joint quality or to prevent thermal stress on (blind or micro) vias.

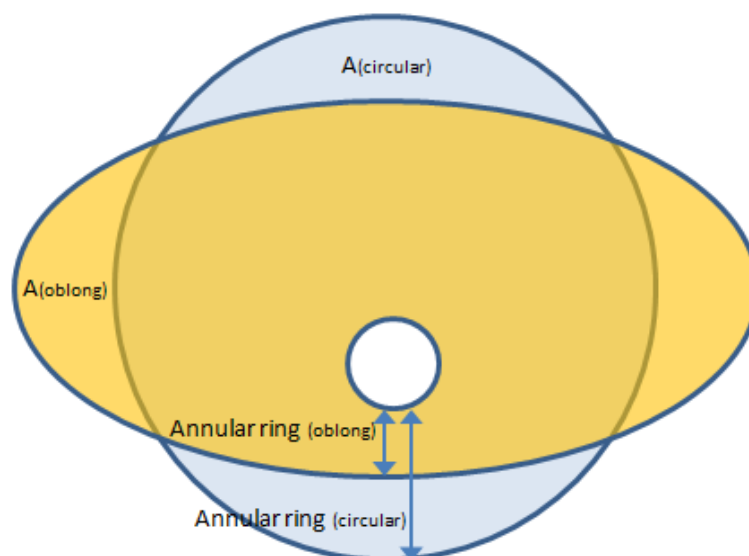


Figure 7-2: Comparison between circular and oblong pads showing annular ring and the centre of the hole misregistered with the centre of the pad