



BSI Standards Publication

Space product assurance – Qualification and Procurement of printed circuit boards

National foreword

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Raumfahrtproduktsicherung - Qualifizierung und
Beschaffung von Leiterplatten

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Table of contents

European Foreword	13
Introduction	14
1 Scope	15
2 Normative references	16
3 Terms, definitions and abbreviated terms	18
3.1 Terms from other standards.....	18
3.2 Terms specific to the present standard	19
3.3 Abbreviated terms.....	27
3.4 Nomenclature	29
4 Principles	30
4.1 General.....	30
4.2 Roles	30
4.3 References to acceptance criteria.....	30
5 QA for qualification	31
5.1 Qualified PCBs	31
5.2 Ceramic PCB technology	32
5.3 Flexible PCB	32
5.3.1 General	32
5.3.2 Qualification of flexible PCB	32
5.4 Qualification process	34
5.5 Request for qualification	34
5.6 Quality standards.....	35
5.7 Description of qualification vehicle	35
5.8 Evaluation.....	36
5.9 Audit	36
5.10 Qualification test programme	38
5.11 PID	38
5.12 Qualification approval	39
5.13 Process change.....	39

5.14	QA report.....	40
5.15	Qualification renewal	40
5.16	Nonconformances during qualification renewal	41
6	QA for manufacture and procurement.....	43
6.1	Overview	43
6.2	Procurement process.....	43
6.2.1	Overview	43
6.2.2	Procurement specification	44
6.2.3	Quotation	44
6.2.4	Purchase order	45
6.2.5	Design review (DR).....	45
6.2.6	MRR	45
6.3	Final and in-process inspection.....	46
6.4	Quality records for manufacture and procurement	47
6.5	Control of materials and chemistry.....	48
6.6	Control of plating chemistry	49
6.7	Cleanliness of PCB processes.....	50
6.7.1	Overview	50
6.7.2	Cleanliness control.....	51
6.8	Traceability	52
6.9	Operator and inspector training.....	53
6.10	Repair of bare PCBs.....	54
6.10.1	Overview	54
6.10.2	General	54
6.11	Packaging.....	56
6.12	Storage and baking of PCB and coupons	57
6.13	Shelf-life and relife testing.....	57
6.14	QA for PCB procurement in space projects.....	58
7	Test and inspection for qualification	61
7.1	Overview	61
7.2	Test selection for qualification activities	64
7.3	Initial qualification of PCB manufacturer	68
7.4	Initial qualification of PCB technology	68
7.5	Qualification renewal	68
7.6	Delta qualification	68
7.7	Project qualification and RFA.....	69
7.7.1	Overview	69

7.7.2	Requirements for project qualification and RFA	69
8	Test and inspection for procurement	74
8.1	Outgoing inspection on PCB	74
8.2	Outgoing inspection on coupons	75
8.2.1	Overview	75
8.2.2	Configuration of coupons for plated holes	78
8.2.3	Configuration of dedicated coupons	81
8.2.4	Evaluation of coupons	82
8.2.5	Delivery of coupons, microsections and spare coupons	84
8.3	Reporting of outgoing inspection and delivery	85
8.4	Incoming inspection by procurement authority	85
8.5	FAI on PCB by microsectioning	86
9	Test descriptions	88
9.1	Overview	88
9.2	Additional tests	88
9.2.1	Cleanliness	88
9.2.2	Bake-out	88
9.2.3	Plated copper tensile strength and elongation	89
9.2.4	Steam ageing	89
9.3	Group 1 – Visual inspection and non-destructive tests	90
9.3.1	Visual inspection - general	90
9.3.2	Visual inspection for qualitative aspects	90
9.3.3	Visual inspection for dimensional verification	90
9.3.4	Impedance test	94
9.3.5	Dielectric constant and loss tangent	94
9.3.6	Cleanliness	94
9.3.7	High resistance electrical test	95
9.3.8	Continuity test	97
9.4	Group 2 - Miscellaneous tests	99
9.4.1	Overview	99
9.4.2	Peel strength	100
9.4.3	Flexural fatigue	101
9.4.4	Bending test	102
9.4.5	Coating adhesion – tape test	103
9.4.6	Analysis of tin-lead coating	104
9.4.7	Outgassing	104
9.4.8	Thermal analysis	105

9.4.9	Flammability.....	105
9.4.10	Offgassing.....	106
9.4.11	Solderability	106
9.5	Group 3 – Thermal stress and as-received	110
9.5.1	Overview.....	110
9.5.2	Microsectioning	110
9.5.3	Solder bath float.....	115
9.5.4	Rework simulation.....	115
9.5.5	Interconnect stress test (IST)	117
9.6	Group 4 – Assembly and life test - extended.....	124
9.6.1	Overview	124
9.6.2	Test flow for group 4	124
9.6.3	Insulation resistance	126
9.6.4	Dielectric withstanding voltage (DWV).....	127
9.7	Group 5 – ECM tests	128
9.7.1	Overview.....	128
9.7.2	Temperature, Humidity, Bias (THB)	128
9.7.3	Conductive Anodic Filament (CAF)	134
9.8	Group 6 – Assembly and life test - short	140
9.8.1	Overview	140
9.8.2	Test flow for group 6	140
9.8.3	Reflow simulation.....	141
9.8.4	Thermal cycling.....	141
10	Acceptance criteria	143
10.1	Overview	143
10.2	Inspection by microsectioning for dimensional verification	143
10.3	Inspection by microsectioning for qualitative aspects.....	164
10.4	Visual inspection.....	194
10.5	Visual inspection of sculptured flex PCB.....	210
10.6	Additional requirement to the tables.....	229
10.6.1	Annular ring.....	229
10.6.2	Pad lift and associated laminate cracks.....	230
10.6.3	Miscellaneous	232
Annex A	(normative) Qualification letter – DRD	235
Annex B	(normative) CoC for PCB – DRD	236
Annex C	(normative) Qualification test report – DRD	250

Annex D (normative) Process Identification Document (PID) for PCB manufacturing – DRD.....	251
Annex E (normative) Process change notice (PCN) – DRD	254
Annex F (normative) QA report – DRD	255
Annex G (normative) PCB approval sheet – DRD	256
Annex H (informative) Example of plated-through hole microsection	261
Annex I (informative) Cleanliness requirements for laminate and prepreg.....	262
Annex J (informative) Example qualification programme.....	265
Bibliography.....	268

Figures

Figure 3-1: Example of material supplier treatment side of foil (white arrows) and PCB manufacturer treatment side of foil (opposite side)	25
Figure 7-1: Test flow for qualification	62
Figure 8-1: Flow for preparation, test and inspection of procurement coupons	78
Figure 8-2: Example of Bn coupon with 3 holes per drilling sequence	79
Figure 8-3: Example of placement of coupons and PCB in usable area of manufacturing panel.....	80
Figure 8-4: Example of vias manufactured at different plating and drilling sequences	81
Figure 8-5: Example of target quality of microsection of rigid-flex interface with UV fluorescent resin and polarised light	84
Figure 9-1: Conductor width (w) measured at the foot as seen in a cross-section.	91
Figure 9-2: Warp	92
Figure 9-3: Twist.....	93
Figure 9-4: Horizontal adjacency on layer Ln and vertical adjacency on the layers above and below.	97
Figure 9-5: Midpoint classification	97
Figure 9-6: Setting of test point assignments. The numbers 1 to 7 correspond to the conditions of requirement 9.3.8.2g.	99
Figure 9-7: Example of target quality of microsection of innerlayer (top) and knee of the hole (bottom), as-polished (left) and after micro-etch (right).	113
Figure 9-8: Examples of inadequate quality of microsection showing in the top image inadequate polishing, leaving scratches on surface, in the middle image over-etched sample and in the bottom image inadequate lighting, revealing no detail on metallisation, nor on laminate by transparency.....	114
Figure 9-9: Examples of barrel cracks after IST testing showing a nominal crack size (left) and a large crack filled with SnPb (right)	123
Figure 9-10: THB test pattern	130

Figure 9-11: Build-up for THB test vehicle	130
Figure 9-12: Insulation resistance during THB Ambient (until sample nr 1000) and THB ECM showing continuous breach of insulation on 4 patterns in the lower graph. The top graph shows stable insulation.	133
Figure 9-13: Horizontal microsection showing fibre contamination on tracks in prepreg resin causing breach of insulation.	133
Figure 9-14: Lay-out of CAF pattern	137
Figure 9-15: Schematic for CAF growth.....	137
Figure 10-1: Annular ring internal	145
Figure 10-2: Annular ring external	146
Figure 10-3: Copper foil thickness	147
Figure 10-4: Three measurements of copper plating thickness at locations that are at 25 %, 50 % and 75 % of the height of the hole	149
Figure 10-5: Measurement “average on resin” is performed on zone A. Measurement “on any local thin areas on resin or glass” is performed on Zone B	149
Figure 10-6: Glass fibre protrusion in case of negative etchback (left) and positive etchback (right)	150
Figure 10-7: Example of negative etchback (left) and approximately neutral etchback (right)	150
Figure 10-8: Wicking is measured from resin of hole wall (red arrows). In case it exceeds the annular ring, the insulation distance to adjacent circuitry (blue arrow) can be reduced.	151
Figure 10-9: Example of wicking.....	151
Figure 10-10: Wrap target condition	152
Figure 10-11: Wrap thickness below requirement, not acceptable.....	152
Figure 10-12: Projected-peak-to-peak insulation	153
Figure 10-13: Example of glass compression	153
Figure 10-14: Microvia insulation.....	154
Figure 10-15: Penetration of capture pad for μ via, not acceptable.....	154
Figure 10-16: Microvia aspect ratio, $X \geq Z$	155
Figure 10-17: Dimple in microvia	155
Figure 10-18: ICD on capture pad (pictures are unetched).....	155
Figure 10-19: Microvia plating, target condition	156
Figure 10-20: Example of void in microvia plating.....	156
Figure 10-21: Tin-lead thickness in PTH schematic (left) and a typical microsection (right)	158
Figure 10-22: Tin-lead thickness on PTH corner – target thickness (left), coverage of less than 1 μ m (middle), absence of SnPb on IMC (right)	158
Figure 10-23: Tin-lead thickness on pad.....	158
Figure 10-24: Undercut.....	161
Figure 10-25: Example of spurious copper	161

Figure 10-26: Overhang of electrolytic Au	162
Figure 10-27: Example of dimensional verification of rigid-flex interface.....	163
Figure 10-28: Examples of acceptable voids	167
Figure 10-29: Examples of unacceptable voids	167
Figure 10-30: Examples of separation between hole wall and resin inside blind via	167
Figure 10-31: Example of acceptable thin line separation.....	168
Figure 10-32: Example of non-acceptable bulging.....	168
Figure 10-33: Example of dimple on blind via	169
Figure 10-34: Example of bump on blind via.....	169
Figure 10-35: Example of plating nodule	170
Figure 10-36: Example of burrs reducing hole diameter	170
Figure 10-37: Example of voids – top image shows etch-out and bottom image shows an encapsulated void or inclusion.....	172
Figure 10-38: Skip plating on flex laminate as-polished (top) and after micro-etch (bottom).....	172
Figure 10-39: Skip plating on glass fibres	172
Figure 10-40: Open wedge void (top), enclosed wedge void (middle), copper filled wedge (bottom)	174
Figure 10-41: Schematic of wedge void dimensions.....	174
Figure 10-42: Example of wedge voids.....	174
Figure 10-43: Example of resin void	175
Figure 10-44: Example of delamination	176
Figure 10-45: Pad lift schematic	177
Figure 10-46: Examples of pad lift cracks. The right image is unacceptable because cracks continue until the hole wall	178
Figure 10-47: Acceptable (green) and non-acceptable (red) dielectric cracks.....	180
Figure 10-48: Examples of laminate cracks	180
Figure 10-49: Example of C foil separation as-polished and after micro-etch	182
Figure 10-50: Example of interface line between plated copper layers on a non-etched microsection	182
Figure 10-51: Interconnect after stress, target condition, after microetch (top) and as- polished (bottom)	183
Figure 10-52: Examples of ICD	183
Figure 10-53: Example of smear	184
Figure 10-54: Example of hole wall pull away - showing separation of copper in a straight line (left) or slightly bulging outward (right).....	185
Figure 10-55: Example of resin recession - showing concave retraction of resin	185
Figure 10-56: Target condition.....	186
Figure 10-57: Acceptable nail heading	186

Figure 10-58: Unacceptable nail heading, exceeding 50 % of innerlayer copper thickness	186
Figure 10-59: Examples of CIC connection, target condition (left), nailheading (middle), separation to CIC (right)	187
Figure 10-60: Examples of swirl (1 st and 2 nd image) and demarcation line (3rd). In the 2 nd picture the difference between no-flow prepreg (top) and laminate (bottom) is noticeable	189
Figure 10-61: Example of dotted interface line observed in dark field out of focus (right), which is not visible in focus (middle) and in bright field (left)	189
Figure 10-62: Example of metallic contamination in laminate	190
Figure 10-63: Acceptable adhesion between coverlay and prepreg	191
Figure 10-64: Delamination between coverlay and prepreg	191
Figure 10-65: Example of voids in acrylic adhesive in rigid-to-flex interface	192
Figure 10-66: Example of adhesive filet recession into rigid section as observed in microsection	193
Figure 10-67: Conductor width	195
Figure 10-68: Conductor spacing	196
Figure 10-69: Example of lifted land	197
Figure 10-70: Example of visible copper on top surface (left) and on side of track (right) ...	197
Figure 10-71: Example of measling	198
Figure 10-72: Examples of crazing	198
Figure 10-73: Examples of contamination and inhomogeneity	199
Figure 10-74: Example of scratches on conductors and dielectric	200
Figure 10-75: Haloing at edge	202
Figure 10-76: Haloing from non-plated hole to footprint for stiffener	202
Figure 10-77: Granular aspect	203
Figure 10-78: Dewetting	203
Figure 10-79: Example of unclear marking	204
Figure 10-80: Example of resin squeeze out	205
Figure 10-81: Example of adhesive filet recession into rigid section as observed in visual inspection	205
Figure 10-82: Examples of fibre protrusion	206
Figure 10-83: Example of acceptable incidental haloing ≤ 1 mm into rigid section	207
Figure 10-84: Example of an acceptable superficial scratch	209
Figure 10-85: Examples of non-acceptable cut and blister, evident by a sharp indentation	209
Figure 10-86: Examples of burrs on edge of flex	209
Figure 10-87: Misregistration of top and bottom coverlay	212
Figure 10-88: Misregistration of hole in coverlay to the conductor	212
Figure 10-89: Examples of white spot configurations and black spot contamination	214

Figure 10-90: Examples of fibre contamination.....	214
Figure 10-91: Examples of SnPb infiltration on sculptured pad (left) and on tracks (right)	215
Figure 10-92: Bare copper on fingers	216
Figure 10-93: Misregistration of pads	217
Figure 10-94: Hole misregistration causing reduced annular ring	218
Figure 10-95: Schematic of conductor width and spacing and local defects	220
Figure 10-96: Examples of nick near pad, nick on conductor, overetching reducing thickness of conductor, nick on finger, pinhole and local reduced track width (left to right).....	220
Figure 10-97: Examples of insufficient spacing between conductors, copper residue between pads, copper residue to edge of flex, bump on conductor (left to right).....	220
Figure 10-98: Adhesive in plated holes.....	221
Figure 10-99: Example of adhesive in plated holes	221
Figure 10-100: SnPb coverage on pads	222
Figure 10-101: Pad diameter reduction due to local coverage by coverlay or resin squeeze out	222
Figure 10-102: Copper wrinkle	223
Figure 10-103: Tear in hole and edge of coverlay.....	224
Figure 10-104: Burrs on holes	224
Figure 10-105: Nick on edge of coverlay	224
Figure 10-106: Coverlay scratch – Non acceptable	225
Figure 10-107: Acceptable aspect of finger after bending.....	226
Figure 10-108: Unacceptable aspect of finger after bending.....	226
Figure 10-109: Cross-section of hole: Copper conductor shown.....	228
Figure 10-110: Calculation of remaining insulation distance	233
 Figure H-1 : Typical phenomena in cross-section of PTH. Not all phenomena are specified in ECSS-Q-ST-70-60 in the same way.	261

Tables

Table 6-1: Example of lead time in weeks (wk) for various phases of PCB procurement, manufacture, test and inspection.....	43
Table 7-1: List of coupons with pattern ID, description and references to definition requirements	63
Table 7-2: Test matrix for qualification and procurement	66
Table 8-1: Sampling plan for outgoing visual inspection on PCB	75
Table 8-2: Overview of coupons	76
Table 9-1: Nonconformance criteria for solderability of PTH.....	109

Table 9-2: CAF pattern dimensions – via-to-via straight	136
Table 9-3: CAF pattern dimensions – via-to-via staggered	136
Table 9-4: CAF pattern dimensions – via-to-plane	136
Table 10-1: Annular ring internal	145
Table 10-2: Annular ring external	146
Table 10-3: Copper foil thickness	147
Table 10-4: Copper plating thickness	148
Table 10-5: Etchback and glass fibre protrusion	150
Table 10-6: Wicking	151
Table 10-7: Wrap copper	152
Table 10-8: Dielectric thickness – standard technology	153
Table 10-9: Dielectric thickness – microvia layers	154
Table 10-10: Dimension and aspect of microvias	155
Table 10-11: Microvia plating voids	156
Table 10-12: Tin-lead thickness and composition	157
Table 10-13: Dimensional requirements for electrolytic and chemical Ni, Pd, Au	159
Table 10-14: Undercut and spurious copper	160
Table 10-15: Overhang	162
Table 10-16: Rigid-flex interface -dimensional verification	163
Table 10-17: Blind, buried and plugged via filling	166
Table 10-18: Cap lift on blind via and plugged via	168
Table 10-19: Blind and plugged via planarity	169
Table 10-20: Burrs and nodules	170
Table 10-21: Voids and inclusions in copper plating	171
Table 10-22: Wedge voids	173
Table 10-23: Resin void	175
Table 10-24: Delamination, blistering, crazing, measling	176
Table 10-25: Pad Lift	177
Table 10-26: Dielectric cracks	179
Table 10-27: Cracks and separation in copper	181
Table 10-28: Interconnect defect, ICD	183
Table 10-29: Smear	184
Table 10-30: Hole wall pull away and resin recession	185
Table 10-31: Nail heading	186
Table 10-32: Cu-Invar-Cu	187
Table 10-33: Inhomogeneity in dielectric	188
Table 10-34: Contamination or foreign inclusion	190

Table 10-35: Rigid-flex interface - delamination between coverlay and prepreg	191
Table 10-36: Rigid-flex interface - adhesive voids in coverlay and bond-ply	192
Table 10-37: Rigid-flex interface - misalignment of prepreg	193
Table 10-38: Conductor width.....	195
Table 10-39: Conductor spacing.....	196
Table 10-40: Surface metallization	197
Table 10-41: Measling, crazing, blistering, delamination.....	198
Table 10-42: Contamination, inhomogeneity	199
Table 10-43: Scratches	200
Table 10-44: Weave exposure.....	201
Table 10-45: Haloing at PCB edge and non-plated holes	202
Table 10-46: Tin-lead surface quality.....	203
Table 10-47: Marking, identification	204
Table 10-48: Rigid-flex interface - misalignment of prepreg	205
Table 10-49: Rigid-flex interface - fibre protrusion	206
Table 10-50: Rigid-flex interface - haloing	207
Table 10-51: Rigid-flex - aspect of flex laminate and coverlay	208
Table 10-52: Sculptured flex - misregistration of holes	212
Table 10-53: Sculptured flex - aspect of coverlay	213
Table 10-54: Sculptured flex - SnPb infiltration.....	215
Table 10-55: Sculptured flex - bare copper on fingers and pads.....	216
Table 10-56: Sculptured flex – misregistration between pads	217
Table 10-57: Sculptured flex – annular ring	218
Table 10-58: Sculptured flex - copper conductor width and spacing	219
Table 10-59: Adhesive in plated holes.....	221
Table 10-60: Sculptured flex – aspect of pads on solder side	222
Table 10-61: Sculptured flex - copper wrinkle.....	223
Table 10-62: Sculptured flex – aspect of mechanical holes and edge of coverlay	224
Table 10-63: Sculptured flex – scratch on coverlay	225
Table 10-64: Sculptured flex - aspect of finger after bending	226
Table 10-65: Sculptured flex - marking adhesion strength	227
Table 10-66: Sculptured flex - microsection.....	228

European Foreword

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This document (EN 16602-70-60:2019) originates from ECSS-Q-ST-70-60C Corrigendum 1.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by January 2020, and conflicting national standards shall be withdrawn at the latest by January 2020.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN shall not be held responsible for identifying any or all such patent rights.

This document will supersede EN 16602-70-10:2015 and EN 16602-70-11:2015.

This document is the result of the merge and update of both superseded standards, including the implementation of Change Requests.

This document has been developed to cover specifically space systems and will therefore have precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

This document has been prepared under a standardization request given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

According to the CEN-CENELEC Internal Regulations, the national standards organizations of the following countries are bound to implement this European Standard: Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, Former Yugoslav Republic of Macedonia, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey and the United Kingdom.

Introduction

PCBs are used for the mounting of electronic components to produce PCB assemblies that perform electrical functions. The PCBs are subjected to thermo-mechanical stress during assembly such as soldering of components, rework and repair under normal terrestrial conditions. In addition, the assembled PCBs are exposed to the launch and space environment. The reliability of the circuit depends on the robustness of the manufacturing processes, for which this standard specifies requirements. PCB technology needs detailed inspections to verify its reliability, which is specified for the qualification and procurement phases of the PCB technology.

1

Scope

This standard specifies the requirements for the PCB manufacturer, the procurement authority and the qualification authority for qualification and procurement of PCB technology.

ECSS-Q-ST-70-60 is applicable for all types of PCBs, including sequential, rigid and flexible PCBs, sculptured flex, HDI and RF PCBs.

This standard can be made applicable for other products combining mechanical and electrical functionality using additive or reductive manufacturing processes, as used in PCB manufacturing. Examples of such products are slip-rings, bus bars and flexible flat cables.

This standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revision of any of these publications do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the more recent editions of the normative documents indicated below. For undated references, the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system — Glossary of terms
EN 16602-10-09	ECSS-Q-ST-10-09	Space product assurance — Nonconformance control system
EN 16602-20	ECSS-Q-ST-20	Space product assurance — Quality assurance
EN 16602-70	ECSS-Q-ST-70	Space product assurance — Material, mechanical parts and processes
EN 16602-70-02	ECSS-Q-ST-70-02	Space product assurance — Thermal vacuum outgassing test for the screening of space materials
EN 16602-70-08	ECSS-Q-ST-70-08	Space product assurance — Manual soldering of high-reliability electrical connections
EN 16602-70-12	ECSS-Q-ST-70-12	Space product assurance — Design rules for printed circuit boards
EN 16602-70-21	ECSS-Q-ST-70-21	Space product assurance — Flammability testing for the screening of space materials
EN 16602-70-22	ECSS-Q-ST-70-22	Space product assurance — Control of limited shelf-life materials
EN 16602-70-29	ECSS-Q-ST-70-29	Space product assurance — Determination of offgassing products from materials and assembled articles to be used in a manned space vehicle crew compartment
EN 16602-70-38	ECSS-Q-ST-70-38	Space product assurance — High reliability soldering for surface mount and mixed technology printed circuit boards
	EN 9100:2016	Quality management systems – Requirements for aviation, space and defense organisations

EN reference	Reference in text	Title
	IEC 60326-2-am 1 (1992-06)	Printed boards. Part 2: Test methods
	IEC 60194 (1999-04)	Printed board design, manufacture and assembly — Terms and definitions
	IPC-A-600J (2016)	Acceptability of Printed Boards
	IPC-T-50M (2015)	Terms and definitions for interconnecting and packaging electronic circuits
	IPC-TM-650	Test methods manual
	IPC-1710A (2004)	OEM Standard for Printed Board Manufacturers' Qualification Profile
	IPC-4101E (2017)	Specification for base materials for rigid and multilayer printed boards
	IPC-4103A-WAM1 (2014)	Specification for Base Materials for High Speed/ High Frequency Applications
	IPC-4203A (2013)	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
	IPC-4204A-WAM1 (2014)	Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry
	IPC-6012D (2015)	Qualification and performance specification for rigid printed boards
	IPC-6012DS (2015)	Space and military avionics applications addendum to IPC-6012D
	IPC-6013D (2017)	Qualification and Performance Specification for Flexible Printed Boards
	IPC-6018C (2016)	Qualification and Performance Specification for High Frequency (Microwave) Printed Boards
	IPC-6018CS (2016)	Space and Military Avionics Applications Addendum to IPC-6018C
	ISO 9001:2015	Quality management systems - Requirements
	ISO-14644-1 (2015)	Cleanrooms and associated controlled environments - Part 1: Classification of air cleanliness by particle concentration

Terms, definitions and abbreviated terms

3.1 Terms from other standards

- a. For the purpose of this Standard, the terms and definitions from ECSS-S-ST-00-01 apply, and in particular the following terms:

1. customer
2. supplier

NOTE See clause 4.2 for a description of roles of customer and supplier.

- b. For the purpose of this Standard, the terms and definitions from ECSS-Q-ST-70-12 apply, and in particular the following terms:

1. annular ring
2. area array device (AAD)
3. aspect ratio
4. basic copper
5. blind via
6. bond-ply
7. build-up
8. buried via
9. conductor
10. FR4
11. hole wall pull away
12. heat sink
13. high density interconnect (HDI)
14. interlayer
15. intralayer
16. laminate
17. microvia
18. no-flow prepreg
19. non-functional pad

- 20. non-pated hole
- 21. normal pitch
- 22. panel
- 23. plated through-hole (PTH)
- 24. prepreg
- 25. printed circuit board (PCB)
- 26. resin starvation
- 27. serialization
- 28. spacing
- 29. stack
- 30. track
- 31. via
- 32. X,Y direction
- 33. Z direction

3.2 Terms specific to the present standard

3.2.1 automated optical inspection (AOI)

inspection method using an automated equipment to verify the pattern on an etched layer

3.2.2 back-drilled via

type of via with part of its metallisation removed on one side by depth controlled mechanical drilling with a larger diameter drill

3.2.3 batch

group of PCBs and coupons that are covered by the same CoC and the same traveller

NOTE 1 A batch is processed approximately at the same time. See 6.8a.

NOTE 2 The terms “lot” and “work order” are synonymous.

3.2.4 blind-via-in-pad

type of via directly underneath a SMT pad

3.2.5 blister

delamination in the form of a localized swelling and separation between any of the layers of a laminated base material, or between base material and conductive foil or protective coating

[IPC-T-50M]

3.2.6 cap lift

separation between resin in blind via and copper cap plating on surface

NOTE Cap lift can be shown as bulging and as thin line separation, as shown in Table 10-18.

3.2.7 contamination

<CONTEXT: Qualification and procurement of PCBs>

foreign material embedded in dielectric material

NOTE 1 Synonyms are: FOD, inclusion (see definition 3.2.20), foreign material, debris, pollution.

NOTE 2 Contamination can be organic, metallic, particulate or fibres.

3.2.8 coupon

small piece of test circuitry that is used for quality conformance evaluation by specific tests and inspection

NOTE 1 The coupon is manufactured as part of a panel and at the final manufacturing stage it is separated from it. The coupon is thus associated with the PCBs within the panel, with which it was simultaneously manufactured.

NOTE 2 The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

[adapted from IPC-T-50M]

3.2.9 coverlay

thin dielectric material used to encapsulate circuitry, most commonly for flexible circuit applications

NOTE The terms 'cover layer' and 'cover material' are synonymous.

3.2.10 crazing

condition that occurs in reinforced laminate base material whereby glass fibre bundles are separated from the resin not limited to the weave intersections

NOTE 1 This condition manifests itself in the form of connected white spots or crosses that are below the surface of the base material. It is usually related to thermally or mechanically induced stress. Crazing is a more severe defect than measling. Delamination is a further worsening of crazing.

NOTE 2 See also "measling".

3.2.11 delamination

separation between plies within a base material, between base material and a conductive foil, or any other planar separation with a PCB

NOTE See also 'blister', which is a local delamination.

[IPC-T-50M]

3.2.12 destructive physical analysis (DPA)

analysis method using sampling, potting, grinding, polishing and inspection which, thus, destroys the test vehicle

NOTE The term 'microsectioning' is approximately synonymous.

3.2.13 dewetting

condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the base metal not exposed

[IPC-T-50M]

3.2.14 dross

oxide and other contaminants that form on the surface of molten solder

[IPC-T-50M]

3.2.15 etchback

distance from resin of hole wall to innerlayer foil

3.2.16 fine pitch

spacing of tracks or pads that is more dense than for normal pitch

NOTE Pitch is specified in clause 7.4 of ECSS-Q-ST-70-12.

3.2.17 flexible

PCB technology that uses only flexible layers in its build up

NOTE The term 'flex' is synonymous.

3.2.18 glass compression

deformed glass fibre bundles of prepreg causing absence of resin between glass and copper due to profiled copper pattern

NOTE See also 'resin starvation'.

3.2.19 haloing

mechanically-induced fracturing or delamination, on or below the surface of a base material, that is usually exhibited by a light area around holes or other machined features

[IPC-T-50M]

3.2.20 inclusion

foreign particle, metallic or non-metallic, that can be entrapped in an insulating material, conductive layer, plating, base material or solder connection
[IPC-T-50M]

3.2.21 interconnect defect (ICD)

separation at the interface between internal layer and through-hole plating

NOTE 1 The term 'innerlayer separation' is synonymous.

NOTE 2 See 'smear' for additional explanation.

[IPC-6012D]

3.2.22 interconnect stress test (IST)

test method using a specific IST coupon and a specific IST equipment

3.2.23 IST coupon

specific coupon for IST

NOTE The term 'coupon' refers to a generic pattern, whereas the term 'IST coupon' refers to the specific IST pattern.

3.2.24 key personnel

personnel with specialist knowledge responsible for defined production or product assurance areas

3.2.25 lay-out

design of the conductive pattern on a layer

3.2.26 measling

condition that occurs in laminated base material whereby glass fibre bundles are separated from the resin limited to the weave intersection

NOTE 1 This condition manifests itself in the form of discrete white spots or "crosses" that are below the surface of the base material. It is usually related to thermally-induced stress or humidity.

NOTE 2 See also "crazing", which is a further worsening of measling.

[IPC-T-50M]

3.2.27 metal core

layer or local insert of thick metal embedded inside the PCB usually used as a heat sink, grounding layer or restriction of thermal expansion

3.2.28 milling

mechanical method that removes a portion of the material outlining a PCB using a cutting bit

NOTE See also 'routing'.

3.2.29 multilayer

PCB technology that uses lamination of several copper layers and plated holes for interconnection

NOTE PCBs that are not multilayer, are double-sided or single-sided PCBs. See also "sequential".

3.2.30 plated hole

hole that is used as an interlayer connection

NOTE Types of plated holes are PTH and vias.

3.2.31 PCB manufacturer

entity that manufactures the PCB

NOTE The PCB manufacturer is supplier to the procurement authority.

3.2.32 PCB technology

category of manufacturing processes, materials and design for PCBs

NOTE Examples of PCB technology are:

- Polyimide sequential rigid
- Polyimide sequential rigid/flex
- Epoxy sequential rigid
- Epoxy non-sequential rigid/flex
- HDI with microvias
- RF
- Flexible and sculptured flex

3.2.33 plugged via

via type that is cap plated and filled with resin in a specific via filling process

NOTE Blind vias can be resin-filled using resin from the prepreg during sequential lamination. Plugged vias use a resin that does not originate from the prepreg and the filling process does not occur during lamination.

3.2.34 procurement authority

entity that procures the PCB

NOTE 1 The procurement authority is customer of the PCB manufacturer.

NOTE 2 The procurement authority can be supplier to the prime contractor.

3.2.35 qualification authority

entity that qualifies the PCB technology and PCB manufacturer

3.2.36 radio frequency (RF)

electronic functionality that requires specific design precautions on dielectric materials and copper pattern to maintain time dependant signal integrity

NOTE 1 The term 'high speed' is synonymous.

NOTE 2 The term 'RF PCB' identifies the PCB technology.

3.2.37 rigid

PCB technology that uses only rigid layers in its build-up

3.2.38 rigid/flex

PCB technology that uses a combination of rigid and flexible layers in its build-up

3.2.39 routing

the lay-out and connection of conductors between plated-holes and pads

NOTE The term 'routing' is also used for 'milling'. This second meaning is not used in ECSS-Q-ST-70-60 to avoid confusion.

3.2.40 scratch

narrow furrow or groove in a surface

NOTE It is usually shallow and caused by the marking or rasping of the surface with a pointed or sharp object.

[IEC 60194 (1999-04)]

3.2.41 sculptured flex

flexible PCB technology that uses profiled copper tracks

NOTE Aviflex is a commercial identification of sculptured flex.

3.2.42 sequential

PCB technology that uses more than one lamination or drilling step

NOTE The term 'sequential' also implies that the PCB is of type 'multilayer'. The opposite is 'non-sequential'.

3.2.43 sequential via

via type that interconnects layers within the same plating sequence

NOTE Examples of sequential vias are blind vias and buried vias.

3.2.44 skip plating

local missing deposition of plating

NOTE Skip plating can occur on electroless copper plating on glass in the hole wall. Skip plating can also occur on surface finish.

3.2.45 smear

base material resin that covers the interface between the exposed edge of an innerlayer pad and through-hole plating

NOTE 1 The resin transfer is usually caused by the drilling operation and removed during the desmear process. The term 'resin smear' or 'smearing' are synonymous.

NOTE 2 The aspect of smear can be mistaken for interconnect defect, or vice versa. Smear is the presence of resin, whereas interconnect defect is an adhesive separation of copper plating.

[adapted from IPC-T-50M]

3.2.46 test pattern

part of the PCB or coupon that refers to the copper pattern for a specific test

[adapted from IPC-T-50M]

3.2.47 through-going via

type of via that is drilled through the entire thickness of the PCB

3.2.48 traveller

documentation kept with the batch during the manufacturing processes in which the order of specific processes are recorded

3.2.49 treatment side of foil

the side of copper foil that is submitted to a surface treatment process by the materials supplier or by the PCB manufacturer

NOTE The material supplier treatment side of copper foil on laminate is typically rougher. See Figure 3-1.

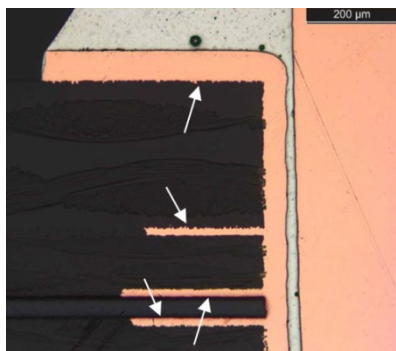


Figure 3-1: Example of material supplier treatment side of foil (white arrows) and PCB manufacturer treatment side of foil (opposite side)

3.2.50 waiver request

written agreement between PCB manufacturer and procurement authority to deliver PCBs with a nonconformance to a requirement from a specification

NOTE 1 The following terms are synonymous: “request for concession”, “demande de derogation”, “request for waiver”, “request for deviation”.

NOTE 2 In space projects the terms RFW and RFD have specific meaning as specified in ECSS-Q-ST-70. This specific meaning does not strictly apply in the context of PCB procurement.

3.2.51 weave exposure

a base material surface condition in which unbroken fibres of woven glass are not completely covered by resin

NOTE See also ‘weave texture’.

[IPC-T-50M]

3.2.52 weave texture

a surface condition of base material in which a weave pattern of cloth is apparent although the unbroken fibres of woven cloth are completely covered by resin.

NOTE See also ‘weave exposure’.

[IPC-T-50M]

3.2.53 wicking

infiltration of copper plating into the dielectric of the hole wall

NOTE The terms “copper infiltration” and “copper ingress” are synonymous.

3.2.54 work instruction

quality document that describes the technical details about processes, material usage, inspection and acceptance criteria

NOTE 1 The terms ‘manufacturing procedure’ or ‘control procedure’ or ‘process instruction’ are synonymous.

NOTE 2 Work instructions can include process flow charts, production documents (e.g. manufacturing plans, travelers, routers, work orders, process cards) and inspection documents.

3.3 Abbreviated terms

For the purpose of this Standard, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
AAD	area array device
AC	alternating current
AOI	automated optical inspection
AR	as received
CDR	critical design review
CIC	copper-invar-copper
CoC	certificate of conformance
CTE	coefficient of thermal expansion
Cu	copper (element)
CVCM	collected volatile condensable material
DC	direct current
DML	declared materials list
DPA	destructive physical analysis
DR	design review
DRB	delivery review board
DRD	document requirements definition
DSC	differential scanning calorimetry
DWV	dielectric withstanding voltage
EBB	elegant breadboard
ECM	electrochemical migration
EM	engineering model
EOL	end of life
EQM	engineering qualification model
FAI	first article inspection
FCSI	final customer source inspection
FM	flight model
FOD	foreign object debris
FR4	type of epoxy resin for PCBs
FS	flight spare
HDI	high density interconnect
ICD	interconnect defect
IMC	intermetallic compound
IPA	isopropanol
IPC	association connecting electronic industries
IST	interconnect stress test

Abbreviation	Meaning
KPI	key performance indicator
max	maximum
min	minimum
MIP	mandatory inspection point
MPCB	material and processes control board
MRR	manufacturing readiness review
MTO	metal turnover
n. a.	not applicable
NCR	nonconformance report
NRB	nonconformance review board
OTD	on time delivery
PCB	printed circuit board
PCN	process change notice
PDR	preliminary design review
PFM	proto flight model
PID	process identification document
PTH	plated-through hole
PTFE	polytetrafluoroethylene
QA	quality assurance
QM	qualification model
QML	qualified manufacturers list
QPL	qualified product list
r.m.s.	root-mean-square
R&D	research and development
Ref	reference (for tables in clause 10)
RF	radio frequency
RFA	request for approval
RML	residual mass loss
RW	rework simulation
SB	solder bath float
SMT	surface mount technology
SPC	statistical process control
sq	square (in unit Ω/sq)
TBD	to be defined
TDR	time domain reflectometry
T288	time to delamination at 288°C
Td	temperature of decomposition
Tg	temperature of glass transition

Abbreviation	Meaning
TGA	thermogravimetric analysis
TMA	thermomechanical analysis
wk	week

3.4 Nomenclature

The following nomenclature applies throughout this document:

- a. The word “shall” is used in this Standard to express requirements. All the requirements are expressed with the word “shall”.
- b. The word “should” is used in this Standard to express recommendations. All the recommendations are expressed with the word “should”.

NOTE It is expected that, during tailoring, recommendations in this document are either converted into requirements or tailored out.

- c. The words “may” and “need not” are used in this Standard to express positive and negative permissions, respectively. All the positive permissions are expressed with the word “may”. All the negative permissions are expressed with the words “need not”.
- d. The word “can” is used in this Standard to express capabilities or possibilities, and therefore, if not accompanied by one of the previous words, it implies descriptive text.

NOTE In ECSS “may” and “can” have completely different meanings: “may” is normative (permission), and “can” is descriptive.

- e. The present and past tenses are used in this Standard to express statements of fact, and therefore they imply descriptive text.

4 Principles

4.1 General

This standard specifies requirements for the manufacture, qualification, procurement, test and inspection of PCBs.

4.2 Roles

In the context of ECSS-Q-ST-70-60 the roles “PCB manufacturer”, “procurement authority” and “qualification authority” were explicitly introduced and defined in clause 3.2 to allow proper allocation of requirements.

4.3 References to acceptance criteria

Clause 10 includes tables to specify acceptance criteria for certain technological features. The technological features can be further subdivided in each table. This is indicated with a reference letter in the first column and abbreviated as “Ref x”. This allows cross-referencing to specific line items in the table, rather than to an entire table. An example of this is “internal annular ring on an inner layer at the end of a blind via” which is cross-referenced as Ref. b in Table 10-1.

QA for qualification

5.1 Qualified PCBs

- a. Qualified PCBs for space applications shall meet all the following conditions:
1. the PCB is procured in conformance with clauses 6 and 8,
 2. the PCB is procured from a PCB manufacturer that is qualified in conformance with clauses 5 and 7 and as specified in the PID,
 3. the PCB design is in conformance with the requirements of ECSS-Q-ST-70-12.

NOTE Some specific PCB technologies can be used that are not covered by a valid PID or by a company qualification. Procurement can be done under RFA, including tests for (delta) qualification and tests for procurement but it can exclude the qualification of the company. Examples of specific PCB technology are complex HDI, complex RF and flex technology that are under development. This is described in clauses 5.2 and 7.7.

- b. The qualification of PCBs in conformance with this standard shall cover for a maximum operational temperature of 85 °C.

NOTE 1 This is also described in clause 1 "Scope" of ECSS-Q-ST-70-08 and clause 1 "Scope" of ECSS-Q-ST-70-38.

NOTE 2 This is in conformance with current rating requirements from clause 13.6.2 of ECSS-Q-ST-70-12.

NOTE 3 PCBs are not qualified for a specific voltage as this is depending on PCB design in conformance with ECSS-Q-ST-70-12.

5.2 Ceramic PCB technology

- a. PCBs manufactured using ceramic filled laminate shall be in conformance with ECSS-Q-ST-70-60.

NOTE This is opposed to ceramic substrates using thick film or thin film processes that are in conformance with ESCC-2566000.

5.3 Flexible PCB

5.3.1 General

Flexible PCBs can be used as harness or cable for interconnection of PCB assemblies, components or detectors, in which case they are short, typically less than 0,5 m. Flexible PCBs can also be used to interconnect larger elements such as equipment, solar cells or solar panels. And they can be used as radiating RF element for antennae. In such applications the flexible PCBs can be long, typically more than 1 m. Moreover, they can be used in dynamic applications such as solar array drive mechanisms, thruster orientation mechanisms or antenna pointing mechanisms.

Products can include various terminology, such as “flat cable”, “flexprint”, “ribbon flex” and similar. These products are referred to in this standard as “flexible PCB”. A specific type of flexible PCB also referred to in this standard is the “sculptured flex PCB”, which is typically used for interconnection of components to PCBs or in between PCBs.

Encapsulation of separate copper strings or wires to form a flexible cable is not a conventional PCB manufacturing process, and can therefore be considered a cable. Etching of copper clad flexible laminate and lamination of coverlay, among others, are conventional PCB manufacturing processes and are covered by ECSS-Q-ST-70-60.

Heaters are in conformance with ESCC-4009. Cables are in conformance with ESCC-3901.

5.3.2 Qualification of flexible PCB

- a. For flexible PCBs, a company specific qualification with auditing and review of QA should be performed.

NOTE This is good practice to verify batch-to-batch reproducibility.

- b. In case the flexible PCB is not qualified in conformance with ECSS-Q-ST-70-60, the project qualification of flexible PCB shall be reviewed under RFA in conformance with clause 7.7.2.
- c. Flexible PCB for harness shall be qualified and procured as per ECSS-Q-ST-70-60 and designed as per ECSS-Q-ST-70-12, except for the cases from requirements 5.3.2d and 5.3.2e.

- d. In case the self-heating of maximum 10 °C in conformance with requirement 13.6.2a from ECSS-Q-ST-70-12 or in case the operational temperature of maximum 95 °C in conformance with requirement 13.6.2c from ECSS-Q-ST-70-12 is exceeded, it shall be specifically covered by the project qualification of flexible PCB for harness.

NOTE Current rating of ECSS-Q-ST-70-12 can be too conservative for harness applications for power lines.

- e. In case double insulation in Z-direction is not in conformance with Table 13-6 from ECSS-Q-ST-70-12, it shall be specifically covered by the project qualification of flexible PCB for harness.

NOTE The test plan can be based on the test selection for a change in dielectric material from clause 7.2d.

- f. Electrical testing of the integrated subsystem of connector and flexible PCB shall be specifically covered by the project qualification of flexible PCB for harness.

NOTE An example of a relevant electrical test is DWV in conformance with clause 9.6.4, using 1000 VDC for 30 s. Another example of a relevant electrical test is the whole length voltage test and whole length insulation resistance test in conformance with clauses 9.7b and 9.8b from ESCC-3901. Tests for qualification and for procurement in conformance with ECSS-Q-ST-70-60 includes high resistance electrical test with a 1 GΩ insulation resistance threshold in conformance with clause 9.3.7.2 and continuity test in conformance with 9.3.8.

- g. Dynamic application shall be specifically covered by the project qualification of flexible PCB for harness, including at least the following:

1. evaluation of the mechanical integrity of the insulation due to routing limitations, and
2. mechanical testing from ESCC-3901 tailored to meet the application, and
3. electrical evaluation before and after mechanical test and qualitative evaluation by microsectioning after mechanical test.

NOTE 1 Mechanical integrity of the insulation can be impacted by abrasion, point loads and the dynamic movement.

NOTE 2 In addition, dynamic application can be covered at unit level as specified in clause 4.8.3 of ECSS-E-ST-33-01. Unit level qualification testing is performed at a later stage in the project than qualification of subassemblies including the flexible PCB.

- h. RF application shall be specifically covered by the project qualification of flexible PCB.

- i. Assembly to flexible PCB using PTH or SMT shall be verified in conformance with ECSS-Q-ST-70-08 and ECSS-Q-ST-70-38.

5.4 Qualification process

- a. The process for PCB qualification shall contain the following stages:
 - 1. request for qualification and associated documentation in conformance with clause 5.5,
 - 2. evaluation of a technology sample in conformance with clause 5.8,
 - 3. audit of the manufacturing facility in conformance with clause 5.9,
 - 4. qualification programme in conformance with clause 5.10.
- b. The approval from the qualification authority of the completed qualification shall be in conformance with clause 5.12.

5.5 Request for qualification

- a. The PCB manufacturer shall send a formal request for qualification to the qualification authority.
- b. The PCB manufacturer shall provide the company profile including the following information:
 - 1. description of the manufacturer capabilities,
 - 2. business plan with basic financial figures for sales and R&D.

NOTE The business plan demonstrates a healthy economical business and a strong commitment to quality assurance for space products.
- c. The PCB manufacturer shall demonstrate the heritage on the PCB technologies for which qualification is requested, by providing the types of technology and quantity of PCBs produced for non-space customers, industrial space customers and space agencies.

NOTE This is in particular important for the approved surface finishes, such as hot oil reflowed tin-lead.
- d. The PCB manufacturer shall provide a letter of support from the main industrial space customers.
- e. The PCB manufacturer shall provide a preliminary strategic planning, indicating the following:
 - 1. the space projects for which qualified PCBs are foreseen to be provided,
 - 2. identification of the current customers that can benefit from possible qualification,
 - 3. identification of new customers or orders that can be gained in case qualification is achieved,
 - 4. identification of technologies that are foreseen to be qualified initially and in the medium and longer term,

- 5. the internal resource estimate for achieving qualification,
- 6. a target schedule for all activities related to achieving qualification.
- f. The PCB manufacturer shall provide the completed survey for assessment of the PCB manufacturer's capabilities in conformance with IPC-1710.
- g. The PCB manufacturer shall demonstrate that it meets the requirements for quality assurance in conformance with clause 5.6.

5.6 Quality standards

- a. The quality assurance requirements specified in ECSS-Q-ST-20 shall apply.
- b. The PCB manufacturer shall manage nonconformances in accordance with ECSS-Q-ST-10-09.
- c. The PCB manufacturer shall hold certification for its quality management system in conformance with ISO 9001:2015 and EN 9100:2016 or demonstrate that he has a quality management system in line with the above standards.

5.7 Description of qualification vehicle

- a. The PCB manufacturer shall provide the PCB definition dossier, in conformance with the DRD in Annex A of ECSS-Q-ST-70-12, to the qualification authority for approval of the qualification vehicle.
- b. The qualification vehicle shall be representative of the highest technological complexity for which qualification is requested.
- c. The design of the qualification test vehicle shall accommodate the tests specified in clause 7.

NOTE Examples of test patterns are shown in IPC-2221B.

- d. The design of the qualification vehicle shall be in conformance with requirements from ECSS-Q-ST-70-12.
- e. The coupons that are included in the qualification vehicle shall be in conformance with the clauses 8.2.2 and 8.2.3.
- f. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2b shall be performed on at least 3 PCBs and the coupons in conformance with Figure 7-1.
- g. Initial qualification of a PCB manufacturer or PCB technology in conformance with requirement 7.2b should include a spare PCBs and spare coupons in conformance with Figure 7-1.
- h. Delta qualification and qualification renewal in conformance with requirement 7.2 shall be performed on at least 1 PCB and associated coupons.

5.8 Evaluation

- a. The requirements of clause 5.7 shall apply to the evaluation samples.
- b. The submission of evaluation samples shall include PCB, coupons, microsections and documentation in conformance with requirement 5.15a.
- c. A first set of evaluation samples should be evaluated by a third-party.
- d. The test flow for evaluation shall be in conformance with requirements from clause 7.5.

NOTE It is beneficial to request a third-party evaluation by a company with knowledge on evaluation in conformance with ECSS-Q-ST-70-60.

NOTE 1 This test flow includes DPA of PCB and coupons and IST.

NOTE 2 Any duplication of IST tests on panels for evaluation, qualification and procurement allows assessment of batch-to-batch reproducibility.

NOTE 3 The evaluation phase is only performed in case of qualification of new PCB manufacturers. It is intended as a relatively fast assessment of the quality to gain confidence in the product before initiating the full qualification programme. Therefore the evaluation typically does not include mission representative thermal cycling, which is included in qualification.

- e. The qualification authority shall perform the evaluation and issue the test report.
- f. The qualification authority shall provide to the PCB manufacturer the authorization to proceed with the qualification in case all the following conditions are met:
 - 1. Evaluation is acceptable.
 - 2. Assessment of the request for qualification, in conformance with the clause 5.5, is acceptable.

NOTE It is the intention to perform a PCB evaluation only once. In case the first attempt fails, a second final opportunity for passing the evaluation successfully can be offered. The qualification process can be discontinued in case the evaluation fails or in case the schedule as agreed in the strategic planning is exceeded.

5.9 Audit

- a. The qualification authority shall audit the manufacturing line.
- b. The audit shall occur when PCB production is in progress.

- c. Before the audit, the PCB manufacturer shall make the following documents available to the qualification authority for review and approval:
 - 1. PID in conformance with the DRD in Annex D;
 - 2. Qualification test plan in conformance with clause 7.1 including test description, test vehicle and schedule.
- d. The qualification authority shall submit to the PCB manufacturer an audit checklist that verifies the requirements from ECSS-Q-ST-70-60 and its normative references one month prior to the date of the audit.
- e. The PCB manufacturer shall provide the response to the audit checklist to the qualification authority at least one week prior to the date of the audit.
- f. The response from the PCB manufacturer in the audit checklist shall include the following:
 - 1. compliance level as follows:
 - (a) "compliant" or
 - (b) "non-compliant" or
 - (c) "partial compliant" or
 - (d) "not applicable",
 - 2. a comment explaining any non-compliance, partial compliance or non-applicability,
 - 3. references to work instructions that specify the verified requirement.
- g. During the audit, the PCB manufacturer shall make the following documents available to the qualification authority:
 - 1. Documented information in conformance with EN 9100:2016 clause 4.2.2.
 - 2. Business process procedures, in conformance with EN 9100.
 - 3. Work instructions, in conformance with EN 9100.
 - NOTE 1 Quality manual is one possible type of Documented information from 5.9g.1.
 - NOTE 2 See definition of work instructions in clause 3.2.54.
- h. In case of an audit for qualification renewal, the PCB manufacturer shall provide the following:
 - 1. A summary of the QA reports in conformance with clause 5.14.
 - 2. Lists of PCBs per PID supplied in conformance with ECSS-Q-ST-70-60 since the previous audit.
- i. The qualification authority shall issue the audit report and any findings, in conformance with clause 5.9j.
 - NOTE The minutes of meeting can be the audit report.
- j. Findings from the audit shall be categorised by the qualification authority as follows:

1. “Major nonconformance” is a nonconformance against ECSS-Q-ST-70-60 that is evaluated by the qualification authority as mandatory to disposition by a corrective action for successful audit closure.
 2. “Minor nonconformance” is a nonconformance against ECSS-Q-ST-70-60 that is a longer term action for continuous improvement and therefore not preventing successful audit closure according to the qualification authority.
 3. “Observation” is a recommendation or observation that does not prevent successful audit closure and that is not a nonconformance against ECSS-Q-ST-70-60.
- k. The audit report and any findings shall be approved and signed by the PCB manufacturer and qualification authority.
 - l. Corrective actions from findings shall be added to the updated audit report or minutes of meeting of a delta audit.
 - m. The final conclusion of the audit process shall be provided in the final audit report or minutes of meeting.

5.10 Qualification test programme

- a. The requirements of clause 5.7 shall apply to the qualification vehicle.
- b. The PCB manufacturer shall perform the qualification tests as specified in the qualification test plan in conformance with requirement 7.2b and approved by the qualification authority in conformance with requirements 5.9c and 5.9k.

NOTE The PCB manufacturer can use labs from a third-party or from the customer to perform tests.

- c. The PCB manufacturer shall issue the qualification test report in conformance with the DRD in Annex C.
- d. The PCB manufacturer shall provide the qualification test report to the qualification authority for review and approval.
- e. The qualification authority may request to the PCB manufacturer an additional test vehicle or microsections for evaluation.

5.11 PID

- a. The PCB manufacturer shall issue the PID in conformance with the DRD of Annex D.
- b. The specific parts of the PID shall be issued, in conformance with D.2.1.2, for the following PCB technologies in separate documents:
 1. Polyimide rigid
 2. Polyimide rigid/flex
 3. Epoxy rigid
 4. Epoxy rigid/flex

5. HDI
6. RF
7. Flexible
8. Sculptured flex
9. Low thermal expansion materials

5.12 Qualification approval

- a. Upon successful qualification, the qualification authority shall issue a qualification letter in conformance with the DRD in Annex A.
- b. The qualification authority shall publish the qualification status.
- c. The reason for a change or updated qualification status shall be published as a comment to the qualification status.

NOTE The term “qualified” can be used to indicate a valid qualification status. The term “not qualified” can be used to indicate an invalid qualification status, for instance as a result of nonconformances during qualification renewal or as a result of an expired qualification period. The status is not definite and can be updated when new results are available. A comment is included to clarify the reason for the qualification status. A definite disqualification or discontinuation of PCB technology or PCB manufacturer can be indicated by deletion from the published list or by the terms “disqualified” or “discontinued”.

- d. The qualification authority shall grant qualification approval to the PCB manufacturer based on the acceptance of the evaluation in conformance with clause 5.8, the audit in conformance with clause 5.9 and the qualification programme in conformance with clause 5.10.
- e. The qualification approval shall be valid for a period of maximum two years.
- f. In case nonconformances have been encountered, the qualification authority may grant a period of validity for the qualification that is shorter than two years.

NOTE One year is a commonly used qualification period to ensure a more frequent verification of the process control for a critical technology.

5.13 Process change

- a. Process changes shall include process parameters, chemistry, material, equipment, process flow and inspections.

- b. Process changes shall be categorised by the PCB manufacturer as “major” or “minor” in the PCN.
- c. Requests for major process changes shall be submitted to the qualification authority for approval.

NOTE Review of process changes by the qualification authority in a timely manner is important for the continuation of manufacturing.

- d. The implementation of a major change shall be submitted to the qualification authority for approval.
- e. Minor process changes may be implemented by the PCB manufacturer without prior approval of the qualification authority.

NOTE The PCN for a minor change includes the acceptable evaluation of the affected acceptance criteria in conformance with E.2.1b6.

- f. For major and minor process changes, the PCB manufacturer shall issue a process change notice in conformance with the DRD in Annex E to the qualification authority.
- g. All process change notices should be submitted to the procurement authority for information.
- h. Major process change notices should be submitted to the procurement authority for approval.

5.14 QA report

- a. The PCB manufacturer shall issue a QA report to the qualification authority in conformance with the DRD in Annex F.
- b. The QA report shall be issued quarterly.

5.15 Qualification renewal

- a. The PCB manufacturer shall submit to the qualification authority the following items for qualification renewal at least two months prior to expiration of the qualification:
 - 1. A PCB from a normal production batch, not older than one year, that is representative of the highest technological complexity that is qualified,
 - 2. CoC in conformance with requirement 6.4b.1,
 - 3. Coupons and microsections in conformance with clause 8.2,
 - 4. The description, drawing and review items from the PCB definition dossier in conformance with clauses A.2.1<2> , A.2.1<4> A.2.1<6> of ECSS-Q-ST-70-12,
 - 5. The justification from the PCB manufacturer for the highest technological complexity being submitted,
 - 6. The PCB manufacturer’s test report on a second identical PCB.

NOTE 1 The coupons from 5.15a.3 include an IST coupon if this is specified for the technology in accordance with requirement 8.2.3a. The coupons from 5.15a.3 also include several coupons that are untested by the PCB manufacturer, in conformance with Table 8-2. It is important that these coupons are included, as it is good practice to perform, for instance, peel strength testing for qualification renewal.

NOTE 2 The highest technological complexity is difficult to obtain on a single PCB for all design features. Therefore the PCB manufacturer justifies the selection of technology submitted for qualification renewal.

NOTE 3 It is good practice to manufacture two PCBs in a panel, one of which is evaluated by the PCB manufacturer, and the other one submitted for qualification renewal together with the required coupons.

- b. In case requirement 5.15a is not achieved because the sample is sent late, the qualification status shall be “not qualified” after the expiration date until completion of qualification renewal, including a comment to the qualification status in conformance with the requirement 5.12c.

NOTE It is good practice that the PCB manufacturer sends the sample earlier than 2 months before expiration. If the PCB manufacturer sends multiple samples at the same time, it is good practice to allow for more than 2 months for evaluation.

- c. The qualification authority shall issue a qualification renewal test report.
- d. An audit of the PCB manufacturer shall be performed by the qualification authority at least every second year.
- e. Upon successful qualification renewal, the qualification authority shall approve the qualification in conformance with the clause 5.12 and issue a new qualification letter in conformance with requirement 5.12a.
- f. The qualification authority may decide to initiate a new qualification in the following cases:
 - 1. the manufacturing was interrupted or qualification was expired for more than 2 years,
 - 2. major changes in production line and its location.

5.16 Nonconformances during qualification renewal

- a. In case nonconformances are observed during qualification renewal, the PCB manufacturer shall perform the following:
 - 1. Investigate root cause, implement corrective actions on associated processes and materials, demonstrate repeatability.

2. Investigate why nonconformance was not detected by outgoing inspection and perform training.
3. Verify how the nonconformance affects the running orders and inform customers.
4. Evaluate a new PCB and provide test report in conformance with 5.15a.6.
5. Have a new PCB sample evaluated by a third-party lab and provide test report.
6. Upon approval from the qualification authority, submit a new sample for qualification renewal.

NOTE Third-party evaluation from requirement 5.16a.5 is also specified in requirement 5.8c.

- b. In case nonconformances are observed during qualification renewal, the qualification authority should indicate the qualification status as “not qualified” until acceptable completion of the qualification renewal, including a comment to the qualification status in conformance with the requirement 5.12c, except in case of 5.16c.
- c. In case the PCB manufacturer demonstrates that nonconformances observed during qualification renewal are of a one-time occurrence, the qualification authority should indicate for a maximum period of 6 months the qualification status as “qualified” with a comment to identify the failed and ongoing qualification renewal.

NOTE 1 A one-time occurrence of a nonconformance does not invalidate the qualification of other orders in case the efficiency of outgoing inspection is verified. A one-off nonconformance is relatively straightforward to correct for and the qualification renewal of a second sample is, therefore, done within the maximum period of 6 months.

NOTE 2 Since the PCB manufacturer re-submits the sample for qualification renewal 2 months prior to the expiration of the qualification status in conformance with requirement 5.15a, this provides him with 4 months to complete remanufacture of the sample, third-party evaluation and all other actions specified in 5.16a.

- d. The qualification authority may withdraw the qualification in case:
 1. Repeated nonconformances are observed during evaluation of a PCB during qualification renewal,
 2. Repeated nonconformances are observed during audits,
 3. Repeated nonconformances are observed with respect to the quality requirements from ECSS-Q-ST-70-60.

6

QA for manufacture and procurement

6.1 Overview

This clause describes requirements on quality assurance during the procurement and the manufacturing stages of the PCB.

6.2 Procurement process

6.2.1 Overview

This clause describes various steps in the procurement process of PCBs. This is followed by the manufacturing and inspection. Table 6-1 provides an estimation of typical lead time for the various phases for a typical batch size.

Table 6-1: Example of lead time in weeks (wk) for various phases of PCB procurement, manufacture, test and inspection.

Phase	Rigid non sequential	Rigid sequential	Flex rigid	HDI
Tooling including design review and MRR	2-3 wk	2-3 wk	2-3 wk	2-3 wk
IST coupon design data	2 wk	2 wk	2 wk	2 wk
MRR approval	0,5-1 wk	0,5-1 wk	0,5-1 wk	0,5-1 wk
Manufacturing & inspection	4 wk	5-6 wk	5-6 wk	6-7 wk
IST	2,5-4 wk	2,5-4 wk	2,5-4 wk	2,5-4 wk
Total	11-14 wk	12-16 wk	12-16 wk	13-17 wk

6.2.2 Procurement specification

- a. ECSS-Q-ST-70-60 shall be used as the PCB procurement specification.

NOTE It is not good practice that the procurement authority issues his own procurement specification in which he refers to ECSS-Q-ST-70-60 as an applicable or a reference document. A reason for this is because traceability of compliance to ECSS-Q-ST-70-60 can be lost. Another reason for this is because the PCB manufacturer issues its CoC against the procurement standard and he categorises his KPIs according to the used procurement standard. In case the procurement authority desires specific additional requirements that are not covered by ECSS-Q-ST-70-60, it is good practice to include these in the PCB definition dossier or in the purchase order.

6.2.3 Quotation

- a. The procurement authority shall start the procurement process by requesting the quotation and lead time from the PCB manufacturer for tooling, production and test of a specified quantity based on the provided PCB definition dossier.

NOTE The provided PCB definition dossier can be in a draft form, as specified in requirement 5.2e of ECSS-Q-ST-70-12.

- b. The procurement authority shall maintain the PCB definition dossier under configuration control.
- c. The procurement authority should specify in the PCB definition dossier the reporting of work in progress, content and frequency.
- d. The procurement authority shall record double insulation in the PCB definition dossier.

NOTE Double insulation is specified for critical nets in conformance with requirement 13.9.2a from ECSS-Q-ST-70-12.

- e. The presence of blind-via-in-pad for soldering should be recorded in the PCB definition dossier.

NOTE This can be done by a tick box.

- f. In case the procurement authority does not define the tolerances in the PCB definition dossier, the following tolerances shall be used:

1. external dimension: $\pm 0,2$ mm,
2. thickness over dielectric: ± 10 %,
3. diameter of all hole types: $\pm 0,1$ mm,
4. external dimension for flex PCB: $\pm 0,4$ mm;
5. thickness for flex PCB: ± 20 %;

6. clearance in coverlay for flex PCB: $\pm 0,50$ mm;

NOTE Tolerance of $\pm 0,1$ mm on hole diameter is equal to Δ maximum of 0,2mm.

6.2.4 Purchase order

- a. The procurement authority shall issue the purchase order including the reference to the quotation, the ordered quantity of PCBs, the contact persons and the completed MRR checklist in conformance with Annex G of ECSS-Q-ST-70-12.
- b. The PCB manufacturer shall acknowledge the purchase order, confirm the delivery date and start the tooling activities.

6.2.5 Design review (DR)

- a. The PCB manufacturer shall initiate the DR, as specified in requirement 5.2a to 5.2g from ECSS-Q-ST-70-12 and provide compliance of the provided PCB definition dossier to the PID.

NOTE 1 This is also done at MRR which is at a later stage in the procurement. It is important that this information is available at the quotation phase.

NOTE 2 Design review includes design rule check (DRC).

NOTE 3 Design review is included within the tooling process.

6.2.6 MRR

- a. The PCB manufacturer shall complete the MRR checklist.

NOTE See example of MRR checklist in Annex G of ECSS-Q-ST-70-12.

- b. The PCB manufacturer shall perform the MRR in conformance with the requirements 5.2h to 5.2k from ECSS-Q-ST-70-12.
- c. The PCB manufacturer and procurement authority shall review during the MRR as a minimum the following aspects:
 1. Design review of PCB definition dossier including review items
 2. Traceability of any design modifications
 3. Build-up
 4. Panelisation, placement of coupons and PCBs in the panel
 5. Risk assessment
 6. Compliance to ECSS-Q-ST-70-12
 7. Compliance to ECSS-Q-ST-70-60
 8. Compliance to PID recorded in PCB approval sheet part 2 from Annex G.2.1b.

NOTE For the risk assessment, it is good practice to use a risk rating from 1 to 5. At a risk rating until 3 it is typical that the PCB manufacturer endorse the responsibility of the risk. At a risk rating of 4 or 5 it is typical that the procurement authority endorses the responsibility of the risk. At a risk rating from 3 to 5 it is good practice to involve the project for acceptance of the risk, because there can be a potential schedule impact.

- d. In case more than three prepreg sheets are used between layers, it shall be a review item in the MRR.

NOTE More than three prepreg sheets can be used in case a large volume to be filled with resin while maintaining a specific dielectric thickness, such as for thick copper layers or blind vias.

6.3 Final and in-process inspection

- a. The PCB manufacturer shall demonstrate that the available manpower and equipment are able to perform the final and in-process inspection.

NOTE The verification of this requirement is performed during the audit.

- b. The PCB manufacturer shall include coupons on the panel for in-house quality control.

NOTE The panel also includes coupons for batch release and spare coupons. These are described in clause 8.

- c. Visual standards that specify the quality characteristics shall be available to each inspector.

NOTE Visual standards for final inspection can consist of photos or drawings of microsections, which are given in clause 10.

- d. Work instructions shall specify the processes for which an in-process inspection is performed.

- e. Work instructions shall specify the methodology for final inspection in conformance with clause 8.

- f. In-process inspection shall be specified in the PID , at least for the following processes:

1. Microvia laser drilling, to verify the diameter to the capture pad in conformance with requirement 11.4.2g of ECSS-Q-ST-70-12;
2. Microvia cleaning, to verify its efficiency;
3. Etching, to verify the tolerances on track width and spacing;
4. The AOI process, to verify its efficiency by calibration;

5. Coverlay bonding, to verify the aspect of flex laminate and coverlay in conformance with Table 10-51 and the absence of overlap of coverlay and pads in conformance with Table 10-16 Ref. c;
6. Thickness measurements after lamination.

NOTE 1 For microvia laser drilling and microvia cleaning in process 6.3f.1 and 6.3f.2, a homogeneous dielectric thickness in microvia layers is necessary to avoid nonconformances such as interconnect defect. The local thickness of dielectric can be affected by the designed footprint and the tolerances of prepreg thickness.

NOTE 2 This requirement specifies which processes are verified by in-process inspection. The work instructions referenced in the PID specify the verification method, in conformance with D.2.1.1a.8.

- g. Comparison of lay-out to the drawing from the PCB definition dossier shall be performed to verify presence of plated and non-plated holes and milling.
- h. The PCB manufacturer shall specify in its PID an approach for TMA measurements to determine Tg and CTE in Z-direction, including frequency of test and material and technology of test vehicle.

NOTE This test is specific for a build-up and for the used process equipment.
- i. The PCB manufacturer shall specify in its PID the range of etchback.
- j. In-process control by IST testing shall be in conformance with clause 9.5.5.2.1.

6.4 Quality records for manufacture and procurement

- a. The PCB manufacturer shall retain the quality records for at least ten years and in accordance with business agreement requirements.
- b. The quality records shall be composed of the following:
 1. Documentation of the final inspection of manufactured PCBs, including CoC and lab reports in conformance with Annex B;
 2. Nonconformance reports and corrective actions in conformance with ECSS-Q-ST-10-09;
 3. Qualification test reports, in conformance with requirement 5.10c;
 4. Traveller;
 5. Batch summary statistics;
 6. Process records.

NOTE Process records typically include SPC of chemical processes, maintenance and calibration records.

- c. Non-nominal performance of equipment, materials or processes shall be documented including the following topics:
 - 1. Root cause investigation;
 - 2. Corrective action;
 - 3. Effect on previous, ongoing and future manufacturing batches;
 - 4. Assessment by QA personnel.

NOTE These topics are the same as for an NCR in conformance with ECSS-Q-ST-10-09.
- d. The PCB manufacturer shall maintain a database for calibration of electrical and mechanical manufacturing and test equipment.
- e. The PCB manufacturer should provide to the procurement authority the list of nonconformances specific to them, as reported quarterly in the QA report in conformance with F.2.1a.3.

6.5 Control of materials and chemistry

- a. The base materials shall be in conformance with clause 5 from ECSS-Q-ST-70.
- b. The base materials shall be in conformance with IPC-4101E for rigid laminates, IPC-4103A for RF laminates, IPC-4204A for flexible laminates and IPC-4203A for coverlay.
- c. In case of double insulation in conformance with requirement 6.2.3d, the base materials for rigid laminates and prepreg shall be in conformance with IPC-4101E Appendix A.

NOTE Double insulation is specified in clause 13.9 of ECSS-Q-ST-70-12. Annex I describes the more stringent cleanliness requirements for prepreg and laminate from IPC-4101E Appendix A.
- d. Base materials in conformance with IPC-4101E Appendix A shall be manufactured by a laminate supplier that is listed in the IPC QPL or that passed a specific audit from the PCB manufacturer.
- e. For requirement 6.5b, newer revisions of the referenced IPC standards may be used in case raw materials can only be procured in conformance to those newer revisions.
- f. For requirement 6.5c and 6.5d, newer revisions of the referenced IPC-4101E standard may be used in case
 - 1. raw materials can only be procured in conformance to those newer revisions, and
 - 2. it is in conformance with Appendix A from IPC-4101E.

NOTE The text from Appendix A of IPC-4101E is included in Annex I.