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Space engineering — Spacecraft discrete interfaces

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National foreword

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The UK participation in its preparation was entrusted to Technical Committee ACE/68, Space systems and operations.

A list of organizations represented on this committee can be obtained on request to its secretary.

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Raumfahrttechnik - Diskrete Schnittstellen in
Raumfahrzeugen

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Foreword

This document (EN 16603-50-14:2014) has been prepared by Technical Committee CEN/CLC/TC 5 “Space”, the secretariat of which is held by DIN.

This standard (EN 16603-50-14:2014) originates from ECSS-E-ST-50-14C.

This European Standard shall be given the status of a national standard, either by publication of an identical text or by endorsement, at the latest by March 2015, and conflicting national standards shall be withdrawn at the latest by March 2015.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any EN covering the same scope but with a wider domain of applicability (e.g. : aerospace).

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1

Scope

This standard specifies a common set of spacecraft onboard electrical interfaces for sensor acquisition and actuator control. The interfaces specified in this standard are the traditional point-to-point interfaces that are commonly used on modern spacecraft.

The interfaces specified in this standard include analogue and discrete digital interfaces used for status measurement and control, as well as point-to-point serial digital interfaces used for digital data acquisition and commanding of devices.

This standard specifies:

- interface signal identification;
- interface signal waveforms;
- signal timing requirements;
- signal modulation;
- voltage levels;
- input and output impedance;
- overvoltage protection requirements;
- bit ordering in digital data words;
- cabling requirements where appropriate.

This standard does not cover:

- connector requirements;
- digital data word semantics;
- message or block formats and semantics.

Connector requirements are not covered because these are normally mission or project specific. The goal of this standard is to establish a single set of definitions for these interfaces and to promote generic implementations that can be re-used throughout different missions.

When referred, the present standard is applicable as a complement of the already existing interface standards ANSI/TIA/EIA-422B-1994 and ITU-T Recommendation V.11 (Previously “CCITT Recommendation”) – (03/93).

Guidance for tailoring of the present standard can be found in Annex A.

This Standard may be tailored for the specific characteristics and constraints of a space project in conformance with ECSS-S-ST-00.

Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this ECSS Standard. For dated references, subsequent amendments to, or revisions of any of these publications, do not apply. However, parties to agreements based on this ECSS Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references the latest edition of the publication referred to applies.

EN reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system - Glossary of terms
	ANSI/TIA/EIA-422B-1994	Electrical characteristics of balanced voltage digital interface circuits
	ITU-T Recommendation V.11 (Previously "CCITT Recommendation") – (03/93)	Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s

NOTE This document is technically equivalent to ANSI/TIA/EIA/422B-1994.

3

Terms, definitions and abbreviated terms

3.1 Terms from other standards

For the purpose of this Standard, the terms and definitions from ECSS-ST-00-01 apply.

3.2 Terms specific to the present standard

3.2.1 accuracy

closeness of a measurement to the actual quantity being measured

NOTE For the purposes of this Standard it is expressed as percentage of the full measurement range or as an absolute value.

3.2.2 circuit

conducting path which conveys a signal across the interface from the signal source to the signal destination

NOTE A circuit includes the cable conductor, any intervening connectors, and any circuit elements such as protection resistors and coupling capacitors, which make up the signal path.

3.2.3 DHS data interchange bus

underlying communication medium which connects the DHS core elements

NOTE This can consist of more than one physical bus.

3.2.4 DHS core element

component of a data handling system which has a direct connection to the DHS data interchange bus

NOTE E.g.: bus controllers and remote terminals.

3.2.5 DHS peripheral element

component of a data handling system which does not have a direct connection to the DHS data interchange bus

NOTE E.g.: sensors and actuators.

3.2.6 ground displacement voltage

voltage difference between source and receiver ground references

NOTE Users are encouraged to use this definition instead of 'common mode voltage' that is not correct when referring to the academic definition.

3.2.7 time reference point

point at which a time interval starts or ends

NOTE It is the mid point between the nominal high and nominal low signal voltages.

3.3 Abbreviated terms

For the purpose of this standard, the abbreviated terms of ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
A/D	analogue to digital
ADC	analogue digital converter
ASM	analogue signal monitor
BDM	bi-level discrete monitor
BSD	bi-directional serial digital
BSM	bi-level switch monitor
CM	common mode
DHS	data handling system
HPC	high power command
HC-HPC	high current high power command
HV-HPC	high voltage high power command
ISD	input serial digital
LPC	low power command
LPC-P	low power command, pulsed
LPC-S	low power command, static
LSB	least significant bit
LV-HPC	low voltage high power command
MSB	most significant bit
OBDH	on-board data handling
OSD	output serial digital
TSM	temperature sensors monitor

3.4 Conventions

3.4.1 Bit numbering convention

The most significant bit of an n-bit field is:

- numbered bit 0 (zero),
- the first bit transmitted, and
- the leftmost bit on a format diagram.

The least significant bit of an n-bit field is:

- numbered bit n-1,
- the last bit transmitted, and
- the rightmost bit on a format diagram.

This convention is illustrated in Figure 3-1.

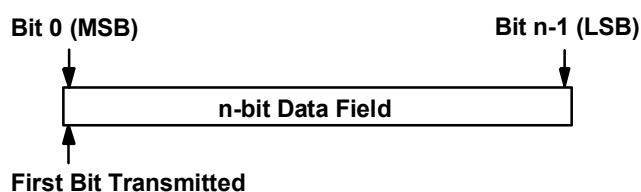


Figure 3-1: Bit numbering convention

3.4.2 Timing diagram conventions

Timing diagrams are always drawn with the earliest time on the left and time advancing to the right.

Where an event, such as a transition, in one signal causes an event in another, the two events are linked by an arrow with the tail of the arrow on the causal event and the head of the arrow on the resultant event.

Where an event in one signal is the result of an event in another signal and a qualifying condition in one or more other signals, the connecting arrow is associated with the governing condition using a bull's eye.

These conventions, together with other timing diagram symbols, are shown in Figure 3-2.

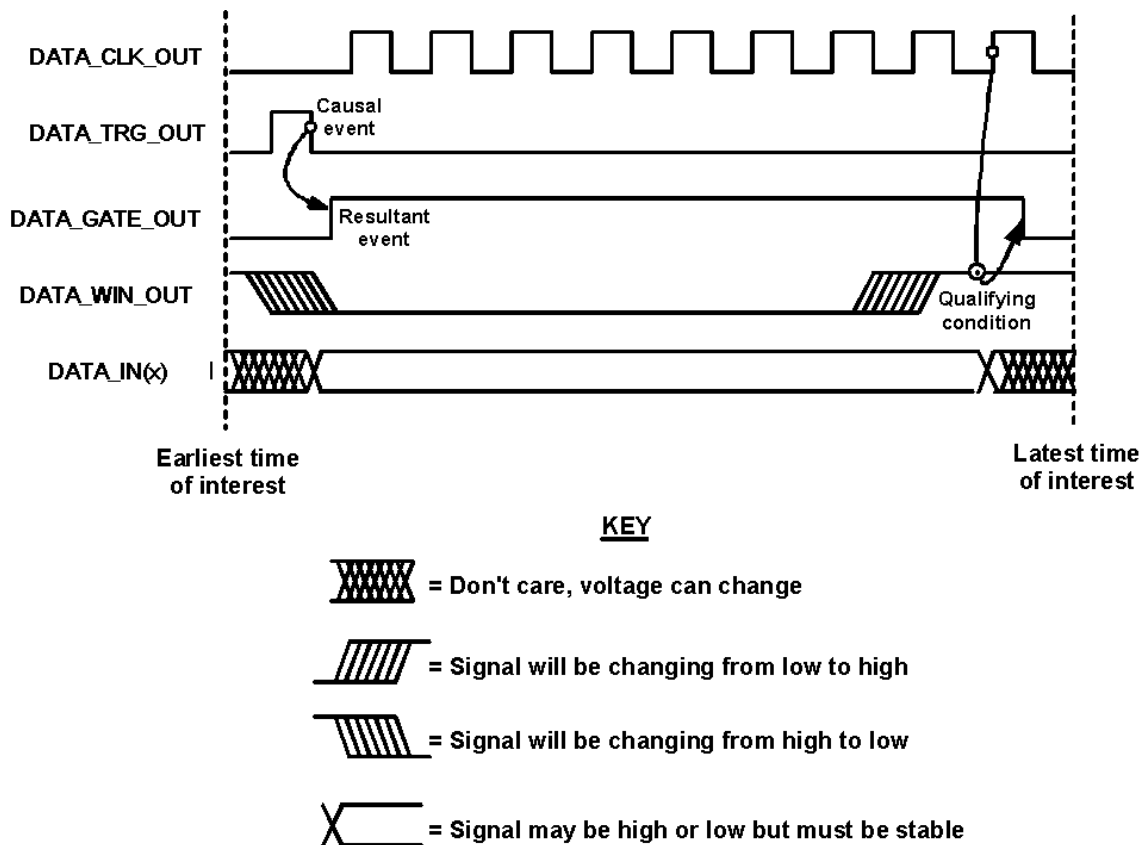


Figure 3-2: Timing diagram conventions

3.4.3 Signal and signal event naming convention

Signals are named in a manner which indicates the function of that signal. For example, a clock used for data bit sampling can be called DATA_CLK.

Control signal naming is meaningful with the function of the signal, its direction, and its assertion levels all indicated. The direction is indicated with respect to the DHS core element so that an OUT signal is an output, i.e. driven from the core element. An IN signal is an input to the core element. For example, a signal carrying data out of the core element is named DATA_OUT.

Control signal assertion or validity levels are indicated within brackets. For example, a gate output signal which is asserted when low is named GATE_OUT(L). Similarly, an input signal which indicates that a device is ready when it is high is named READY_IN(H).

Signal events such as transitions and pulses are also named symbolically using "UP" and "DOWN" indication. For example, START_{UP} indicates a rising edge event on the start signal, and STOP_{DOWN} indicates a falling edge on the stop signal. RUN_{UPDOWN} indicates a positive going pulse on the run signal, while HALT_{DOWNUP} indicates a negative going pulse on the halt signal.

3.4.4 Signal timing and measurement references

Signal rise and fall times, which are shown in Figure 3-3, are measured between 10 % and 90 % of the difference between the nominal low and nominal high signal voltages, as it can be seen in the mentioned figure.

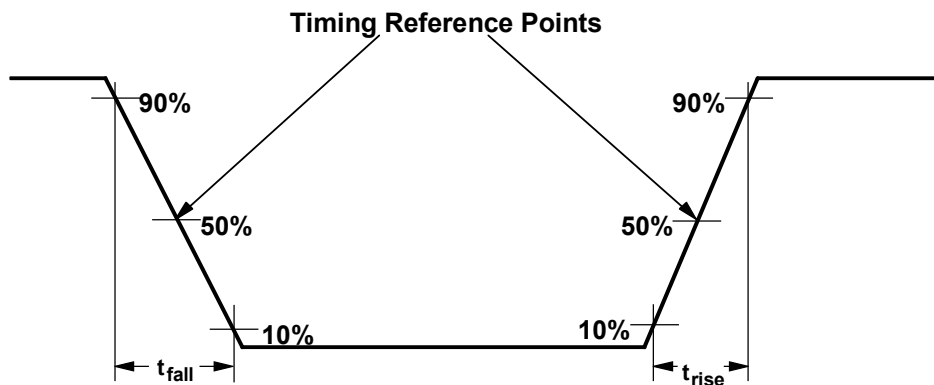


Figure 3-3: Signal timing and measurement references

4 General

4.1 Introduction

This standard defines electrical interfaces for use onboard spacecraft to connect simple devices such as sensors and actuators to the data handling system. The interfaces defined are:

- analogue signal interfaces (clause 5)
 - analogue signal monitor
 - temperature sensor monitor
- bi-level discrete input interfaces (clause 6)
 - bi-level discrete monitor
 - bi-level switch status monitor
- command interfaces (clause 7)
 - high power pulse command
 - low power command
- serial digital interfaces (clause 8).

Each interface is defined in terms of the electrical and timing characteristics of the signals comprising that interface. Connectors for the interfaces are not defined because these are often highly project dependent. Cabling characteristics are defined where appropriate.

For the serial digital interfaces, the data content of the digital words is not defined since this is the subject of higher level protocol standards beyond the scope of this Standard.

Unless otherwise stated, specified performances are applicable when both source and receiver are powered.

4.2 Architectural concepts

4.2.1 Overview

The interfaces specified in this Standard are intended to connect DHS core elements to DHS peripheral elements as shown in Figure 4-1. However, there are no technical reasons to prevent these interfaces being used between core

elements where it is appropriate to do so, and this Standard does not preclude such a configuration.

A peripheral element can have more than one user interface and also user interfaces of different types, depending on its function and design. For example, some sensors can set threshold levels or sensitivities by means of data written to them. In this case that sensor can use an output serial digital interface to write the data in addition to an input serial digital interface to read the sensor value. Alternatively, some devices are signalled to indicate that they are commanded to acquire a data sample. In that case they can use a serial digital interface together with a pulse interface.

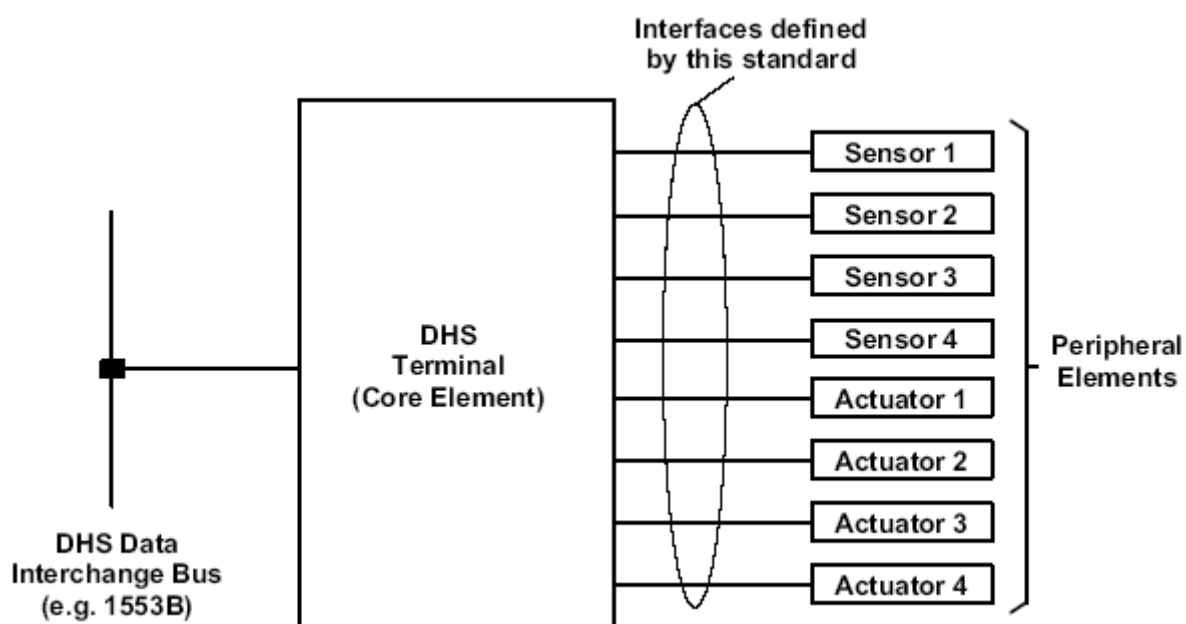


Figure 4-1: Architectural context of interfaces defined in this standard

4.2.2 General failure tolerance

4.2.2.1 Input interfaces

- a. Among other failure cases, receivers shall:
 1. Not be stressed and not show degraded performance when input is open circuit except on the input I/F that is open circuit.
 2. Not be stressed and not show degraded performance when input is short circuit to ground except on the input I/F that is short circuit.

NOTE No specific performance requirements are imposed while in this status.

4.2.2.2 Output interfaces

- a. Among other failure cases, transmitters shall:
1. Not be stressed and not show degraded performance when output is open circuit except on the output I/F that is open circuit.
 2. Not be stressed when output is short circuit to ground.

NOTE No specific performances requirement is imposed while in this status.

4.2.3 Interface control during power cycling

4.2.3.1 Input interfaces

- a. Input interfaces shall not be damaged or harmed during power cycling conditions taking the transmitting side state into account in any normal state or applicable failure condition.
- b. Receivers shall not deliver power to the other circuits or be stressed when the unit is OFF while connected to an active driver.

NOTE No specific performance requirements are imposed while in this status.

4.2.3.2 Output interfaces

- a. Output interfaces shall not be damaged or harmed during power cycling conditions when the receiving side state is in any normal state or specified failure condition.

NOTE No specific performance requirements are imposed while in this status.

- b. For pulse commands it shall be ensured that spurious commands are not emitted during power cycling that exceed activation limits for the receivers.

NOTE 1 For pulse commands, see Clause 7.

NOTE 2 This requirement does not specify the prevention of spurious pulses, but ensures either that:

- spurious pulses are below the threshold for the receiver, or
- the spurious pulse duration is short enough to not drive the load into activation (for example a relay coil or opto-coupler diode).

4.2.4 Cross-strapping

4.2.4.1 General

- a. For 2 units (UNIT_1 & UNIT_2), that can be used in redundancy, the cross-strapping of drivers and receivers shall be as specified in Figure 4-2, and meet the following conditions:
 1. The UNIT_2_A I/F is capable to receive:
 - (a) A signal from the UNIT_1_A I/F through a dedicated link
 - (b) A signal from the UNIT_1_B I/F through a dedicated link
 2. The UNIT_2_B I/F shall is capable to receive:
 - (a) A signal from the UNIT_1_A I/F through a dedicated link
 - (b) A signal from the UNIT_1_B I/F through a dedicated link
 3. The UNIT_1_A I/F is capable to deliver:
 - (a) A signal to the UNIT_2_A I/F through a dedicated link
 - (b) A signal to the UNIT_2_B I/F through a dedicated link
 4. The UNIT_1_B I/F is capable to deliver:
 - (a) A signal to the UNIT_2_A I/F through a dedicated link.
 - (b) A signal to the UNIT_2_B I/F through a dedicated link.
- b. To achieve full cross-strapping benefits, in terms of reliability, any potential common failure of UNIT_1_A and UNIT_1_B drivers and UNIT_2_A and UNIT_2_B receivers shall be avoided.

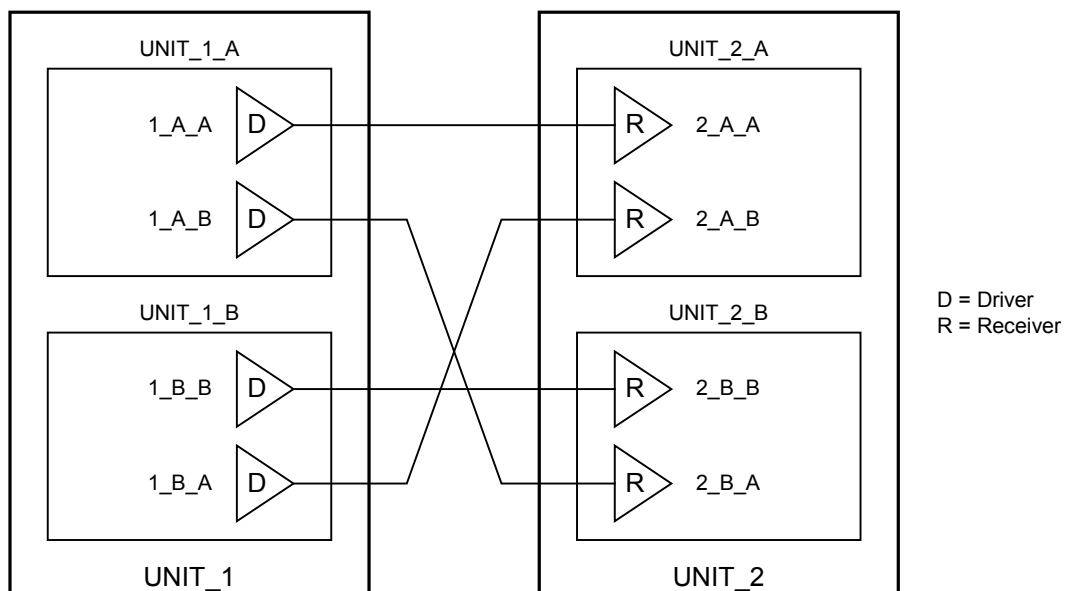


Figure 4-2: General scheme of redundant unit's cross-strapping

4.2.4.2 Immunity at UNIT_2 level

- a. Under the condition (Receiver = ON linked to Transmitter = OFF of UNIT_1), in the configuration where UNIT_1 driver is OFF and UNIT_2 receiver is ON, the information received by this receiver shall not disturb the valid information received by the other receiver (linked to a Transmitter ON).

NOTE In this configuration the electrical status at receiver output is stable (due to hysteresis) but possibly unknown (logical "1" or "0").

- b. It should be ensured that any input signal is in a known (inactive) stable state when driver is OFF.
- c. If 4.2.4.2b is not met, a validation / inhibition stage at the receiver output of UNIT_2 should be implemented.

NOTE For example, the validation of the path can be made by a dedicated direct command arriving from UNIT_1, which inhibits the UNIT_2 receiver output unused (if such a configuration has been thoroughly designed with respect to failure cases).

4.2.4.3 Protections at UNIT_1 driver level

- a. Under the condition (Transmitter = OFF linked to Receiver = ON of UNIT_2), whether powered or not, UNIT_1 drivers shall withstand any receiver characteristics as described in Clauses 5 to 8.

4.2.4.4 Protections at UNIT_2 receiver level

- a. Under the condition (Receiver = OFF linked to Transmitter = ON of UNIT_1), whether powered or not, UNIT_2 receivers shall withstand any driver characteristics as described in Clauses 5 to 8.

4.2.5 Harness cross-strapping

4.2.5.1 Overview

Harness cross-strapping is applied when heritage units, without classical cross-strapping interfaces, are used, in the case that a single redundant unit is interfaced to both a nominal and redundant system. If the spacecraft is severely mass-limited, harness cross-strapping can be used instead.

Harness cross-strapping can be used in two configurations:

- Single source – Dual receiver configuration, as shown in Figure 4-3.
- Dual source – Single receiver configuration, as shown in Figure 4-4.

The Single source – Dual receiver configuration is typically applied for BSM interfaces as described in clause 6.2.

The Dual source – Single Receiver configuration is typically applied for HPC interfaces as described in clause 7.1.

Note that this harness cross-strapping can be performed by galvanic connections in harness, as indicated in Figure 4-3 and Figure 4-4. However, the equivalent configuration applies in case the physical inter-connection is performed either within the source or within the receiver unit. The general rules and protections as mentioned in this clause 4.2.5 apply then also for those cases.

Possible problems that can be introduced by harness cross-strapping include failure propagation, loading and leakage injection of the active I/F by the redundant, inactive circuit such that the active circuit does not meet its performance requirements, incompatibility of protection circuitry of a given circuit with either the Receiver I/F circuit or the Driver (see Figure 4-4) I/F circuit. Note that in general it is important to consider loading by the redundant, inactive circuit also when powered off, even if the inactive circuit is normally powered (hot redundancy).

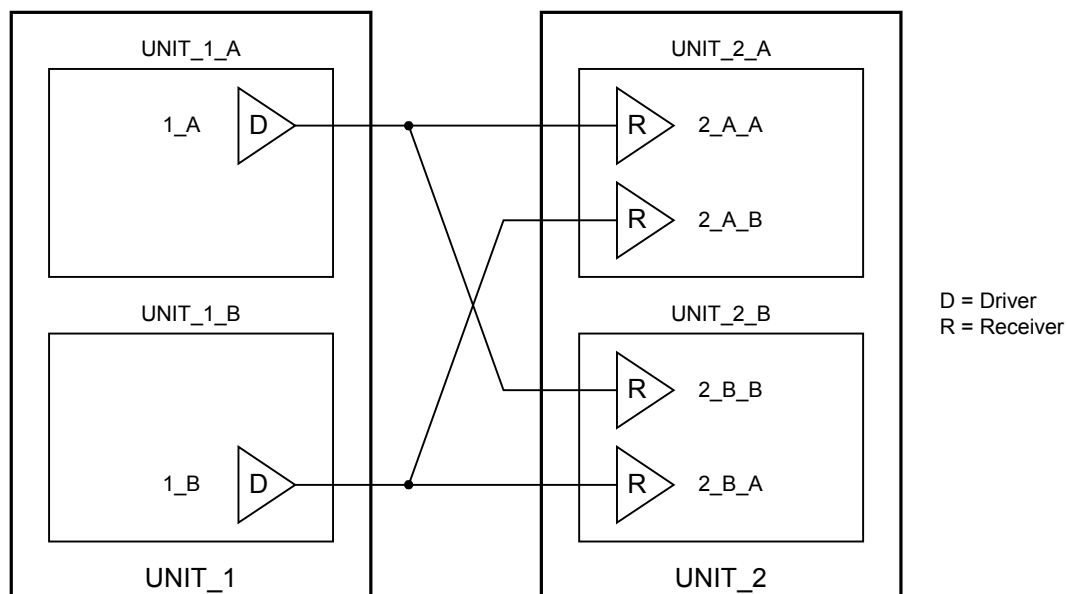


Figure 4-3: Example scheme for Single source – Dual receiver cross-strapping

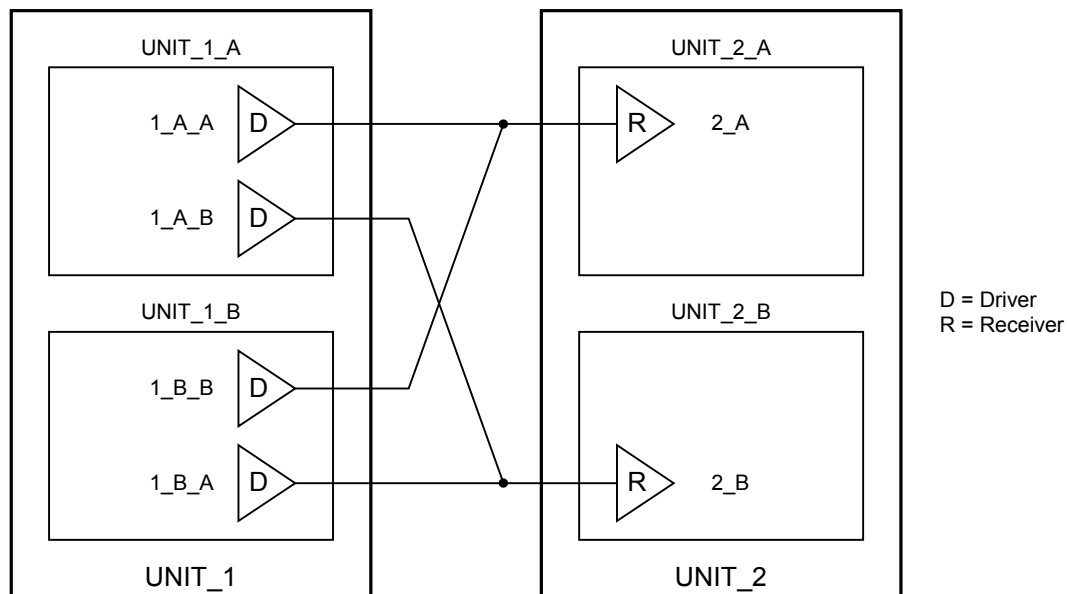


Figure 4-4: Example scheme for Dual source – Single receiver cross-strapping

4.2.5.2 Provisions

- a. If harness cross-strapping is used, there shall be no mechanism whereby the failure of either the receiver or unit interface can propagate to the I/F of another, unrelated unit.

NOTE This requirement refers to a common mode failure where a failure of one interface then propagates inside the receiver thereby affecting units unrelated to the original failure.

- b. If harness cross-strapping is used, the calculation of the overall system reliability shall include the potential degradation or damage of the I/F of a redundant unit due to the failure of other interface.

NOTE This requirement refers to the failure on a nominal unit causing the inoperability of the cross-strap. This means that there is a reduction in the possible reliability of the cross-strap.

- c. If harness cross-strapping is used, the capability shall be provided to shut down the inoperable unit regardless of the failure mode

NOTE This implies that the power can be removed from the unit by independent means such as disabling the power interface at the power distribution unit (e.g. with the means described in clause 4.2.4.2)

- d. Under the condition (Transmitter = OFF linked to Receiver = ON of UNIT_2), whether powered or not, UNIT_1 drivers shall withstand any receiver characteristics as described in Clauses 5 to 8.

- e. Under the condition (Receiver = OFF linked to Transmitter = ON of UNIT_1), whether powered or not, UNIT_2 receivers shall withstand any driver characteristics as described in Clauses 5 to 8.

4.2.6 Cable capacitance

It is important that the DHS interfaces consider the capacitive loading by the harness. Figure 4-5 defines the capacitances involved for a twisted shielded pair cable.

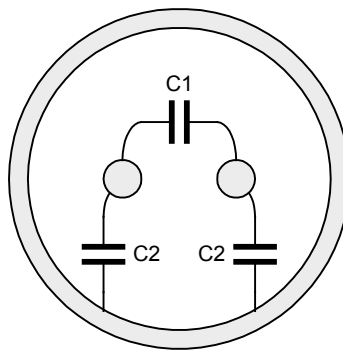


Figure 4-5: Cable capacitance definitions

Effective capacitances can then be calculated according to:

- Core to core capacitance $C_{CC} = C1 + \frac{C2}{2}$
- Core to shield capacitance $C_{CS} = C2 + \frac{C1 \cdot C2}{C1 + C2}$
- Core to core capacitance with shield connected to one core $C_{CT} = C1 + C2$

Note that the latter case applies typically when either the source or the receiver is single ended, which implies that both the shield and one of the core wires are grounded.