

**Harmonized system of quality
assessment for electronic components**

Generic specification: Monolithic integrated circuits

The European Standard EN 190000:1995 has the status of a
British Standard

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- British Telecommunications plc
- Federation of the Electronics Industry
- Ministry of Defence
- National Supervising Inspectorate (BSI PC)

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National foreword

This British Standard has been prepared by Subcommittee EPL/47/5 and is the English language version of EN 190000:1995, *Generic specification: Monolithic integrated circuits* published by the European Committee for Electrotechnical Standardization (CENELEC). It supersedes BS CECC 90000:1991 which is declared obsolescent; BS CECC 90000:1991 remains valid for existing approvals, but may not be used for any new approvals.

Cross-references

Publication referred to	Corresponding British Standard
ISO 1000:1973 ^a	BS 5555:1993 <i>Specification for SI units and recommendations for the use of their multiples and certain other units</i>
IEC 50	BS 4727 <i>Glossary of electrotechnical, power, telecommunication, electronics, lighting and colour terms</i>
IEC 68	{ BS 2011 <i>Environmental testing</i> BS EN 60068 <i>Environmental testing</i>
IEC 148:1969	
IEC 191	BS 3363:1980 <i>Specification for letter symbols for semiconductor devices and integrated microcircuits</i>
IEC 617	BS 3934 <i>Mechanical standardization of semiconductor devices</i>
IEC 617-12:1991	BS 3939 <i>Graphical symbols for electrical power, telecommunications and electronics diagrams</i>
IEC 617-13:1993	Part 12:1991 <i>Guide for binary logic elements</i>
IEC 747	BS EN 60617 <i>Graphical symbols for diagrams</i>
IEC 747-1:1983	BS EN 60617-13:1993 <i>Analogue elements</i>
IEC 747-10:1991	BS 6493 <i>Semiconductor devices</i>
QC 700000:1991	Part 1 <i>Discrete devices</i>
IEC 748	Section 1.1:1984 <i>General</i>
IEC 748-1:1984	BS QC 700000:1991 <i>Harmonized system of quality assessment for electric components. Semiconductor devices. Generic specification for discrete devices and integrated circuits</i>
IEC 748-2:1985	BS 6493 <i>Semiconductor devices</i>
IEC 748-3:1986	Part 2 <i>Integrated circuits</i>
IEC 748-4:1987	Section 2.1:1985 <i>General</i>
IEC 749:1984	Section 2.2:1986 <i>Recommendations for digital integrated circuits</i>
CECC 00007:1978	Section 2.3:1987 <i>Recommendations for analogue integrated circuits</i>
CECC 00114	Section 2.4:1989 <i>Recommendations for interface integrated circuits</i>
ENV 190000-6:1993	Part 3:1985 <i>Mechanical and climatic test methods</i>
	BS E9007:1975 <i>Specification for harmonized system of quality assessment for electronic components: Basic specification: Sampling plans and procedures for inspection by attributes</i>
	BS EN 100114:1992 <i>Rule of procedure 14. Quality assessment procedures</i>
	DD ENV 190000 <i>Generic specification: monolithic integrated circuits</i>
	DD ENV 190000-6:1994 <i>Procedure for approval and quality management</i>

^a Supersedes by ISO 1000:1992.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, the EN title page, pages 2 to 198, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Descriptors: Quality, electronic components, monolithic integrated circuits

English version

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Spécification générique: Circuits intégrés
monolithiques

Fachgrundspezifikation: Monolitische
integrierte Schaltungen

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

This European Standard was prepared by Working Group CLC/TC CECC/WG 9, *“Integrated circuits”*.

The text of the draft based on CECC 90000:1990 (Issue 4) and documents CECC(Secretariat)2739, 2740, 2741, 2567, 2565, 2570, 2644, 2668, 2669, 2566, 2645, 2646 and 3117 was submitted to the formal vote. Together with the voting reports, circulated as documents CECC(Secretariat)3187, 2632, 2631, 2674, 2784, 2790, 3189, 2726, 2785, 2786 and 3251, it was approved as EN 190000 on 1992-11-28.

This European Standard supersedes CECC 90000:1990.

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- latest date by which
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conflicting with the EN
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1 Scope

This specification specifies the terms, definitions, symbols, test methods and other material for monolithic integrated (micro)circuits¹⁾, as defined in IEC 747, necessary to prepare appropriate detail specifications (DS) in the CECC System. Supplementary requirements for different families of integrated microcircuits are included in separate specifications.

2 General

2.1 Order of precedence

Where any discrepancies occur for any reason, documents shall rank in the following order of authority:

- the detail specification (DS)
- the sectional specification (SS)
- the generic specification (GS)
- the internal regulation of the FEN e.V.
- any other international documents to which reference is made.

The same order of precedence shall apply to equivalent national documents.

2.2 Related documents

In each case the latest issue of the documents prior to the date of issue of this document is valid.

ISO 1000, *SI units and recommendations for the use of their multiples and of certain other units*.

IEC 27-1, *Letter symbols to be used in electrical technology. General*.

IEC 50, *International Electrotechnical Vocabulary*.

IEC 68, *Basic environmental testing procedures*.

IEC 134, *Rating systems for electronic tubes and valves and analogous semiconductor devices*.

IEC 148, *Letter symbols for semiconductor devices and integrated microcircuits (Chapter X)*.

IEC 617, *Graphical symbols for diagrams*.

IEC 617-12, *Part 12: Binary logic elements*.

IEC 617-13, *Part 13: Analogue elements*.

IEC 747, *Semiconductor devices — Discrete devices and integrated circuits*.

IEC 747-1, *Part 1: General*.

IEC 747-10, *Part 10: Generic specification for discrete devices and integrated circuits*.

IEC 748, *Semiconductor devices — Integrated circuits*.

IEC 748-1, *Part 1: General*.

IEC 748-2, *Part 2: Digital integrated circuits*.

IEC 748-3, *Part 3: Analogue integrated circuits*.

IEC 748-4, *Part 4: Interface integrated circuits*.

IEC 749, *Semiconductor devices: Mechanical and climatic test methods*.

IEC 191, *Mechanical standardization of semiconductor devices*.

CECC 00007, *Basic specification: Sampling plans and procedures for inspection and attributes*.

CECC 00114, *Quality Assessment Procedures*.

Internal Regulations of the FEN e.V. and CECC Rules of Procedure.

¹⁾ In the following the term “integrated circuits” is used.

2.3 Units, symbols and terminology

2.3.1 General

Units, graphical symbols, letter symbols and terminology shall, whenever possible, be taken from the following documents:

ISO 1000, *SI units and recommendations for the use of their multiples and of certain other units*.

IEC 27, *Letter symbols to be used in electrical technology*.

IEC 50, *International Electrotechnical Vocabulary*.

IEC 617, *Graphical symbols for diagrams*.

Any other units, symbols, and terminology required shall be derived in accordance with the principles of the documents listed above in **2.2**.

2.3.2 General terms for integrated circuits

- | | |
|---------------------------|--|
| — Microelectronic | IEC 748-1 chapter IV clause 1.5 |
| — Microcircuit | IEC 748-1 chapter IV clause 2.2 |
| — Integrated circuit | IEC 748-1 chapter IV clause 2.3 |
| — Integrated microcircuit | IEC 748-1 chapter IV clause 2.4 |
| — Microassembly | IEC 748-1 chapter IV clause 2.5 |

2.4 Standard and preferred values

Standard and preferred values should preferably be chosen from the relevant IEC Publications:

- | | |
|----------------|-----------|
| — dimensions | IEC 191-2 |
| — voltages | IEC 747-1 |
| — temperatures | IEC 747-1 |

Preferred values are:

– 65, – 55, – 40, – 25, 0, + 25, + 70, + 85, + 125, + 150 °C.

2.5 Marking of component and package

Apart from statutory hazard warnings which shall, if necessary, take first priority, the following shall be marked on the device, in order of precedence, as space permits. All information except the terminal marking, shall also appear on the primary package used as initial protection or wrapping for delivery.

- 1) Terminal identification (for example position of pin n° 1), (see **2.5.1**)
- 2) Type designation (standardized or commercial)
- 3) Operating temperature range [if not included in 2), in Pro-electron²⁾ code]
- 4) Quality assessment level applied (in code) followed by Z in case of devices supplied under Capability Approval
- 5) Screening class applied (in code)
- 6) Date code (year/week) of the week in which the device is encapsulated encoded into three or four digits as given in standard ISO 2015.
- 7) CECC Mark of Conformity
- 8) Manufacturer's name or trade mark (may include factory code, see **2.5.2**)
- 9) Factory identification code [if not included in 8), see **2.5.2**]
- 10) Package materials [if not included in 2), in Pro-electron²⁾ code]
- 11) Caution label for Electrostatic Sensitive Devices (see **2.5.3**)
- 12) Optional tests (in code), (see **2.5.4**)

²⁾ "Pro-electron code" means the suitable parts for temperatures and for materials from the Pro-electron type description code for integrated circuits.

2.5.1 *Terminal identification*

The terminals shall be identified in at least one of the following ways:

- in accordance with the specified outline or basic drawing
- as given in the DS.

2.5.2 *Factory identification code*

An identification code is allocated to each factory of each manufacturer whose Chief Inspector is responsible for certifying components.

The manufacturer is the allocating authority for letters and/or figures indicating the responsible centre. This code shall be published in CECC 00200 (QPL).

2.5.3 *Precautions for Electrostatic Sensitive Devices*

All integrated circuits covered by this specification are regarded as Electrostatic Sensitive Devices and as such require special packaging and handling precautions to eliminate damage or potential weakening of devices.

Devices shall be packed so that they are protected against electrostatic fields.

2.5.4 *Optional tests*

Sectional specifications (SS) may give the possibility to apply optional test(s). Each test or combination of tests is coded in the following way:

Blank: No optional test

- 1 Salt mist, see 4.6.14
- 2 Combination of optional tests of assessment level P applicable to components for use for example in telecommunication equipment.

The following optional tests are applied to components qualified to:

- CECC 90103: Sub-Groups A3a, D3
- CECC 90104: Sub-Groups A3a, B4, D3, D4
- CECC 90109: Sub-Groups A3a, B4, D3, D4

3 à 8 To be included later

- 9 Special test and/or special tests combinations not called for in the CECC System.

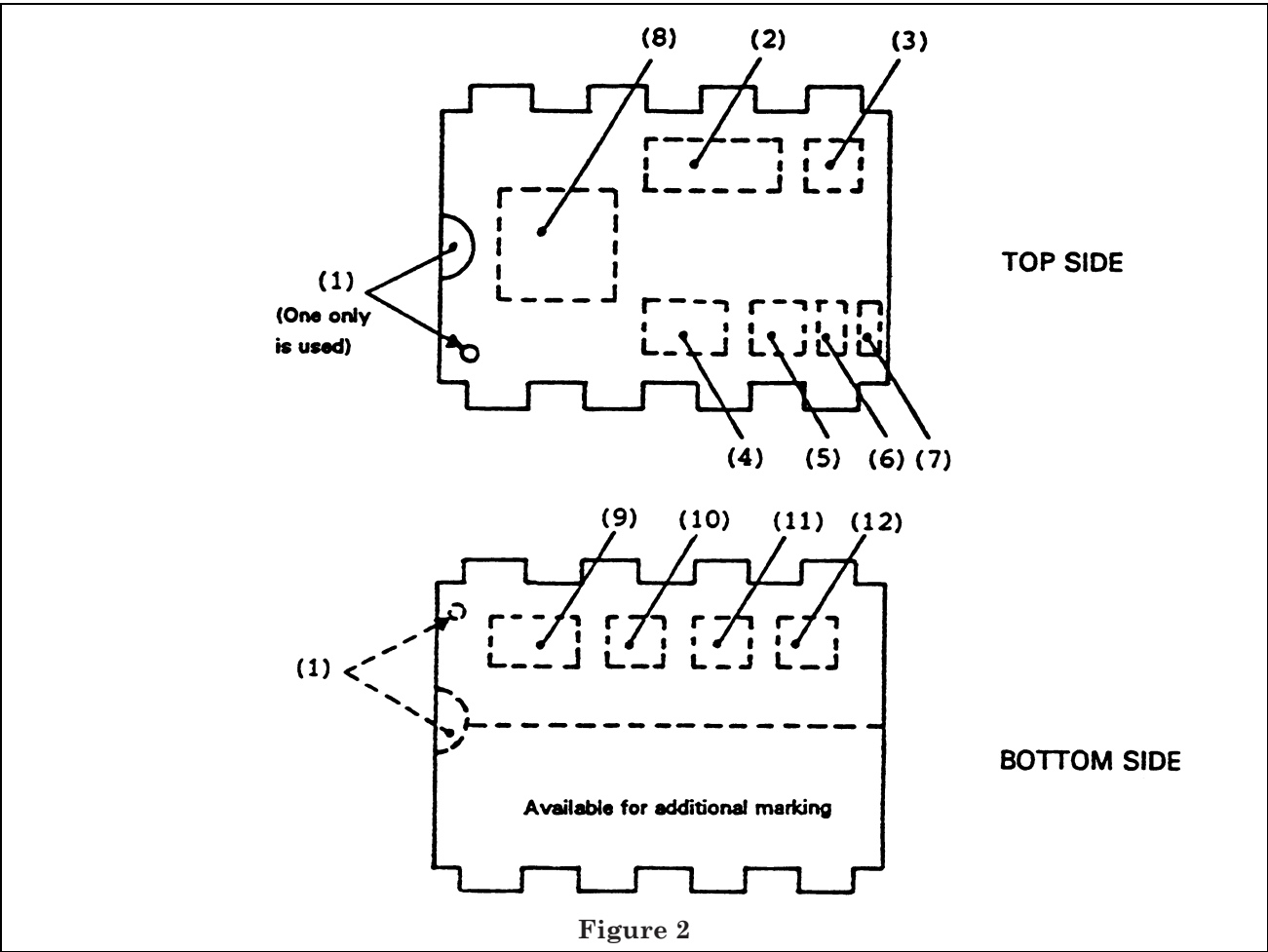
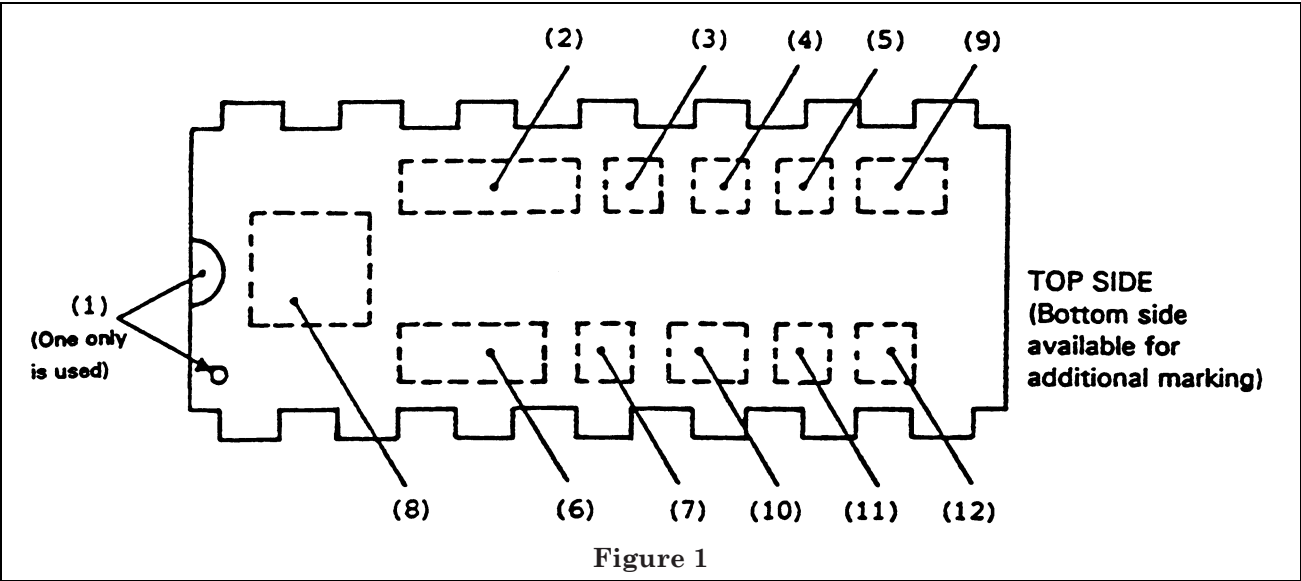
2.5.5 *Marking symbols location*

The marking symbols shall be located in the following order:

Figure 1 is an example for packages with sufficient space. The bottom side of the package is available for manufacturer's additional marking.

Figure 2 is an example for small packages. The lower part of the bottom side is available for manufacturer's additional marking.

The marking of cylindrical packages will be included later.



2.6 Ordering information

The following information shall be included in the order and also in the delivery documents. The package shall include sufficient information to relate to the delivery:

- 1) Manufacturer
- 2) Standardized or commercial type designation
- 3) Operating temperature range [if not included in 2), Pro-electron code may be used]
- 4) Required quality assessment level (in code)
- 5) Required optional test (salt mist for example), (in code, if applicable)
- 6) Required screening class (in code, if applicable)
- 7) Package shape (Pro-electron code may be used)
- 8) Package materials (Pro-electron code may be used)
- 9) Terminals metal and coating (if applicable)
- 10) Relevant DS number and, if necessary, issue and date.

Example: wording in the following order:

“N integrated circuits XXXX CD 4011B, C, Y level with optional test 1, B Class, DG package, gold plated kovar terminals to CECC 90104-XXX, issue 1 of 198x”.

means:

N integrated circuits manufactured by XXXX, type number CD 4011B, operating temperature – 55 °C to + 125 °C, under quality assessment level Y including optional test of salt mist, screened in B class, in glass sealed ceramic “dual in line” package, with gold plated kovar terminals, in compliance with DS CECC 90104-XXX, issue 1 of 198x.

3 Quality assessment procedures

3.1 Primary stage of manufacture and subcontracting

The primary stage for bipolar integrated circuits is the first process which changes the monocrystalline semiconductors material from being either wholly P-type or wholly N-type. The primary stage for MOS circuits is the first oxidation of the substrate.

When the approved manufacturer invokes CECC 00114 for subcontracting, he shall ensure that the following conditions are satisfied:

- when subcontracting is not done in one of his company’s factories, the subcontracted manufacturing processes may be either the wafer fabrication or the assembly of the device;
- the National Supervising Inspectorate (ONS) shall be satisfied that the Chief Inspector of the manufacturer who is certifying the components under the CECC System has the responsibility for inspection of the work and the inspection arrangements there;
- the Chief Inspector shall be provided with the production line process charts, the defined inspection points, the inspection requirements at each stage and the quality control requirements, together with the procedures for the transfer of the parts from the place of manufacture to the manufacturer within the CECC who is certifying the component. The ONS shall be informed and have access to this documentation and be able to verify the application of these requirements;
- any changes in inspection requirements and manufacturing procedures shall be reported back to the CECC approved manufacturer’s Chief Inspector who is certifying the components. The significant changes shall be reported by the approved manufacturer’s Chief Inspector to the ONS;
- the approved manufacturer shall perform the quality conformance inspection tests (Groups A, B, C, D) prescribed by the DS for the component he is certifying. He can perform the Groups A and B tests in a facility outside a CECC member country, provided that this facility is supervised by the ONS. Groups C and D tests shall be performed in one of his company’s factories located in a CECC member country.

On the other hand quality conformance inspection tests can be subcontracted to approved test laboratories within the CECC geographical area.

3.2 Structural similarity procedures

3.2.1 General rules

1) Purpose

Structural similarity procedures are intended to reduce the amount of testing that shall be performed for quality assessment purposes.

2) Principles

For a test applicable to a group of device types, the test may be performed on one type from the group and the results obtained are considered as representative for all the types, if the general and particular criteria for structural similarity described in this section and applicable to this test are complied with. The definition of these criteria shall be based on the principle that conformity and reliability verified on the representative type gives at least the same conformity and reliability assurance for the associated types.

Structural similarity shall not be applied for electrical and visual tests under Group A.

3) Application conditions

Tests and measurements specified in sequence.

Structural similarity procedures apply to a single test.

In a sequence of tests in a Sub-Group, excluding end point tests, the test considered to be most critical shall be used to decide the criteria for structural similarity grouping. Where there are end point tests these shall not be used to decide the structural similarity criteria, e.g. B4 tests, where Sealing or Accelerated Damp Heat are used as part of the end point test sequence for Rapid Change of Temperature.

An example of practical application of structural similarity procedures is given in Annex E of this generic specification.

4) General criteria for structural similarity

- a) The type chosen as representative for a group of types in relation to a given test may differ from period to period, depending on the types produced in that period.
- b) For all relevant types in a group of types the same accelerated test procedure shall be allowed (see 4.9).
- c) If although fulfilling the particular criteria for a group, significant difference(s) still exist in characteristic(s), the type selected for the relevant test shall be represented by the most critical device, giving the greatest risk of failure for this test.
- d) If failure occurs on a device type all the devices associated with this representative type are to be considered affected.
- e) If the circuits are submitted to a screening procedure in accordance with 4.10, they may only be grouped if they are screened according to the same screening class. However, if several screening classes are applied in the same production line, the devices screened according to a given screening class are covered by devices unscreened or screened according to a lower screening class. For this purpose the screening classes as defined in 4.10 are given in the following order: D, E, F, C, B, H, where D is lowest one.

3.2.2 Test dependent criteria for structural similarity

The test dependent criteria for structural similarity applicable to the Group B and periodic tests are given in the following table.

Sub-clauses 3.2.2 1) à 3.2.2 18), specify the interpretation of these criteria.

Test dependent criteria for structural similarity (see note)

Tests		Criteria																							
		Assembly line 3.2.2 1)			Outline and dimensions of the package 3.2.2 2)	Family of packages 3.2.2 3)	Package material 3.2.2 4)	Encapsulation methods 3.2.2 5)	External terminals material 3.2.2 6)	Finishing process 3.2.2 7)	Marking 3.2.2 8)	Number of terminals 3.2.2 9)		Material of internal connections, wire bonding 3.2.2 10)	Die bonding 3.2.2 11)	Ratio of die areas 3.2.2 12)		Diffusion line 3.2.2 1)	Die manufacturing process 3.2.2 13)	Density 3.2.2 14)	Operating supply voltages 3.2.2 15)	Operating temperature range 3.2.2 16)	Functional and electrical criterion 3.2.2 17)	Power dissipation 3.2.2 18) b)	Power dissipation 3.2.2 18) c)
B1	Mains dimensions — Mass	X			X	X	X	X	X	X															
B2	Solderability	X			X		X	X	X																
B3	Sealing test (cavity packages) ^a	X			X	X	X	X	X		X														
B4	Change of temperature	X			X	X	X	X			X		X	X	X										
B5	Electrical endurance 168 h	X			X	X	X	X	X				X	X	X			X	X	X	X	X	X	X	
C1	Secondary dimensions	X		X	X	X	X	X	X																
C2	Immersion in cleaning solvents	X				X	X			X															
C3	Robustness of terminations	X			X		X	X	X																
C4	Resistance to soldering heat	X			X	X	X	X			X		X	X	X										
C5	Shock Vibrations Acceleration steady state	X			X	X	X	X			X		X	X	X										
C6	Damp heat (cavity packages) ^a	X			X	X	X	X	X	X															
C7	Damp heat (non cavity packages)	X			X	X	X	X	X	X	X		X	X	X			X	X	X	X				X
C8	Electrical endurance 2 000 h	X			X	X	X	X	X				X	X	X			X	X	X	X	X	X	X	
C9	Storage — Dry heat 1 000 h	X			X	X	X	X	X	X			X	X				X	X						
C10	Storage — Cold 1 000 h	X			X	X	X	X	X	X			X	X				X	X						
C11a	Correlation — Dynamic tests at T _{amb} max.																	X	X	X	X	X	X	X	
C11b	Correlation — Dynamic tests at T _{amb} min.																	X	X	X	X	X	X	X	
C12a	Correlation — Functional tests at T _{amb} max.																	X	X	X	X	X	X	X	
C12b	Correlation — Functional tests at T _{amb} min.																	X	X	X	X	X	X	X	

^a cavity packages with non-organic sealing only.

^a cavity packages with non-organic sealing only.

Test dependent criteria for structural similarity (see note)

Tests		Criteria																									
		Assembly line 3.2.2 1)			Outline and dimensions of the package 3.2.2 2)	Family of packages 3.2.2 3)	Package material 3.2.2 4)	Encapsulation methods 3.2.2 5)	External terminals material 3.2.2 6)	Finishing process 3.2.2 7)	Marking 3.2.2 8)	Number of terminals 3.2.2 9)			Material of internal connections, wire bonding 3.2.2 10)	Die bonding 3.2.2 11)	Ratio of die areas 3.2.2 12)			Diffusion line 3.2.2 1)	Die manufacturing process 3.2.2 13)	Density 3.2.2 14)	Operating supply voltages 3.2.2 15)	Operating temperature range 3.2.2 16)	Functional and electrical criterion 3.2.2 17)	Power dissipation 3.2.2 18) b)	Power dissipation 3.2.2 18) c)
C13	Salt mist	X				X		X	X	X		X															
D2	Transient energy rating				X							X								X	X			X			
C14	Additional electrical characteristics																			X	X		X	X	X		

^a NOTE A cross in the table denotes that the criterion is mandatory for the corresponding test.

^a NOTE A cross in the table denotes that the criterion is mandatory for the corresponding test.

1) Production lines

The devices shall be made in the same:

- wafer fabrication (it is the set of die manufacturing processes from the primary stage to the last stage before separation of dice);
- assembly line (Assembly is the set of manufacturing process operations comprising die attach, lead bonding and encapsulation).

2) Outline and dimensions of the package

The outline and dimensions of the package defined in the DS shall be the same.

3) Family of package

To be considered as structurally similar for the family of packages, the devices shall be mounted in packages meeting the following criteria:

- same technological sub-family of package
- same form and nominal cross-section of terminals
- for all standard forms (except form 1) see IEC 191-3: same standard form and same kind
- for standard form 1, the package shall have the same single form and the same nominal dimensions, except the dimensions directly related to the number of terminals.

4) Package material

Package material shall be the same.

5) Encapsulation methods

The method for sealing the package for cavity packages or the materials and methods used for non-cavity packages shall be the same.

6) External terminals material

The material used for the external terminals including the coating shall be the same [see also 3.2.2 7)]

7) Finishing process

Excluding the marking method [see 3.2.2 8)] and final electrical measurements, finishing processes performed on the completed device shall be the same.

8) Marking methods

The method of marking and the coating applied to the package shall be the same.

9) Number of terminals

A single group of devices may be formed provided that the maximum difference ($D_{\max}$) between the minimum and the maximum number of terminals in such group is in relationship with the maximum number of terminals (N) existing in this group.

The maximum difference shall be:

$$D_{\max} = \frac{N}{4}$$

10) Material of internal connections and lead bonding

The material of the internal connections, their nominal cross-section and the nature of bonding pads shall be the same. The bonding methods shall also be the same.

11) Die bonding

The methods and materials used for attachment of the die shall be the same.

12) Die areas

The die area of associated types must not be greater than 2 times that of the type which is tested.

13) Die manufacturing process

The dice shall be produced according to the same process, i.e.:

- the basic technology and the basic process are the same (example: Schottky, N MOS, C MOS, etc.)
- the type of passivation is the same
- the same lay-out rules and design data
- the cells or basic components used to perform the elementary function are the same
- the method and material of the metallization are the same
- the number of metallization layers is the same
- the substrate material and characteristics are the same

14) Density

The density of a device is the ratio between the number of elements and the die area as given by the formula:

$$D_c = \frac{\text{Number of elements}}{\text{Area}}$$

The definition of the element is not important, provided in a group of types the same definition is used when structural similarity rules are applied.

The density of associated types shall be less than twice that of the device which is tested.

15) Operating supply voltages

Operating supply voltages specified in the FS and/or in the DS for the relevant test shall be the same.

16) Operating temperature

Operating temperatures specified in the FS and/or the DS for the relevant test shall be the same.

17) Functional and electrical criteria

In a structural similarity grouping, all the device types shall be specified based on the same BDS.

18) Power dissipation

a) Definition

Unless otherwise specified in the FS the power dissipation is defined as the nominal calculated power dissipated by the associated types for the relevant test.

b) Criterion for electrical endurance and correlation tests

The power dissipation of associated types shall normally be maximum 1.2 times that of the device which is tested. However the maximum limit may be increased provided the rise of the junction temperature is not greater than 5 °C. The minimum is not limited.

c) Criterion for humidity tests with bias

The power dissipation of associated types shall be minimum 0.8 times that the device which is tested. The maximum is not limited.

3.3 Qualification approval procedure**3.3.1 Definition of production lot and inspection lot**

Unless otherwise prescribed, a production lot consists of devices having the same design, manufactured on the same production line only differing by a selection based on electrical characteristic limits, and normally assembled during one week.

Where the word lot is used unqualified it shall be taken to mean inspection lot.

The devices forming an inspection lot shall be of one type produced in a uniform manufacturing process³⁾ and shall have been through the assembly process within one month or four consecutive weeks.

An inspection lot consists of either:

— Maximum 15 000 devices originating from maximum 5 wafer lots⁴⁾

or

— The maximum number of devices calculated from the formulae given below, provided that:

- all the devices originated from one wafer lot⁴⁾
- the marking on each device allows traceability to the relevant wafer lot⁴⁾.

Formulae for calculating the maximum size of an inspection lot:

$$L_S = 60\,000 \times (D_W - 2) \text{ if } D_A \text{ up to } 6.5 \text{ mm}^2$$

$$L_S = 30\,000 \times (D_W - 2) \text{ if } D_A \text{ larger than } 6.5 \text{ mm}^2$$

with L_S : maximum size of inspection lot

D_W : wafer diameter in millimeters

$$S_W : \text{wafer size} = \frac{D_W}{25.4} \text{ and } S_W \geq 3$$

D_A : die area

Examples: see table.

Wafer diameter (mm) (D_W)	Wafer size (S_W)	Maximum size of inspection lot for	
		$D_A \leq 6.5 \text{ mm}^2$	$D_A > 6.5 \text{ mm}^2$
76.2	3	60 000	30 000
101.6	4	120 000	60 000
127.0	5	180 000	90 000
152.4	6	240 000	120 000

3.3.2 Approval procedure

The procedure specified for the purposes of qualification approval shall be based on the use of the quality conformance inspection whereby three consecutive lots are subjected to lot-by-lot inspection for Groups A and B and one sample (drawn from all three lots) subjected to Group C periodic inspection.

Where structurally similar devices are currently approved, the relevant Group B and C tests may be omitted.

Samples shall be taken from the lots in accordance with IEC 410. For Group A tests, normal inspection must be used, but if the sampling size gives acceptance on zero defective, a higher sampling size may be used to accept on one defective.

³⁾ Definition under consideration

⁴⁾ A wafer lot is defined as consisting of maximum the number of wafers that have been subjected to all necessary wafer fabrication steps as a single group.

The sectional specification shall specify the regrouping of lots. Unless already prescribed in the DS, the qualification approval for multiple integrated circuits shall include tests to check any presence of interaction between functionally independent sections.

Devices subjected to tests indicated “destructive” (D) shall not be included in the lot for delivery. Devices subjected to “non-destructive” (ND) tests may be delivered provided they are re-tested to Group A requirements and satisfy them.

3.3.3 Major alterations

1) Definition of major alterations

Any change in process technology which could affect the quality or performance of a product supplied to an approved CECC specification, or which could require a product to be transferred from one structural similarity group to another (new or existing) group.

2) Procedure in the event of a major alteration

No major alteration of material, piece parts or manufacturing procedure shall be made without prior notification and the demonstration by sufficient test evidence to the supervising inspectorate [see 3.3.3 3)] that the major alteration does not reduce the quality or performance of the components below the specified requirement.

3) Re-qualification procedure

The re-qualification procedure consists of Group A and B testing on samples from three consecutive lots, and Group C testing on one sample representative of the three. It is necessary only to apply those Sub-Groups agreed with the ONS as necessary to reveal possible or required differences resulting from the relevant alteration.

The procedure shall be completed with a report acceptable to the ONS.

3.3.4 Examples of major alterations

1) Chip mounting

- major alteration of alloying to solder or glue mounting, or
- changing of brass solder to solder, and vice versa

Not considered as major alterations: equipment change without changing the technology, or the use of preform instead of gold plate alloy surfaces.

2) Crystal passivation

- major alterations of the passivation material, for example the use of silicon-nitride instead of silicon-oxide
- or the change of the sequence of the passivation layers.

Not considered as major alterations: changing of the process for applying the passivation layer.

3) Case material

- major alterations of case material, for example, the change of glass to plastic cases
- or major alteration of plastic A to plastic B
- or major alteration of glass to sinter glass
- or alteration of plastic fillmass A to plastic fillmass B.

Not considered as a major alteration: changing of the colloid temperature less than 50 °C (for epoxide envelopes).

4) Metallization

- major alterations of the metals and layer sequence, for instance gold instead of aluminium metallization.

5) Chip size and/or chip lay-out

- major alterations of lay-out (design and size) which influence the active zone including guard ring and barrier layer (as far as they belong to the active zone of the crystal)
- basic alterations of the contact surface, for instance by change to overlay contacts.

Not considered as major alterations: the change of position and design of the adjustment marks, design and size changes of the contact surfaces, changes of the edge lengths of the crystal, which do not influence the active zone.

6) Bonding

- major alterations of the bonding process, for example thermo-compression instead of the ultrasonic method
- or changing the material for bonding, for example gold bond wire instead of aluminium wire
- or change of the nominal diameter of the bond wire.

3.4 Quality conformance inspection**3.4.1 Division into Groups and Sub-Groups**

— Group A inspection

Group A prescribes the visual examination and the electrical measurements to be made on a lot-by-lot basis to assess the principal electrical properties of a circuit (see CECC 00114).

Group A inspection is divided into appropriate Sub-Groups.

— Group B inspection

Group B prescribes the procedures to be used on a lot-by-lot basis to assess certain additional properties of the circuit, including environmental and endurance tests which can be completed in less than one week (see CECC 00114).

Group B inspection is divided into appropriate Sub-Groups.

Reduced inspection may be applied (see 3.4.4).

— Group C inspection

Group C prescribes the procedures to be used on a periodic basis to assess certain properties of the circuit including environmental and endurance tests which are appropriate for checking at intervals of three months, or longer if prescribed by the BDS.

Group C inspection is divided into appropriate Sub-Groups.

— Group D inspection

Group D prescribes the procedures to be used on a periodic basis at intervals of twelve months.

3.4.2 Quality inspection testing

Lot release shall be in accordance with CECC 00114.

The applicable tests are defined in 3.6 of this specification and as appropriate in the SS, FS, BDS relevant to the tested devices.

The inspection levels (IL) and acceptable quality levels (AQL) or alternatively the sample size (n) and acceptance criteria (c), given in the tables apply to the whole of each Sub-Group and not to any single test in the Sub-Group.

The tests sequence(s), given in the Sub-Groups, shall be followed.

Unless otherwise prescribed, specimens which fail Group A inspection shall be rejected and shall not be used as samples for Group B, C and D inspection.

Specimens required for Group B, C and D inspection, shall be components which have passed Group A or Group B inspection for those characteristics of tests specified as post-test limits.

3.4.3 Sampling procedures for small lots

To be included later.

3.4.4 Supplementary procedure for reduced inspection

A special reduced inspection procedure for the tests in all Sub-Groups of Group B inspection may be used, provided that the conditions given for the change from normal to reduced inspection in IEC 410 are met.

Those tests in Group B, which are already included as a periodic test in Group C, shall be under inspection. Where no relevant test exists in Group C, the test shall be performed under Group B test conditions as an additional test with a fixed sample size giving 95 % confidence of accepting product of the Group B AQL (with acceptance on one defect).

This special procedure applies independently to each Sub-Group. It allows a manufacturer to carry out the appropriate Group B test at normal inspection under Group C conditions at intervals of three months instead of on a lot-by-lot basis. Reversion to normal inspection for a Sub-Group in Group B shall be made when a Sub-Group has failed to meet Group C inspection.

3.4.5 Re-submission of rejected lots

Any lot rejected by Group A tests is returned to production for re-work or re-screening for the identified defect. No new parts are to be included in the lot.

The lot is then re-submitted and inspected under the conditions of tightened inspection. It shall retain the same lot number and details of the new submission shall be recorded. The same lot shall not be submitted more than three times.

For Group B tests the conditions for re-submission are under consideration.

3.4.6 Certified test records

The procedure given in CECC 00109 shall apply, and the certified test records shall conform to the information given in the SS.

3.4.7 Delayed delivery

Release lots which have been in store for more than the period stated below shall undergo Group A and Sub-Group B2 tests before delivery. No further re-testing is needed for deliveries within the applicable period.

The relevant period shall be:

- 1 year for devices assessed at Sub-Group B2 without ageing;
- or
- 2 years for devices assessed at Sub-Group B2 with ageing in accordance with 4.6.10.

At the manufacturer's convenience an additional marking can be used. This marking may be on the components and/or the packing before acceptance testing. If the components are marked the original marking shall be maintained.

3.4.8 Delivery of devices subjected to destructive or non-destructive tests

Devices subjected to tests indicated "destructive" (D) shall not be included in the lot for delivery.

Devices subjected to "non destructive" (ND) tests may be delivered provided they are retested to Group A requirements and satisfy them.

3.4.9 Supplementary procedure for deliveries

When permitted by the ONS, the manufacturer may, at his discretion, supply devices that have met a higher assessment level against orders for a lower assessment level.

3.4.10 Supplementary information

Any supplementary information given in the DS for application purposes shall not be the subject of inspection.

3.5 Capability approval

See Annex C and Annex D.

3.6 Inspection requirements

The following data shall be given for Group A, B, C and D inspection requirements through 2 quality assessment levels P and Y.

Key of abbreviations in the tables:

- D = Destructive test
- ND = Non-Destructive test
- IL = Inspection Level
- AQL = Acceptable Quality Level
- n = sample size
- c = acceptance criterion
- na = not applicable
- GS = Generic Specification
- SS = Sectional Specification
- BDS = Blank Detail Specification
- FS = Family Specification

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements									
GROUP A INSPECTION: The following electrical inspection requirements shall be given. Additional characteristics to be inspected may be given for the specific circuit(s) in accordance with the relevant Sectional Specification. The tests of Group A can be done totally or partly on the same sample, by applying the tightest IL and AQL. A circuit is considered defective with appearance of the first defect.				Assessment levels									
				P (Note 1)				Y (Note 2)					
				With correlation (Note 3)		Without correlation		With correlation (Note 3)		Without correlation			
				IL	AQL	IL	AQL	IL	AQL	IL	AQL		
<u>Sub-Group A0</u> Internal visual examination (before-encapsulation)	ND	Annex A (Condition B, unless otherwise specified)		S4	2,5	S4	2,5	na	na	na	na		
<u>Sub-Group A1</u> External visual examination 4.2.2	ND	4.2.2	External visual examination (visual) inoperatives (Note 4)	II	0,1	II	0,1	II	0,1	II	0,1		
<u>Sub-Group A2</u> Verification of the function at 25 °C (Note 5) See relevant SS, FS, BDS and DS	ND	Supply voltage(s) See relevant SS, FS, BDS and DS	See relevant SS, FS, BDS and DS	II	0,065	II	0,065	II	0,065	II	0,065		
<u>Sub-Group A3</u> Static characteristics at 25 °C See relevant SS, FS, BDS and DS	ND	See relevant SS, FS, BDS and DS											
<u>Sub-Group A4a</u> Static characteristics at maximum operating temperature Same characteristics as in Sub-Group A3	ND	T _{amb} = T _{amb} max. See relevant SS, FS, BDS and DS	See relevant DS Limits may be different from those in Sub-Group A3			S4	0,25			II	0,065	S4	0,25
<u>Sub-Group A7a</u> Verification of the function at maximum operating temperature	ND	T _{amb} = T _{amb} max. See relevant SS, FS, BDS and DS	See relevant DS Limits may be different from those in Sub-Group A2										
<u>Sub-Group A4b</u> Static characteristics at minimum operating temperature Same characteristics as in Sub-Group A3	ND	T _{amb} = T _{amb} max. See relevant SS, FS, BDS and DS	See relevant DS Limits may be different from those in Sub-Group A3			S4	0,25					S4	0,25
<u>Sub-Group A7b</u> Verification of the function at minimum operating temperature	ND	T _{amb} = T _{amb} min. See relevant SS, FS, BDS and DS	See relevant DS Limits may be different from those in Sub-Group A2										

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements							
				Assessment levels							
				P (Note 1)				Y (Note 2)			
				With correlation (Note 3)		Without correlation		With correlation (Note 3)		Without correlation	
				IL	AQL	IL	AQL	IL	AQL	IL	AQL
<u>Sub-Group A3a</u> Die attach See 4.5.11 (where appropriate, see option 2 of 2.4.5)	ND	See relevant FS, BDS or DS		II	1,0	II	1,0	na	na	na	na
<u>Sub-Group A5</u> Dynamic characteristics at 25 °C See relevant SS, FS, BDS and DS	ND	See relevant SS, FS, BDS and DS		II	0,25	II	0,25	II	0,25	II	0,25
<u>Sub-Group A6a</u> Dynamic characteristics at maximum operating temperature (Note 6)	ND	$T_{amb} = T_{amb \text{ max.}}$ See relevant SS, FS, BDS and DS	See relevant DS Limits may be different from those of Sub-Group A5			S4	0,65			S4	0,65
<u>Sub-Group A6b</u> Dynamic characteristics at minimum operating temperature (Note 6)	ND	$T_{amb} = T_{amb \text{ min.}}$ See relevant SS, FS, BDS and DS	See relevant DS Limits may be different from those of Sub-Group A5			S4	0,65			S4	0,65
<u>Sub-Group A8</u> Cavity packages only: Sealing	ND	4.6.9 1) or 4.6.9 3) and 4.6.9 2)		II	0,4	II	0,4	na	na	na	na

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements			
GROUP B INSPECTION				Assessment levels			
				P (Note 7)		Y (Note 7)	
				n	c	n	c
<u>Sub-Group B1</u> Dimensions	ND	See 4.3	See relevant DS	11	0	11	0
<u>Sub-Group B2</u> Solderability of terminations	D	4.6.10 1) or 4.6.10 2) Ageing required if specified by the DS		22	0	22	0
<u>Sub-Group B3</u> Cavity packages only: Sealing	ND	4.6.9 1) or 4.6.9 3) and 4.6.9 2)		na	na	45	0
<u>Sub-Group B4</u> Change of temperature (Note 8) Followed by: 1) Cavity packages: Sealing 2) Non cavity packages and cavity packages with organic sealing: Damp heat steady state highly accelerated test End point tests: (Note 10) Electrical tests: Sub-Groups A2 and A3	ND ND D	4.6.8 1) Test Na T _{stg} max. and min. but not exceeding – 65 °C and + 175 °C 10 cycles 4.6.9 1) or 4.6.9 3) and 4.6.8 2) 4.6.3 2), test conditions under consideration (Note 9) ● For level P: 4.6.3 2) variant C with t = 150 h As for Sub-Groups A2 and A3	 As for Sub-Groups A2 and A3	22	0	22	0
<u>Sub-Group B5</u> Electrical endurance 168 h (Note 11) See relevant SS, FS, BDS or DS End point tests: (Note 10) Electrical tests: Sub-Groups A2 and A3	ND	T _{amb} = T _{amb} max. See relevant SS, FS, BDS or DS As for Sub-Groups A2 and A3	 As for Sub-Groups A2 and A3	32	0	32	0
<u>Sub-Group B6</u> Dew point test (for cavity packages only) (under consideration) (Where appropriate, see 2.5.4 option 2)		(under consideration)	(under consideration)	18	1	na	na

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements			
GROUP C INSPECTION				Assessment levels			
				P (Note 7)		Y (Note 7)	
				n	c	n	c
<u>Sub-Group C1</u> Dimensions	ND	See 4.3	See relevant DS	11	0	11	0
<u>Sub-Group C2</u> Immersion in cleaning solvent End point test: Electrical tests (if applicable)	ND	See 4.4 See relevant DS	See relevant DS	11	0	11	0
<u>Sub-Group C3</u> Robustness of terminations	D	According to DS: 4.6.12 1) <u>and/or</u> 4.6.12 2) <u>and/or</u> 4.6.12 3) Number and position of terminations	No final measurements	11 (Note 7)	0	11 (Note 7)	0
<u>Sub-Group C4a</u> Cavity packages (Note 12) Resistance of components to soldering heat followed by: Change of temperature Followed by: Sealing End point tests: (Note 10) Electrical tests: Sub-Groups A2 and A3	D	4.6.11 4.6.8 3) Test Nc 10 cycles <u>or</u> 4.6.8 1) Test Na 100 cycles unless otherwise specified in FS or DS 4.6.9 1) or 4.6.9 3) <u>and</u> 4.6.9 2) As for Sub-Groups A2 and A3	As for Sub-Groups A2 and A3	22	0	22	0
<u>Sub-Group C4b</u> Non cavity packages and cavity packages with organic sealing (Note 12) Resistance of components to soldering heat followed by: Change of temperature Followed by: Damp heat steady state highly accelerated test End point tests: (Note 10) Electrical tests: Sub-Groups A2 and A3	D	4.6.11 4.6.8 1) Test Na 500 cycles T _{stg} max. et min. (but not exceeding – 65 °C and + 175 °C) 4.6.3 2), test condition under consideration (Note 9) ● For level P: 4.6.3 2) variant C with t = 150 h As for Sub-Groups A2 and A3	As for Sub-Groups A2 and A3	45 (Note 7)	0	45 (Note 7)	0

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements			
				Assessment levels			
				P		Y	
				n	c	n	c
<u>Sub-Group C5</u> Cavity packages only: Shock Followed by: Vibration (sinusoidal) Followed by: Acceleration, steady state End point tests: (Note 10) - Sealing - Electrical tests: Sub-Groups A2 and A3	D	4.6.4 Test Ea Condition 1, 2 or 3 4.6.5 4.6.7 4.6.9 1) or 4.6.9 3) and 4.6.9 2) As for Sub-Groups A2 and A3	As for Sub-Groups A2 and A3	11 (Note 7) (Note 13)	0	11 (Note 7) (Note 13)	0
<u>Sub-Group C6</u> Cavity packages only: Damp heat, steady state see 4.6.2 1) End point tests: (Note 10) - External visual examination (Sub-Group A1) - Electrical tests: Sub-Group A2 and A3	D	4.6.2 1) 56 days As for Sub-Groups A2 and A3	As for Sub-Groups A2 and A3	22 (Note 14)	0	22 (Note 14)	0
<u>Sub-Group C7</u> Non cavity packages and cavity packages with organic sealing Damp heat steady state End point tests: (Note 10) Electrical tests: Sub-Groups A2 and A3	D	4.6.3 1) with bias P: Severity 4 Y: Severity 1 As for Sub-Groups A2 and A3	As for Sub-Groups A2 and A3	32 (Note 7)	0	32 (Note 7)	0
<u>Sub-Group C8</u> Electrical endurance 2 000 h See relevant SS, FS, BDS and DS End point tests: (Note 10) Electrical tests: Sub-Groups A2 and A3	ND	$T_{amb} = T_{amb \text{ max.}}$ See relevant SS, FS, BDS et DS As for Sub-Groups A2 and A3	As for Sub-Groups A2 and A3	45 (Note 7)	0	45 (Note 7)	0
<u>Sub-Groups C9 and C10</u> : not applicable							

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements			
Tests of Sub-Groups C11 and C12 can be performed on the same sample. A circuit is considered defective with appearance of the first defect.				Assessment levels			
				P		Y	
				n	c	n	c
<u>Sub-Group C11a</u> Dynamic characteristics at maximum operating temperature	ND	$T_{amb} = T_{amb \text{ max.}}$ Electrical conditions as for Sub-Group A5	Limits may be different from those in Sub-Group A5	22 (Note 7) (Note 15)	0	22 (Note 7) (Note 15)	0
<u>Sub-Group C11b</u> Dynamic characteristics at minimum operating temperature	ND	$T_{amb} = T_{amb \text{ min.}}$ Electrical conditions as for Sub-Group A5	Limits may be different from those in Sub-Group A5	22 (Note 7) (Note 15)	0	22 (Note 7) (Note 15)	0
<u>Sub-Group C12a</u> Verification of the function (as for Sub-Group A7a) and static characteristics (as in Sub-Group A4a) at maximum operating temperature	ND	$T_{amb} = T_{amb \text{ max.}}$ Electrical conditions as for Sub-Groups A4a and A7a	As for Sub-Groups A4a and A7a	22 (Note 7) (Note 16)	0	22 (Note 7) (Note 16)	0
<u>Sub-Group C12b</u> Verification of the function (as for Sub-Group A7b) and static characteristics (as in Sub-Group A4b) at minimum operating temperature	ND	$T_{amb} = T_{amb \text{ min.}}$ Electrical conditions as for Sub-Groups A4b and A7b	As for Sub-Groups A4b and A7b	22 (Note 7) (Note 16)	0	22 (Note 7) (Note 16)	0
<u>Sub-Group C13</u> Salt mist 4.6.14 (where appropriate)	D	4.6.14		11	0	11	0
<u>Sub-Group C14</u> Additional electrical characteristics	ND	See relevant SS, FS, BDS et DS		22 (Note 7)	0	22 (Note 7)	0

Examination or test	D ND	Conditions of test	Limits to be specified	Inspection requirements			
GROUP D INSPECTION				Assessment levels			
				P		Y	
				n	c	n	c
<u>Sub-Group D1</u> Electrical endurance 8 000 h See relevant SS, FS, BDS or DS End point tests: Electrical tests: Sub-Groups A2, A3 and A5	D	$T_{amb} = T_{amb \text{ max.}}$ see relevant SS, FS, BDS or DS As for Sub-Groups A2, A3 and A5	As for Sub-Groups A2, A3 and A5	20	—	20 (Note 14)	—
<u>Sub-Group D2</u> Transient energy test End point tests: Sub-Groups A2, A3 and A5	D	4.5.9 Sub-Groups A2, A3 and A5	See relevant SS, FS, BDS and DS Sub-Groups A2, A3 and A5	11 (Note 7)	0	11 (Note 7)	0
<u>Sub-Group D3</u> Thermal overstress (under consideration) (where appropriate see 2.5.4 option 2)	D	(under consideration)	(under consideration)				
<u>Sub-Group D4</u> Latch-up (under consideration) (where appropriate see 2.5.4 option 2)	D	(under consideration)	(under consideration)				
<u>Sub-Group D5</u> Input capacitance (C_{in}) (where appropriate)	ND	See relevant FS, BDS and DS	See relevant FS, BDS and DS	8	1	8	1
<u>Sub-Group D6</u> Output capacitance (C_{out}) (where appropriate)	ND	See relevant FS, BDS and DS	See relevant FS, BDS and DS	8	1	8	1

NOTE 1 One inspection lot: max. 1 week and max. 35 000 devices.

NOTE 2 One inspection lot: max. 1 month or 4 consecutive weeks.

NOTE 3 Correlated measurements are allowed: see 4.5.10.

NOTE 4 Only the following defects are defined as (visual) inoperatives:

- type identification marking, missing or wrong
- wrong reference for terminal identification
- pins missing and/or broken
- package damaged or incomplete such that chip or bond wires are exposed.

NOTE 5 Verification of the function may be implicitly contained in tests performed in Sub-Groups A3 to A7b.

NOTE 6 With correlation: same characteristics as in Sub-Group A5.

Without correlation: same characteristics as in Sub-Group A5, except where measurability problems justify the shift of a characteristic to Sub-Group C14. This shall be specified in the DS.

NOTE 7 Sampling size can be increased according to LTPD tables with a maximum acceptance number $c = 1$. However the application of this clause to all Sub-Groups for which it is applicable shall not result in a total combined of defectives exceeding 2 for cavity packages and 4 for non cavity packages.

NOTE 8 Components subjected to test B4 shall have satisfied the requirements of 4.6.9 1) or 4.6.9 3) and 4.6.9 2) (applicable to cavity devices with non-organic sealing only).

NOTE 9 Damp heat cyclic test — IEC 68-2-30, Test Db, 55 °C, 6 cycles, variant 2 — shall be used until the damp heat steady state highly accelerated test is published.

NOTE 10 End point tests for level P: electrical tests are A2, A3 and A5

NOTE 11 This test is not applicable for the device with a screening class including a burn-in test of 168 h minimum duration, with an applicable PDA of 5 % maximum and if the temperature and operating conditions for burn-in are the same or more severe than the conditions for endurance testing. Where they are applied, accelerated test conditions shall be the same for burn-in and endurance testing.

NOTE 12 Components subjected to test C4 shall have satisfied the requirements of 4.6.9 1) or 4.6.9 3) and 4.6.9 2) (applicable to cavity devices with non-organic sealing only).

NOTE 13 After three successful consecutive tests the periodicity may be reduced to once per year.

NOTE 14 Applicable if specified in the DS.

NOTE 15 The tests of Sub-Group A6 that are performed with correlated test procedures.

NOTE 16 The tests of Sub-Groups A4 and A7 that are performed with correlated test procedures.

3.7 Statistical process control (SPC)

See Annex F.

4 Test and measurement procedures

4.1 Standard conditions for testing

All tests shall be performed under the conditions given below as required by the test procedure.

4.1.1 *Standard atmospheric conditions for reference*

Temperature	: 25 °C
Relative humidity	: 50 %
Air pressure	: 1 013 hPa

NOTE Air pressure is in accordance with IEC 68-1. Temperature and relative humidity are in accordance with IEC 749.

4.1.2 *Standard atmospheric conditions for referee tests (see clause 5.2 of IEC 68-1)*

Temperature	: (25 ± 1) °C
Relative humidity	: between 48 % and 52 %
Air pressure	: between 860 hPa and 1 060 hPa

NOTE The relative humidity may be disregarded where it has no influence on the test results.

4.1.3 *Standard atmospheric conditions for testing (see clause 5.3 of IEC 68-1)*

Temperature	: between 15 °C and 35 °C
Relative humidity	: between 45 % and 75 %
Air pressure	: between 860 hPa and 1 060 hPa

4.1.4 *Standard atmospheric conditions for electrical measurements*

Temperature	: (25 ± 5) °C
Relative humidity	: between 45 % and 75 %
Air pressure	: between 860 hPa and 1 060 hPa

NOTE These conditions are in accordance with clause 5.3 of IEC 68-1, except for the temperature (see IEC 749).

4.1.5 Standard recovery conditions

Temperature	: actual laboratory temperature within the temperature range between + 15 °C and + 35 °C
Relative humidity	: between 45 % and 75 %
Air pressure	: between 860 hPa and 1 060 hPa
Recovery period	: until reference point temperature equilibrium is reached.

NOTE These conditions are in accordance with clause 5.4 of IEC 68-1, except for humidity.

4.2 Visual examination

4.2.1 Internal visual examination (pre-cap inspection)

When prescribed by the relevant specification, the internal visual examination shall be performed following the method described in Annex A of this specification.

For screening purposes, the test conditions A, in A.3.1, applies to Class H devices and the test condition B, in A.3.2, applies to Classes B and C devices. (Classes of microcircuits refer to screening requirements of 4.10).

For other purposes, the relevant DS shall prescribe requirements as in A.4.

An alternative screening method as defined in A.3.4 of Annex A may be used on an optional basis on any microcircuits, where Condition B of “Internal Visual Examination” is specified as applicable for the relevant screening classes.

This alternate method may be used if the conditions and limits of the special electrical tests and other own applicable manufacturer's tests are submitted to, and approved by the ONS, and if at least one of the following criteria is met:

- 1) Minimum horizontal geometry is less than 5 μm .
- 2) Two or more levels of metallization.
- 3) Opaque materials mask design features.

4.2.2 External visual examination

Unless otherwise specified, visual examination shall be performed under approved factory lighting conditions under normal visual conditions.

Inspection shall include the following items:

- correctness of marking and legibility (excluding possible confusion between figures and/or letters)
- correctness of terminal identification
- correctness of appearance (for example: no broken encapsulation or terminals, no cracks in encapsulation, no open encapsulation).

4.3 Dimensions

Dimensions shall be checked in accordance with the reference drawings or as prescribed in the DS. The dimensions which shall be checked as part of the Group B and Group C are indicated in Table 1, using the reference letters of IEC 191-3.

FORM OF DEVICE (Note 1)	SUB-GROUP B1	SUB-GROUP C1
Form 1	A max. A ₁ min. ϕ b ₂ min. and max. e (note 2) L min. Z max. Z ₁ max.	Other dimensions not included in B1
Form 2	A max. A ₁ min. b min. and max. c min. and max. e (note 2) L min. Z max.	
Form 3	A max. ϕ a (note 2) ϕ b ₂ min. and max. ϕ D max. L min. α and β (note 2)	
Form 4	A max. b min. and max. e (note 2) H min. and max. L min. Z max.	
NOTE 1 See IEC 191-3 NOTE 2 Positional tolerances of terminals		

4.4 Immersion in cleaning solvents

This test shall be in accordance with Test XA of IEC 68-2-45 (1980) with the following requirements:

The sample shall be divided in two equal parts:

- The first part shall be submitted to test with solvent defined by sub-clause 3.1.1 of IEC 68-2-45 at the temperature of $(23 \pm 5) ^\circ\text{C}$.
- The second part shall be submitted to test with solvent defined by sub-clause 3.1.2 of IEC 68-2-45 at the temperature of $(55 \pm 5) ^\circ\text{C}$.

Initial measurements:

- External visual examination : voir 4.2.2
- Electrical measurements : optional

Conditioning: Method 2 (without rubbing)

Recovery time: not less than 1 h and not more than 2 h, unless otherwise specified.

Final measurements:

- External visual examination: see 4.2.2
- Electrical measurements: optional

The values of the following test conditions shall be prescribed in the DS:

- Initial electrical measurements (if applicable)
- Recovery time (if different from 1 h to 2 h)
- Final electrical measurements (if applicable)

4.5 Electrical measurement procedure

4.5.1 Ratings

The test conditions for all measurements shall be such that the maximum ratings of the device are not exceeded (see IEC 134).

4.5.2 Equilibrium conditions

All electrical tests shall be conducted under equilibrium conditions unless otherwise specified, or unless the measurement is being carried out under pulsed conditions. When test conditions cause significant change with time of the characteristics being measured, means of compensation for such effects shall be specified; for example, the length of time that the device shall be maintained at test conditions before making a measurement.

4.5.3 Temperature

The ambient temperature shall be measured as the air temperature adjoining the integrated circuit in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

4.5.4 Precautions

The precautions shall include limits on maximum instantaneous currents and applied voltages. It is recommended that devices shall not be inserted into, or removed from, a test circuit while the latter is energized.

For electrostatic sensitive devices (for example MOS devices), adequate precautions shall be taken to prevent damage from static charge both before and after test.

4.5.5 Measurement circuit requirements

Unless otherwise prescribed in the DS the following tolerances shall apply:

- resistance $\pm 1\%$
- capacitors $\pm 5\%$
- power supplies $\pm 1\%$
- voltage and current instruments $\pm 1\%$
- pulse time measuring equipments $\pm 5\%$ but not less than $\pm 0,5$ ns.
- Constant current source

A current shall be considered constant if a two-to-one increase of the effective load impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.

- Current measuring device

The effective admittance of a current measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of the measurement

- Constant voltage source

A voltage shall be considered constant if a two-to-one decrease of the effective load impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement

- Voltage measuring device

The effective impedance of a voltage measuring device shall be sufficiently high so that halving its value does not significantly affect the measurement

- Load impedance

The load impedance represents the equivalent input impedance of the test circuit and the device under test. For acceptance test purposes, the input impedance may be replaced by a resistor representing worst-case conditions

- Power supplies

The sources of direct currents and voltages shall not have a ripple content large enough to affect the desired accuracy of measurement. Test or supply voltages or current shall be within $\pm 1\%$ of the specified value.

— Precision of measurements

The limits specified in the DS are absolute. Measurement inaccuracies shall be taken into account when determining the actual measurement limits.

4.5.6 Multiple integrated circuits

Each functionally independent section of a multiple integrated circuit shall be tested individually and all terminals associated solely with sections not under test shall be left open circuit, or as specified. Multiple integrated circuits shall be checked to ensure that interaction is not present between functionally independent sections.

Each of a group of functionally equivalent signal terminals shall be tested individually, with connections applied to the remainder as specified in the DS.

4.5.7 Unspecified connections to terminals

Any terminal for which no conditions are specified, shall be left open-circuited.

4.5.8 Electrical measuring methods

Measurements may be carried out by using the methods as prescribed in the SS or any other method giving compatible results, but in case of conflict, the specified method shall be used.

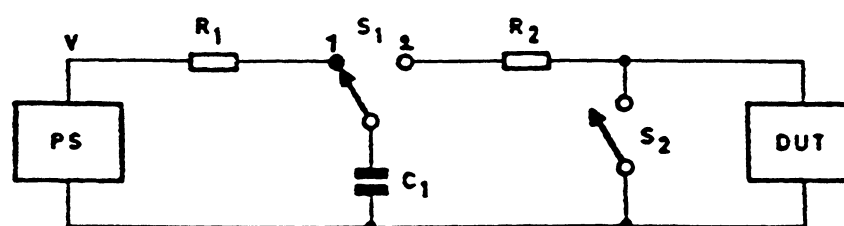
NOTE By "compatible" it is meant that the value of the characteristic established by such other method will fall within the specified limits when measured by the specified method (see also CECC 00111).

4.5.9 Transient energy test

Purpose:

To prove the capability of an integrated circuit to withstand a specified level of electrostatic discharge.

Test circuit:



PS DC power supply

V 500 V

C₁ 100 pF

DUT Device under test

R₁ Protection resistor

R₂ 1,5 kΩ

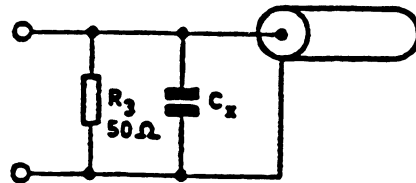
The insulation resistance of the capacitor C₁ shall be greater than 1 GΩ. S₁ is a break-before-make bounceless switch (for example a mercury-wetted relay). The stray capacitance (excluding the device under test) should not exceed 5 % of the value of C₁. Switch S₂ prevents the build-up of charge in the stray capacitance and shall be closed during the insertion and removal of the device under test.

Description:

With S₁ in position 1, the capacitor C₁ is charged to the voltage V, the source of which may be either polarity, via the protection resistor R₁. This resistor has the double function to protect the power supply and the operator in case of malfunction. Its resistance shall be 1 MΩ to 10 MΩ. With S₂ open and S₁ in position 2, capacitor C₁ is discharge into the device under test via the resistor R₂.

The test is regarded as destructive.

The performance of the test apparatus shall be verified by the following procedure. With no device in the test socket and S_2 closed, the waveform across R_2 shall have a rise time (10 % to 90 %) of (13 ± 2) ns. The decay time from the peak value to 36,8 % of this value shall be $150 \text{ ns} \pm 10 \%$. The peak value of this voltage shall be within $\pm 5 \%$ of the specified value.



C_x : Stray capacitance including cable and input of oscilloscope. 100 MHz bandwidth is minimum.

Test procedure:

With all other terminals open-circuited, each specified pair of terminals is subjected to a minimum 5 cycles with one polarity of the voltage V , with a time interval between each discharge of between 100 and 5 000 ms. Each single terminal including supply terminal(s) shall be tested with respect to the reference terminal(s) then with respect to each supply terminal of the device.

The test is repeated with the other polarity of voltage V .

Precaution:

The device should be handled as an electrostatic sensitive device (see Publication IEC 747-1, Chapter IX, Clause 3).

Specified conditions:

- Test voltage, if other than 500 V.
- Post-test measurements.

The conditions should be prescribed as far as possible in order to achieve comparable test results.

4.5.10 Correlated measurements

1) Procedure for correlated measurements

If it can be demonstrated that the results of an electrical or functional parameter tested under two different conditions are correlated, it is allowed to perform the test of the relevant characteristic under one condition only.

This test condition may not necessarily be the specified one.

Example: Measurements at 25 °C, correlated with those at 125 °C:

- The applicable correlation is determined as shown in 4.5.10 2) a) or b);
- The defined correlations shall be checked as shown in 4.5.10 3).

2) Methods for correlation measurement

Two methods are allowed to determine correlation:

- Statistical correlation
- Empirical method

The method is selected by the manufacturer.

The applied correlated limits for each relevant characteristics are declared to the ONS.

a) Statistical correlation

This method is based on the calculation of the correlation coefficient r which shall be higher than 0,85.

This coefficient r is defined by the formula:

$$r = \frac{\sum_{i=1}^n x_i \cdot y_i}{\sqrt{\sum_{i=1}^n x_i^2 \cdot \sum_{i=1}^n y_i^2}}$$

where:

$$x_i = X_i - X$$

$$y_i = Y_i - Y$$

X_i and Y_i are the results of tests under the two relevant conditions.

X and Y are the arithmetic means of the n values of X_i and Y_i respectively.

n is the sample size.

The sample size is at least 100 pieces for each product type from three different production lots (33 pieces minimum per production lot).

The formula applied to the readouts of the relevant electrical characteristics to be correlated.

b) Empirical Method

Based on:

- a thorough knowledge of the technology,
- a good understanding of the influence of the relevant test conditions on the product performances,

the formula applies to determine correlated limits.

3) Verification of correlated test limits

The verification is performed with a sample which is first tested according to correlated test conditions and test limits, and then to the specified test conditions and limits.

The number of devices tested shall be as large as necessary to obtain, at least, the specified sample size n which is accepted at the first test.

The correlation is not valid if the number of devices accepted in the first test and not accepted in the second test is more than the relevant acceptance criteria c .

This verification takes place:

- during the qualification of a type (structural similarity rules do not apply): $n = 76$; $c = 0$
- during periodic testing (structural similarity rules apply) according to the relevant quality assessment procedures.

4.5.11 Die attach (ND)

Purpose:

To determine the integrity of die attachment using a thermal transient measurement, which is an essential requirement for integrated circuits to be used in long term applications.

Description:

With all substrate diodes [input(s), power supply terminal(s)] connected in parallel, a current pulse is applied to the device under test, resulting in a nearly homogeneous heating of the die. The variation on the effective substrate diode forward voltage is measured.

Procedure:

The ambient temperature conditions shall be set to the specified value. The current I_p is set to the specified value. The value of the power burst should be greater than 5 % of the rated package dissipation. The measuring current I_m is set to 1 mA.

The integrated circuit shall be inserted into the test socket in accordance with its marking and terminal identification.

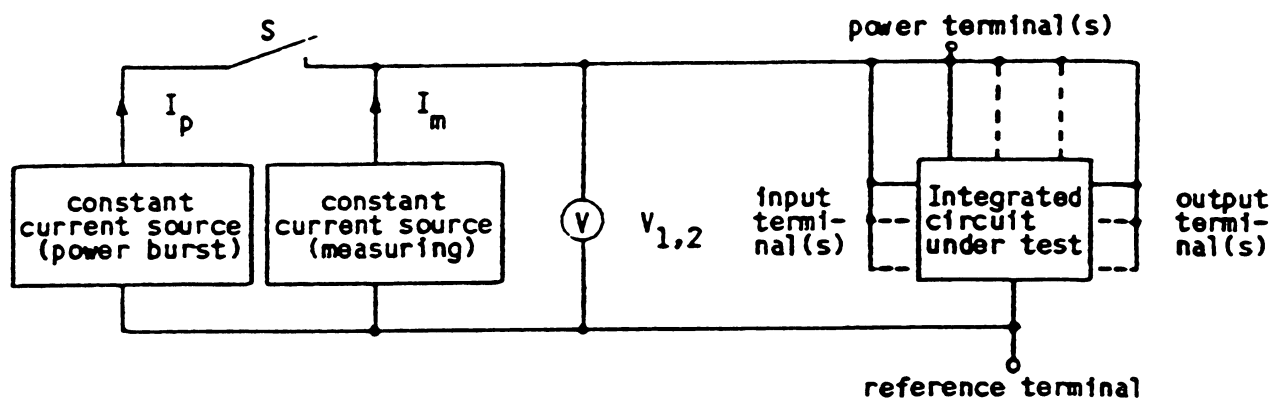
With switch S open the measuring current source is switched on, and the voltage V_1 across the substrate diode is measured.

The power burst is applied by closing the switch S for 100 ms.

Within 1 ms after removal of the power burst the voltage V_2 across the substrate diode is measured.

The variation of the diode forward voltage is calculated from $V_1 - V_2$

The measurement current source is switched off and the integrated circuit is removed from the test socket.

Circuit:**Specified conditions:**

The values of the following test conditions shall be prescribed in the DS:

- Ambient temperature for the test,
- Power burst current I_p ,
- Limits of the diode forward voltage variation $V_1 - V_2$.

4.5.12 Latch-up

1) Terms, definitions and letter symbols

A – Latch-up state

A reversible state in which a low-impedance path has resulted from and persists following the current resulting from an input, output or supply overvoltage that triggers a parasitic four-layer bipolar structure.

NOTE In the latch-up state, the device becomes fully or partially inoperable.

B – Latch-up

A process that results in a latch-up state.

C – Latch-up state voltage ($V_{CC(L)}$, $V_{DD(L)}$)

The voltage between the supply voltage terminals of an integrated circuit at a specified supply current when the integrated circuit is in the latch-up state.

D – Latch-up current (I_{latch})

The lowest current of a specified duration flowing either in or out of a specified terminal of an integrated circuit that causes latch-up to occur.

E – Latch-up voltage (V_{latch})

The lowest voltage of a specified duration applied to a specified terminal of an integrated circuit that causes latch-up to occur.

F – Latch-up supply voltage ($V_{CClatch}$, $V_{DDlatch}$)

The lowest voltage of a specified duration applied to a specified supply voltage terminal of an integrated circuit that causes latch-up to occur.

G – Latch-up supply current ($I_{CClatch}$, $I_{DDlatch}$)

The lowest current of a specified duration flowing either into or out of a specified supply terminal of an integrated circuit that causes latch-up to occur.

H – Latch-up state current ($I_{CC(L)}$, $I_{DD(L)}$) (at a supply terminal)

The current flowing either in or out of specified supply terminal of an integrated circuit when the integrated circuit is in the latch-up state.

I – Latch-up state holding current ($I_{CC(L)min}$, $I_{DD(L)min}$)

The minimum latch-up state current necessary to hold an integrated circuit in the latch-up state.

2) Latch-up characteristics

A – Latch-up current

Maximum value, under specified conditions of ambient or case temperature, supply voltage and application of triggering function.

B – Latch-up voltage

Minimum value, under specified conditions of ambient or case temperature, supply voltage and application of triggering function.

C – Latch-up supply voltage

Minimum value, under specified conditions of ambient or case temperature and supply voltage.

D – Latch-up supply current

Minimum value, under specified conditions of ambient or case temperature and supply voltage.

E – Latch-up state voltage

Minimum value, under specified conditions of ambient or case temperature, supply voltage and supply current.

F – Latch-up state current

Maximum and minimum values, under specified conditions of ambient or case temperature and supply voltage.

G – Latch-up state holding current

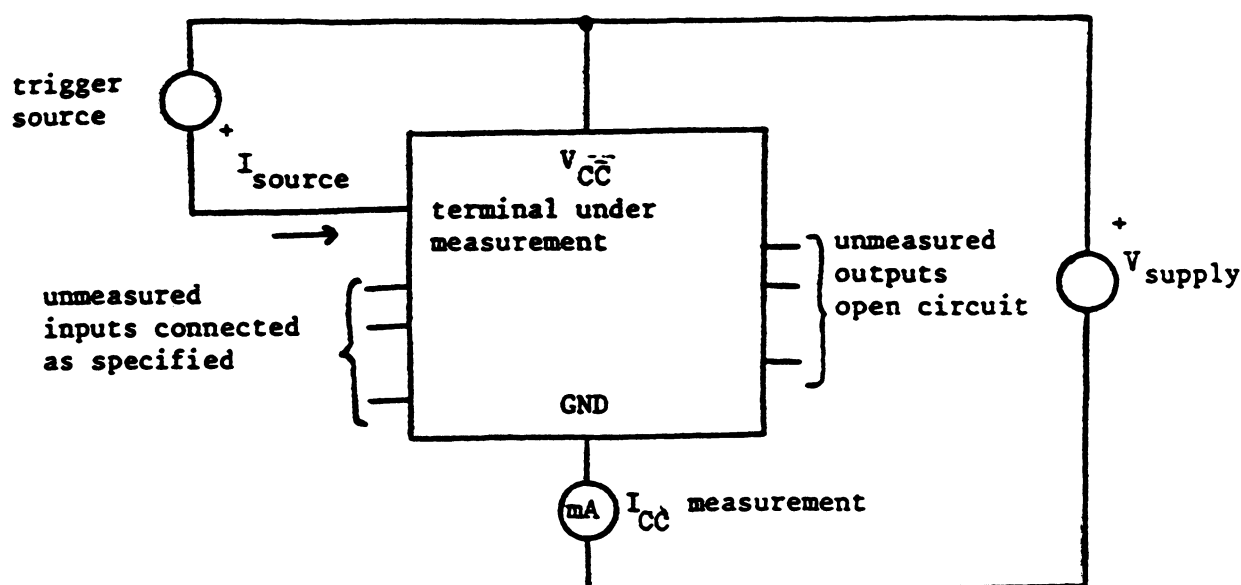
Maximum and minimum values, under specified conditions of ambient or case temperature and supply voltage.

3) Measuring methods

A – Positive latch-up input or output voltage or current

a) Purpose

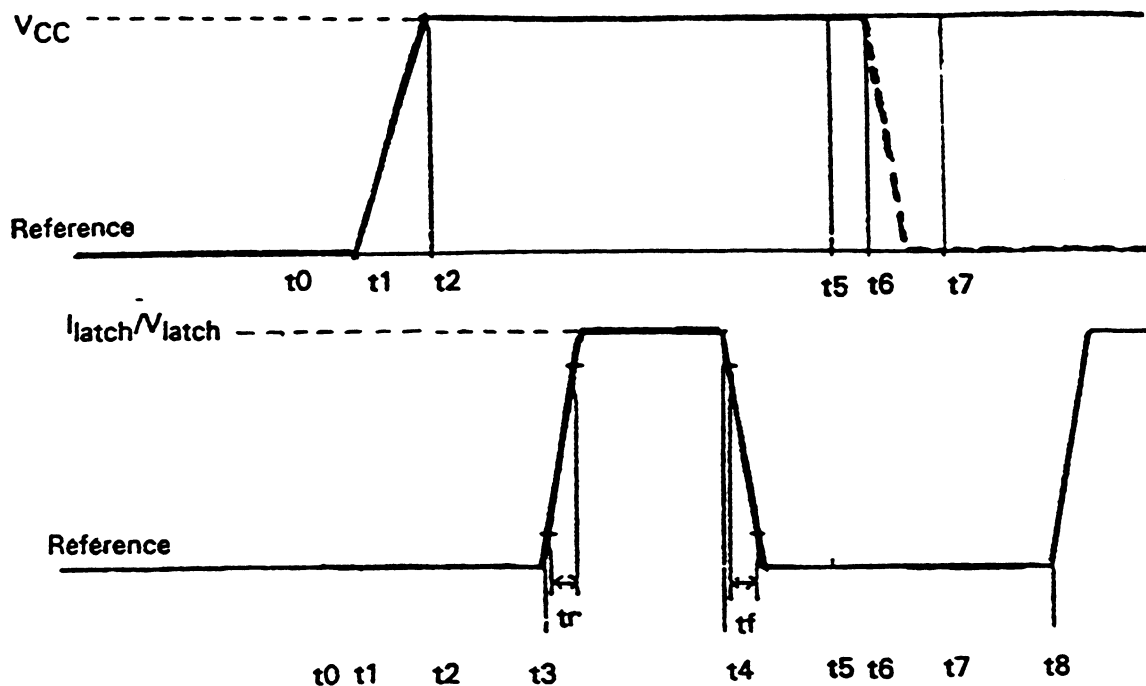
To measure the magnitude of the positive input or output voltage or current necessary to turn an integrated circuit into latch-up state.

b) Circuit diagramc) Circuit description and requirements

With specified supply voltage applied to the device under test, the triggering pulse is applied to the specified terminal. The pulse amplitude of the triggering current or voltage is increased until increase in supply current indicates latch-up in the device or until the specified maximum amplitude of the triggering pulse is reached. The supply voltage is switched off. A reading is taken of the amplitude of the triggering pulse, the positive latch-up voltage or current. All readings are taken by means of oscilloscope or other appropriate test equipment. The current limitation of the power supply shall be set low enough not to destroy the device. A pattern generator may be used to set the logic states of unmeasured input and output terminals. The test is considered as destructive.

d) Measurement procedure

- Adjust ambient temperature as specified.
- Apply power supply.
- Set I/O conditions, logic state, etc. as specified.
- Apply triggering current or voltage under specified pulse conditions of duration, rise and fall time to the specified terminal.
- Measure supply current after specified delay time
- Increase the amplitude of the triggering pulse until latch-up occurs or until the amplitude exceeds the specified value.
- Register the amplitude and repetition rate of triggering pulse.
- If an increase in supply current occurs or if supply current is greater than the specified maximum supply current, latch-up has occurred.
- Disconnect power source and I/O conditions.

e) Time operation

t_1 Connect device as specified.

t_2 Set supply current limitation and supply voltage as specified. Set input and output conditions as specified, to place the device in specified logic state if appropriate.

t_3 Apply single triggering pulse.

t_4 After the specified duration, remove the triggering pulse. Return the terminal under test to the same state as before the application of the trigger pulse.

t_5 After a specified delay time the supply current is measured.

t_6 If the supply current is greater than the specified maximum supply current, the device may have latched-up. Disconnect the supply voltage.

t_7 If the supply current is less than the specified maximum supply current, the device is not in latch-up.

t_8 After a cool down time (t_6 through t_7) a second trigger pulse can be applied, repeating the operations specified at times t_3 through t_6 , then continuing with the measurements as above.

f) Specified conditions

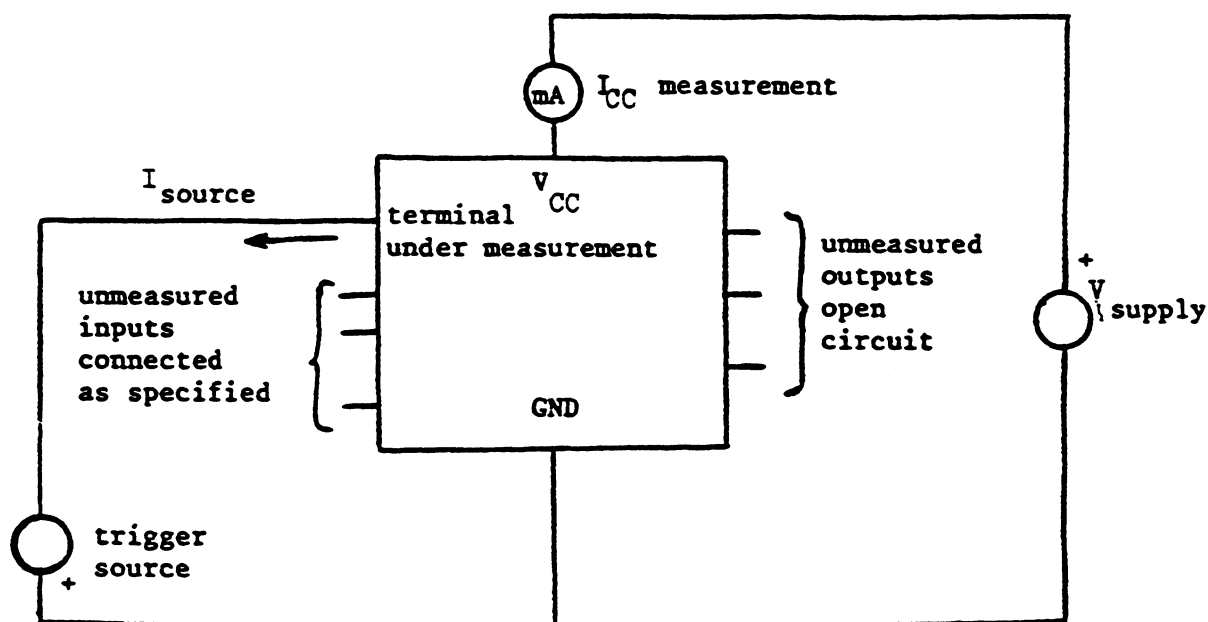
- Ambient or case temperature.
- Supply voltage.
- Terminals to be tested.
- Conditions at untested terminals: Unmeasured inputs connected to ground or V_{CC} (V_{DD}), unless otherwise specified. Unmeasured outputs are left open.
- Logic state.
- Maximum supply current.
- Conditions of triggering pulse:
 - Maximum amplitude
 - Duration
 - Rise and fall time.
- Delay time before measurement of supply current.
- Cool down time.
- Limitation of supply current.

B – Negative latch-up input or output voltage or current

a) Purpose

To measure the magnitude of the negative input or output voltage or current necessary to turn an integrated circuit into latch-up state.

b) Circuit diagram



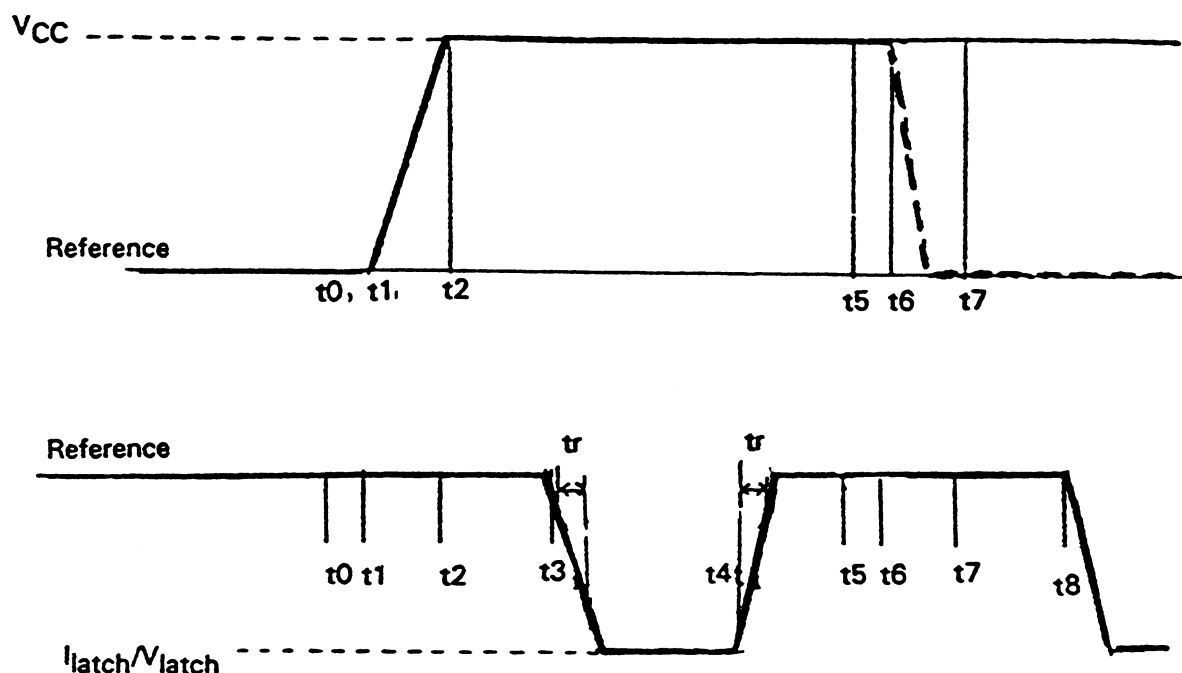
c) Circuit description and requirements

With specified supply voltage applied to the device under test, the negative triggering pulse is applied to the specified terminal. The pulse amplitude of the triggering current or voltage is increased until an increase in supply current indicates latch-up in the device. The supply voltage is switched off. A reading is taken of the amplitude of the triggering pulse, the negative latch-up voltage or current. All readings are taken by means of oscilloscope or other appropriate test equipment.

The current limitation of the power supply shall be set low enough not to destroy the device. A pattern generator may be used to set the logic states of unmeasured input and output terminals. The test is considered as destructive.

d) Measurement procedure

- Adjust ambient temperature as specified.
- Apply power supply.
- Set I/O conditions, logic state, etc. as specified.
- Apply triggering current or voltage under specified pulse conditions of duration, rise and fall time to the specified terminal.
- Measure supply current after specified delay time.
- Increase the amplitude of the triggering pulse until latch-up occurs, or until the amplitude exceeds the specified value.
- Register the amplitude and repetition rate of triggering pulse.
- If an increase in supply current occurs or if supply current is greater than the specified maximum supply current, latch-up occurs.
- Disconnect power source.

e) Time operation

t1 Connect device as specified

t2 Set supply current limitation and supply voltage as specified. Set input and output conditions as specified, to place the device in specified logic state if appropriate.

t3 Apply single pulse triggering.

t4 After the specified duration, remove the triggering. Return the terminal under test to the same state as before the application of the trigger pulse.

t5 After a specified delay time the supply current is measured.

t6 If the supply current is greater than the specified maximum supply current, the device may have latched-up. Disconnect the supply voltage.

t7 If the supply current is less than the specified maximum supply current, the device is not in latch-up.

t8 After a cool down time (t6 through t7) a second trigger pulse can be applied, repeating the operations specified at times t3 through t6, then continuing with the measurements as above.

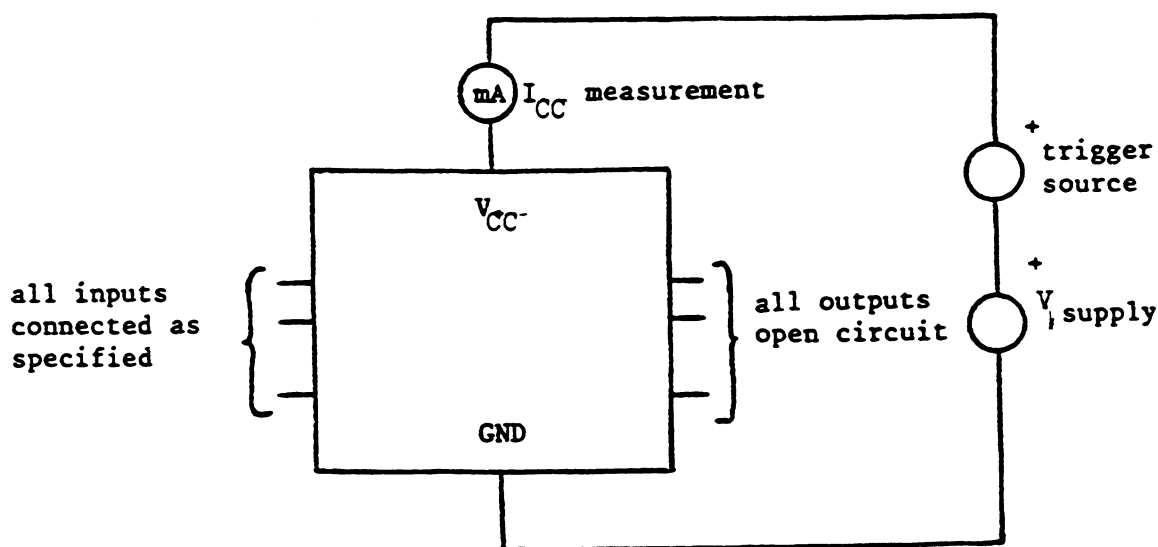
f) Specified conditions

- Ambient or case temperature.
- Supply voltage.
- Terminals to be tested.
- Conditions at untested terminals: Unmeasured inputs connected to ground or V_{CC} (V_{DD}), unless otherwise specified. Unmeasured outputs are left open.
- Logic state.
- Maximum supply current.
- Conditions of triggering pulse:
 - Maximum amplitude
 - Duration
 - Rise and fall time
- Delay time before measurement of supply current.
- Cool down time.
- Limitation of supply current.

C – Latch-up supply voltage or current

a) Purpose

To measure the magnitude of the voltage or current applied to the supply terminals necessary to turn an integrated circuit into latch-up state.

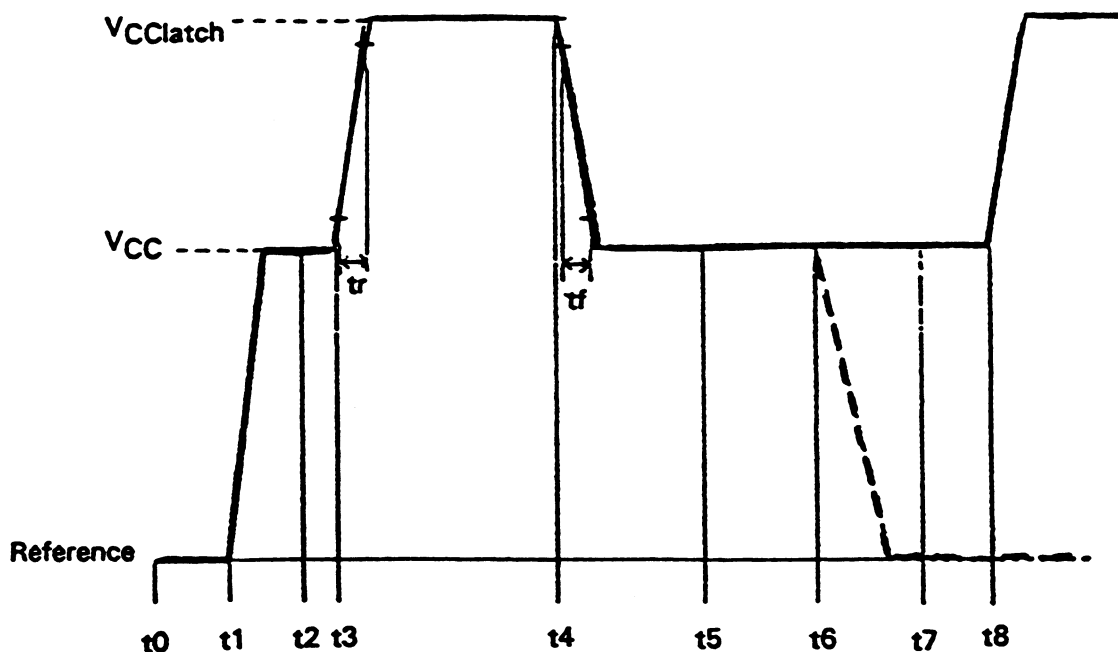
b) Circuit diagramc) Circuit description and requirements

With specified supply voltage applied to the device under test, a voltage or current is superimposed on the supply voltage or current. The pulse amplitude is increased until an increase in supply current indicates latch-up in the device or until the amplitude exceeds the specified value.

A reading is taken of the amplitude of the total supply voltage applied to the device, which is the latch-up supply voltage. The latch-up supply current is not directly measurable, but may be estimated by observing the current prior to latch-up together with the increments by which the current is increased. The supply voltage is switched off. All readings are taken by means of oscilloscope or other appropriate test equipment. The current limitation of the power supply shall be set low enough not to destroy the device. A pattern generator may be used to set the logic states of unmeasured input and output terminals. The test is considered as destructive.

d) Measurement procedure

- Adjust ambient temperature as specified.
- Apply power supply.
- Set I/O conditions, logic state, etc. as specified.
- Apply triggering voltage or current pulse under specified pulse conditions of duration, rise and fall time to the specified terminal.
- Measure supply current after specified delay time.
- Increase the amplitude of the triggering pulse until latch-up occurs, or until the amplitude exceeds the specified value.
- Register the amplitude and repetition rate of triggering pulse.
- If an increase in supply current occurs or if supply current is greater than the specified maximum supply current, latch-up occurs.
- Disconnect power source.

e) Time operation

t_1 Connect device as specified.

t_2 Set supply current limitation and supply voltage as specified. Set input and output conditions as specified, to place the device in specified logic state if appropriate.

t_3 The triggering voltage or current is superimposed on the supply voltage or supply current. Observe and record the total amplitude of the supply voltage or current, which is the latch-up supply voltage or current in case of latch-up.

t_4 After the specified duration, remove the triggering voltage. Return the terminal under test to the same state as before the application of the trigger pulse.

t_5 After a specified delay time the supply current is measured.

t_6 If the supply current is greater than the specified maximum supply current, the device may have latched-up. Disconnect the supply voltage.

t_7 If the supply current is less than the specified maximum supply current in the latch-up state, the device is not in latch-up.

t_8 After a cool down time (t_6 through t_7) a second trigger pulse can be applied, repeating the operations specified at times t_3 through t_6 , then continuing with the measurements as above.

f) Specified conditions

- Ambient or case temperature.
- Supply voltage.
- Terminals to be tested.
- Conditions at untested terminals: all inputs connected to ground or V_{CC} (V_{DD}), unless otherwise specified. All outputs are left open.
- Logic state.
- Maximum supply current.
- Conditions of the triggering pulse:
 - Maximum amplitude
 - Duration
 - Rise and fall time
- Delay time before measurement of supply current.

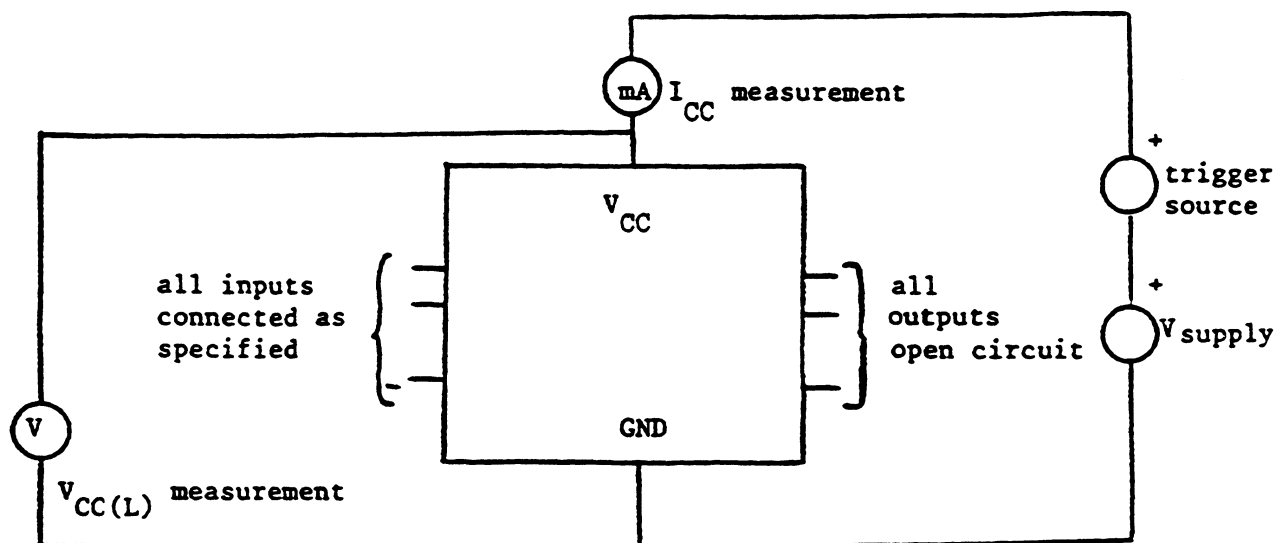
- Cool down time.
- Limitation of supply current.

D – Latch-up state voltage or current

a) Purpose

To measure the magnitude of the voltage across the supply voltage terminals or the supply current of an integrated circuit in the latch-up state.

b) Circuit diagram



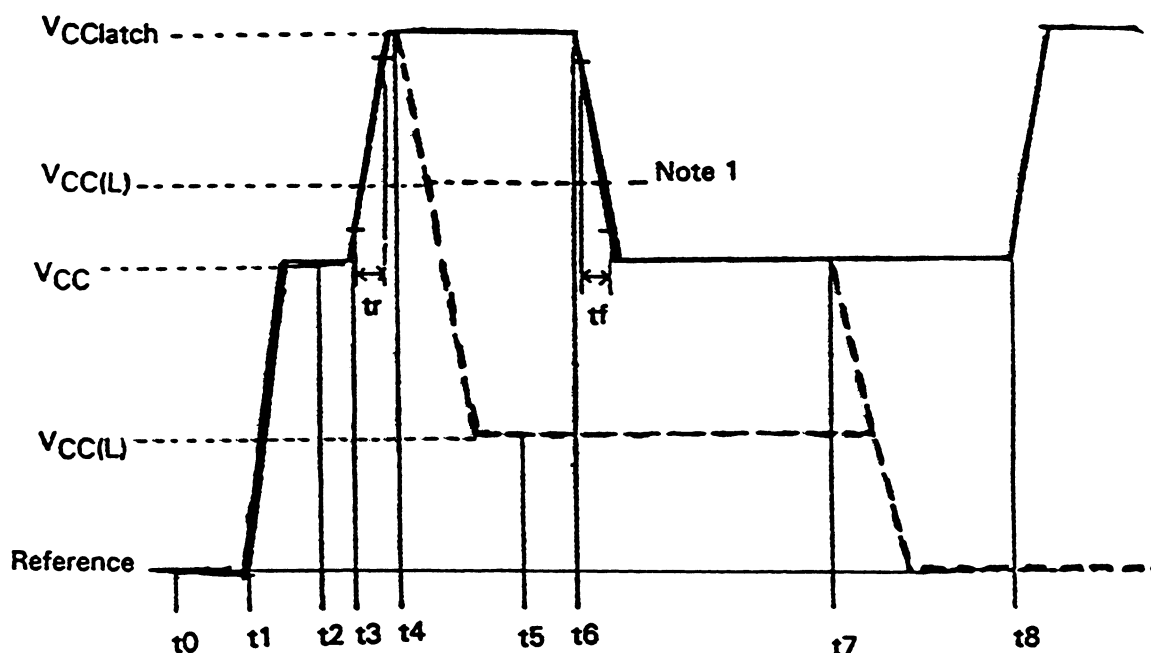
c) Circuit description and requirements

With specified supply voltage applied to the device under test, the triggering pulse is applied to the specified terminal. The pulse amplitude of the triggering pulse is increased until an increase in supply current indicates latch-up in the device, or until the amplitude exceeds the specified value.

A reading is taken of voltage across the device supply terminals, the latch-up state voltage, or of the supply current in the latch-up state. The supply voltage is switched off. All readings are taken by means of oscilloscope or other appropriate test equipment. The current limitation of the power supply shall be set low enough not to destroy the device. A pattern generator may be used to set the logic states of unmeasured input and output terminals. The test is considered as destructive.

d) Measurement procedure

- Adjust ambient temperature as specified.
- Apply power supply.
- Set I/O conditions, logic state, etc. as specified.
- Apply triggering pulse under specified conditions of duration, rise and fall time to the specified terminal.
- Measure supply current after specified delay time.
- Increase the amplitude of the triggering pulse until latch-up occurs, or until the amplitude exceeds the specified value.
- Register the voltage across the device supply terminals, the supply current.
- If an increase in supply current occurs or if supply current is greater than the specified latch-up state current, latch-up occurs.
- Disconnect power source.

e) Time operation

t1 Connect device as specified.

t2 Set supply current limitation and voltage as specified. Set input and output conditions as specified, to place the device in specified logic state if appropriate.

t3 The triggering voltage or current is superimposed on the supply voltage.

t4 The total amplitude of the voltage across the supply voltage terminals at the instant of application is measured and recorded. In case of latch-up this is the latch-up voltage.

t5 After a specified delay time, the voltage across the supply voltage terminals is again measured and recorded. The supply current is also measured and recorded. If the voltage is observed to fall below the amplitude of the applied voltage or if an increase in supply current is observed, the device has latched-up. This is recorded as latch-up state voltage and the current as latch-up state current.

t6 After a specified delay time the trigger pulse is removed and the supply terminal returned to the state it had before the triggering was applied.

t7 If the device is in latch-up the power supply is to be disconnected.

t8 After a cool down time a second trigger pulse can be applied, repeating the operations specified at times t3 through t7, then continuing with the measurements as above.

NOTE If the value of the latch-up state voltage is higher than the supply voltage, the supply voltage terminal will return to the supply voltage level following the trailing edge of the trigger pulse.

f) Specified conditions

- Ambient or case temperature.
- Supply voltage.
- Terminals to be tested.
- Conditions at untested terminals: all inputs connected to ground or V_{CC} (V_{DD}), unless otherwise specified. All outputs are left open.
- Logic state.
- Maximum supply current.
- Conditions of triggering pulse:
 - Maximum amplitude
 - Duration
 - Rise and fall time

- Delay time before measurement of supply current.
- Cool down time.
- Limitation of supply current.

E – Precautions

- As high current may be needed to latch-up some integrated circuits, care has to be taken not to destroy the device during the measurement procedure, e.g. by using short pulses.
- If an integrated circuit has more than one supply voltage, each supply voltage or current has to be measured separately.

4) Quality assessment

For semiconductor technologies suffering from latch-up and similar effects, e.g. CMOS, FAST, the following requirements for qualification approval, capability approval and quality assessment shall apply. The requirements apply to Digital and Analogue integrated circuits.

A – Under Electrical characteristics in the Sectional Specification and the Detail Specification the following characteristics shall be specified.

- a) Latch-up current
- b) Latch-up voltage, where appropriate
- c) Latch-up supply voltage
- c) Latch-up state voltage, where appropriate

B – Qualification approval and capability approval

For qualification approval and capability approval the following test requirements shall be specified in the Detail Specification and be applicable to Group D.

- a) Latch-up current, minimum value under specified conditions of supply voltage, test temperatures, tested terminals, input terminal voltage, logic state and polarity of triggering current.
- b) Latch-up voltage, minimum value under specified conditions of supply voltage, test temperatures, tested terminals, input terminal voltage, logic state and polarity of triggering current.
- c) Latch-up supply voltage, minimum value under specified conditions of supply voltage, test temperatures, input terminal voltage and logic state.
- d) Latch-up state voltage, minimum value under specified conditions of supply voltage, test temperatures, input terminal voltage and logic state.

C – Quality conformance inspection

The following test requirements shall apply to Group C if required by the Detail Specification.

- a) Latch-up current, minimum value under specified conditions of supply voltage, test temperatures, tested terminals, input terminal voltage, logic state and polarity of triggering current.
- b) Latch-up supply voltage, minimum value under specified conditions of supply voltage, test temperatures, input terminal voltage and logic state.

4.6 Environmental testing procedures

The following tests are indicated “destructive” (D) or “non-destructive” (ND) according to their effect on the device.

For additional information on delivery : see 3.4.8

Definition of axes: see 4.7

4.6.1 Storage at high and low temperatures

1) Storage at high temperature (ND)

This test shall be in accordance with Test Ba of IEC 68-2-2 (1974) [with supplement 68-2-2A (1976)], amended by IEC 749 with the following requirements:

Preconditioning: none

Initial measurements: optional