

**Harmonized system of quality
assessment for electronic components**

Family specification: AC MOS digital integrated circuits

The European Standard EN 190116:1993 has the status of a
British Standard

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Austria	Italy
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Denmark	Netherlands
Finland	Norway
France	Portugal
Germany	Spain
Greece	Sweden
Iceland	Switzerland
Ireland	United Kingdom

This British Standard, having been prepared under the direction of the Electronic Components Standards Policy Committee, was published under the authority of the Standards Board and comes into effect on 15 March 1994

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Contents

	Page
Cooperating organizations	Inside front cover
National foreword	ii
Foreword	2
1 Limiting conditions of use for the family	5
2 Recommended operating and associated characteristics for the family	5
3 Test methods and procedures — mechanical data	15
4 Inspection requirements	27
National annex NA (informative) Committees responsible	Inside back cover
National annex NB (informative) Cross-references	Inside back cover
Figure 1 — Loading circuit	11
Figure 2 — Transition times and propagation delay times	11
Figure 3 — Clock-pulse rise and fall times and pulse width	11
Figure 4 — Set-up times, hold times, removal time and propagation delay times for edge triggered sequential logic circuits	12
Figure 5 — Loading circuit	12
Figure 6 — 3-state propagation delay wave shapes	13
Figure 7 — Loading circuit	13
Figure 8 — Transition times and propagation delay times	13
Figure 9 — Clock-pulse rise and fall times and pulse width	14
Figure 10 — Set-up times, hold times, removal time and propagation delay times for edge triggered sequential logic circuits	14
Figure 11 — Loading circuit	14
Figure 12 — 3-state propagation delay wave shapes	15
Figure 13	16
Figure 14 — Input pulse waveforms	18
Figure 15 — Example of a test set-up for positive and negative trigger current	20
Figure 16 — Timing for latch-up immunity tests	21
Figure 17	22
Figure 18 — 14-lead pinout for 20-terminal lead-less chip carrier	24
Figure 19 — 16-lead pinout for 20-terminal lead-less chip carrier	24
Figure 20 — 18-lead pinout for 20-terminal lead-less chip carrier	25
Figure 21 — 24-lead pinout for 28-terminal lead-less chip carrier	25
Table 1 — AC series	6
Table 2 — ACT series	8
Table 3	15
Table 4	23
Table 5	27

National foreword

This British Standard has been prepared under the direction of the Electronic Components Standards Policy Committee and is the English language version of EN 190116:1993 *Family specification: AC MOS digital integrated circuits*, published by the European Committee for Electrotechnical Standardization (CENELEC) Electronic Components Committee (CECC).

The British Standard which implements the CECC Rules of Procedure is BS 9000 *General requirements for a system for electronic components of assessed quality — Part 2:1991 Specification for the national implementation of the CECC system*.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, pages 2 to 30, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

UDC

Descriptors: Quality, electronic components, AC MOS digital integrated circuits

English version

Family specification: AC MOS digital integrated circuits

Spécification de famille:
Circuits intégrés logiques AC MOS

Familienspezifikation

This European Standard was approved by CENELEC Electronic Components Committee (CECC) on 06 December 1992. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the General Secretariat of the CECC or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the CECC General Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom. The membership of the CECC is identical, with the exception of the national electrotechnical committees of Greece, Iceland and Luxembourg.

CECC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

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Foreword

The CENELEC Electronic Components Committee (CECC) is composed of those member countries of the European Committee for Electrotechnical Standardization (CENELEC) who wish to take part in a harmonized System for electronic components of assessed quality.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognized Mark, or Certificate, of Conformity. The components produced under the System are thereby acceptable in all member countries without further testing.

This European Standard was prepared by CECC WG 9, "Integrated circuits".

The text of the draft based on document CECC (Secretariat) 3120 was submitted to the formal vote; together with the voting report, circulated as document CECC (Secretariat) 3275 it was approved by CECC as EN 190116 on 06 December 1992.

The following dates were fixed:

- latest date of announcement of the EN at national level (doa) 1994-01-11
- latest date of publication of an identical national standard (dop) 1994-07-11
- latest date of declaration of national standards obsolescence 1994-07-11
- latest date of withdrawal of conflicting national standards (dow) 2004-01-11

AVA Documents
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1 Limiting conditions of use for the family (Not for inspection purposes)

1.1 Maximum supply voltage positive

$$V_{DD} = +6 \text{ V}$$

1.2 Maximum supply voltage negative

$$V_{CC} = -0,5 \text{ V}$$

1.3.1 Maximum dc input protection diode current

$$I_{IK} = \pm 20 \text{ mA}$$

OR (whichever is the worst case)

1.3.2 Maximum input voltage

$$V_I = V_{DD} + 0,5 \text{ V}^{1)}$$

1.4.1 Maximum dc output diode current

$$I_{OK} = \pm 50 \text{ mA}$$

OR (whichever is the worst case)

1.4.2 Maximum output voltage

$$V_O = V_{DD} + 0,5 \text{ V}^{1)}$$

1.5 Maximum dc output source or sink current per output pin

$$I_O = \pm 50 \text{ mA}$$

1.6 Maximum dc, supply I_{DD} or I_{SS} pin current

$$I_{DD} \text{ or } I_{GND} = \pm 100 \text{ mA}$$

(For up to four outputs per device add $\pm 25 \text{ mA}$ for each additional output).

1.7 Ambient operating temperature range T_{amb}

74 AC/ACT: 0°C to $+70^\circ\text{C}$

54 AC/ACT: -55°C to $+125^\circ\text{C}$

1.8 Storage temperature range T_{stg}

-65°C to $+150^\circ\text{C}$

2 Recommended operating and associated characteristics for the family

(Not for inspection purposes)

These conditions apply over the operating temperature range, unless otherwise specified in the DS.

All voltages are referenced to ground.

AC SERIES: Operating supply voltages $V_{DDB} = 3 \text{ V}^{(*)}$ to $V_{DDA} = 5,5 \text{ V}$

* No parametric or switching characteristics are specified at V_{DD} less than 3 V .

At V_{DD} between 2 V and 3 V the output conditions will stay at their previous state so battery back-up is allowed for data retention at these voltages, with the following conditions:

$$V_{IH} \geq 0,7 V_{DD}; V_{IL} \leq 0,3 V_{DD}; V_{OH} \geq 0,7 V_{DD} (I_{OH} = -20 \mu\text{A}) \text{ and}$$

$$V_{OL} \leq 0,3 V_{DD} (I_{OL} = +20 \mu\text{A})$$

¹⁾ Unless otherwise specified in the detail specification.

Table 1 — AC series

Parameters	Symbol	V _{DD} (V)	54/74 AC						Unit	
			T _{amb} min.		+ 25 °C		T _{amb} max.			
			min.	max.	min.	max.	min.	max.		
CONDITIONS OF TEST										
2.1 High level input voltage	V _{IHB}	3,0	2,1		2,1		2,1		V	
		4,5	3,15		3,15		3,15		V	
		5,5	3,85		3,85		3,85		V	
2.2 Low level input voltage	V _{ILA}	3,0		0,9		0,9		0,9	V	
		4,5		1,35		1,35		1,35	V	
		5,5		1,65		1,65		1,65	V	
DC PARAMETERS TO BE VERIFIED IN SUB-GROUP A3, A4a, A4b										
2.3 Quiescent supply current V _I = 0 V or V _{DD} I _O = 0 μA	I _{DDA} a	5,5		8,0		8,0		80,0	μA	
2.4 High level output voltage V _I = V _{IHB} or V _{ILA}	V _{OHB} b									
2.4.1 I _O = − 50 μA		3,0	2,9		2,9		2,9		V	
		4,5	4,4		4,4		4,4		V	
		5,5	5,4		5,4		5,4		V	
2.4.2 I _O = − 12 mA		3,0	2,4		2,56		2,4		V	
2.4.3 I _O = − 24 mA		4,5	3,7		3,86		3,7		V	
	5,5	4,7		4,86		4,7		V		
2.5 Low level output voltage V _I = V _{IHB} or V _{ILA}	V _{OLA} b									
2.5.1 I _O = + 50 μA		3,0		0,1		0,1		0,1	V	
		4,5		0,1		0,1		0,1	V	
		5,5		0,1		0,1		0,1	V	
2.5.2 I _O = + 12 mA		3,0		0,4		0,36		0,50	V	
2.5.3 I _O = + 24 mA		4,5		0,4		0,36		0,50	V	
	5,5		0,4		0,36		0,50	V		
2.6 Positive a) and negative b) input clamping voltage a) GND open, V _{DD} = 0 V b) V _{DD} open, GND = 0 V I _{IK} = 1 mA	V _{IK}				0,4	1,5			V	
2.7 Input leakage current V _I = 0 V or V _{DD}	I _{I(off)A}	5,5		0,1		0,1		1,0	μA	

^a Unless otherwise specified in the DS
^b Not applicable to open drain outputs

Table 1 — AC series

Parameters		Symbol	V _{DD} (V)	54/74 AC						Unit
				T _{amb} min.		+ 25 °C		T _{amb} max.		
				min.	max.	min.	max.	min.	max.	
2.8	3-state output off-state current V _I = V _{DD} or 0 V V _O = 0 V for I _{OZL} V _O = V _{DD} for I _{OZH}	I _{OZA}	5,5		0,5		0,5		10,0	μA
CAPACITANCE TO BE VERIFIED IN SUB-GROUP D5										
2.9	Power dissipation capacitance	C _{PDA} a	5,5			a				pF
ADDITIONAL INFORMATION (Not for inspection purpose)										
2.10	Noise margin at low level output (V _{ILA} – V _{OLA}) I _O = + 50 μA	V _{NLB}	3,0 4,5 5,5	0,8 1,25 1,55		0,8 1,25 1,55		0,8 1,25 1,55		V V V
2.11	Noise margin at high level output (V _{OHB} – V _{IHB}) I _O = – 50 μA	V _{NHB}	3,0 4,5 5,5	0,8 1,25 1,55		0,8 1,25 1,55		0,8 1,25 1,55		V V V
2.12	Input rise and fall time between V_{ILA} and V_{IHB}	t _r , t _f b	3,6 to 5,5		8,0		8,0		8,0	ns/V
2.13	Maximum continuous internal power dissipation with reference to derating curve or factor related to reference point temperature or ambient temperature	P _{DA} Reduction factor (mW/°C)	T _{JA} = 150 °C Case DG: P _{DA} = 1,25 W f = 10 mW/°C Case PC: P _{DA} = 1,25 W f = 11 mW/°C							
a See measurement method in clause 3.4 here after and limits for each type in the relevant DS. b Except for Schmitt inputs.										