

Low-voltage switchgear and controlgear — Controller and device interface systems — Actuator Sensor interface (AS-i)

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ICS 29.130.20

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National foreword

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A list of organizations represented on this subcommittee can be obtained on request to its secretary.

Attention is drawn to the fact that this standard is subject to certain patent rights. Details are given in the EN foreword.

Textual error

The textual error set out below was discovered when the English language version of EN 50295 was adopted as the national standard. It has been reported to CEN in a proposal to amend the text of the European Standard.

In Figure 27 the supply rails to AS-i slave have their polarity incorrectly indicated. The note defining V_1 and V_2 gives the correct voltage polarities. The circuit in Figure 28 shows the correct rail polarities.

Cross-references

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Summary of pages

This document comprises a front cover, an inside front cover, the EN title page, pages 2 to 79 and a back cover.

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Descriptors: low-voltage switchgear, control equipment, automatic systems, interfaces sensor-actuator, definition, classification, marking, performance evaluation, equipment specification, tests

English version

**Low-voltage switchgear and controlgear —
Controller and device interface systems —
Actuator Sensor interface (AS-i)**

Appareillage à basse tension —
Systèmes d'interface appareil de commande - appareils —
Interface capteur-actionneur (AS-i)

Niederspannungsschaltgeräte Steuerungs - und
Geräte-Interface Systeme —
Aktuator Sensor Interface (AS-i)

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European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
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Foreword

This European Standard was prepared by Technical Committee CENELEC TC 17B, Low-voltage switchgear and controlgear including dimensional standardization.

The text of the draft was submitted to the Unique Acceptance Procedure and was approved by CENELEC as EN 50295 on 1998-12-01.

There are patent rights linked to EN 50295:1999. The patent holder, SIEMENS Aktiengesellschaft has declared to grant licences to these patents and corresponding patent applications under fair and reasonable terms in accordance with CEN/CENELEC Memorandum 8.

The following dates were fixed:

- | | | |
|--|-------|------------|
| — latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement | (dop) | 1999-12-01 |
| — latest date by which the national standards conflicting with the EN have to be withdrawn | (dow) | 1999-12-01 |

Annexes designated “normative” are part of the body of the standard.

In this standard, both annexes A and B are normative.

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1 Scope

This standard specifies requirements for a bit-oriented interface system between a single controlling device and control circuit devices or switching elements as defined in EN 60947-1, connected by an unshielded, untwisted two-wire cable carrying data and power. It also enables the interchangeability of components which have such interfaces.

This standard specifies:

- requirements for interfaces and for electromechanical structures for slaves and masters;
- performance of slaves, electromechanical structures and masters under normal service conditions;
- constructional and performance requirements;
- tests to verify conformance to the requirements.

Specific requirements for the various profiles for slaves and masters are given in annexes A and B.

NOTE 1 The standardized low-voltage switchgear and controlgear products covered by the EN 60947 series are:

- EN 60947-1: *General rules*;
- EN 60947-2: *Circuit-breakers*;
- EN 60947-3: *Switches, disconnectors, switch-disconnectors and fuse-combination units*;
- EN 60947-4: *Contactors and motor-starters*;
- EN 60947-5: *Control-circuit devices and switching elements*;
- EN 60947-6: *Multiple function equipment*;
- EN 60947-7: *Ancillary equipment*.

NOTE 2 Where inputs and outputs (I/O) are described in this standard, their meaning is relative to the master. The meaning relative to the application is the opposite.

2 Normative references

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

- EN 55011:1998, *Industrial, scientific and medical (ISM) radio-frequency equipment — Radio disturbance characteristics — Limits and methods of measurement*.
- EN 60947-1:1997, *Low-voltage switchgear and controlgear — Part 1: General rules*.
- EN 60947-5-1:1997, *Low-voltage switchgear and controlgear — Part 5-1: Control circuit devices and switching elements — Electromechanical control circuit devices*.
- EN 60947-5-2:1997, *Low-voltage switchgear and controlgear — Part 5: Control circuit devices and switching elements — Section 2: Proximity switches*.
- EN 60998-2-3:1993, *Connecting devices for low-voltage circuits for household and similar purposes — Part 2-3: Particular requirements for connecting devices as separate entities with insulation piercing clamping units*.
- EN 61000-4-2:1995, *Electromagnetic compatibility (EMC) — Part 4: Testing and measurement techniques — Section 2: Electrostatic discharge immunity test*.
- EN 61000-4-3:1996, *Electromagnetic compatibility (EMC) — Part 4: Testing and measurement techniques — Section 3: Radiated, radio-frequency, electromagnetic field immunity test*.
- EN 61000-4-4:1995, *Electromagnetic compatibility (EMC) — Part 4: Testing and measurement techniques — Section 4: Electrical fast transient/burst immunity test*.
- EN 61131-2:1994, *Programmable controllers — Part 2: Equipment requirements and tests*.
- HD 384.4.41 S2:1996, *Electrical installation of buildings — Part 4: Protection for safety — Chapter 41: Protection against electric shock*.
- (IEC 60364-4-41:1992, mod)

3 Definitions, symbols and abbreviations

Alphabetical index of definitions

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3.1 Definitions

The following terms and definitions apply to this standard.

3.1.1

active slave

slave connected to the AS-i line and capable of communicating as specified in this standard

3.1.2

actuator Sensor interface (AS-i)

set of interfaces and serial communication method for the connection of low-voltage switchgear, controlgear and other simple devices to a controller

3.1.3

address

numerical parameter between 0 and 31 which specifies a node of an AS-i network

NOTE Address 0 is reserved for slaves which have not had an address assigned.

3.1.4

address assignment

replacement of the existing address of the AS-i slave with a new address

3.1.5

AS-i cycle

set of up to 33 transactions

NOTE A transaction may, in case of a detected fault, include one master request or slave response retransmission.

3.1.6

AS-i input

physical (external) or logical (internal) slave input port (see Figure 1)

3.1.7

AS-i line

two-wire cable utilized by AS-i slaves and the AS-i master for transferring information and power

3.1.8

AS-i master

unit on the AS-i line that manages the communication between the slaves and the controller

3.1.9

AS-i network

network composed of AS-i master, slaves, power supply and line

3.1.10

AS-i output

physical (external) or logical (internal) slave output port (see Figure 1)

3.1.11

AS-i power supply

combined d.c. supply and decoupling circuit needed for an AS-i network

3.1.12

AS-i slave

physical and logical means of connecting the application devices (actuator, sensor, or other components) to the AS-i line

NOTE A slave may be a stand-alone device or part of another device.

3.1.13

bit time (effective)

duration of the transmission of one bit (T_{bit})

3.1.14

decoupling circuit

part of the AS-i power supply for decoupling the d.c. source and for conditioning the physical data transmission within the AS-i network

3.1.15

field devices

items connected to the AS-i slave

NOTE 1 Examples are actuators, sensors, push-buttons, indicator lights.

NOTE 2 “Intelligent” field devices also include integrated AS-i circuitry.

3.1.16

I/O configuration (I/O code)

set of four bits which defines the direction of data flow at the four I/O ports of a slave

3.1.17

identification code (ID code)

set of four bits which defines the type of slave profile for a given I/O configuration

3.1.18

master pause

time between the last bit of a master request and the first bit of the slave response at the master

3.1.19

master request

data or parameter or function sent from the master to a single slave

3.1.20

non-volatile stored data

data that remains unchanged following power interruption

3.1.21

operation address

address of the AS-i slave other than the zero address

3.1.22

output current limit I_{Lim}

output current of the power supply which cannot be exceeded under all environmental and load conditions

3.1.23

send pause

period after receipt of the slave response during which no transmission occurs

3.1.24

slave pause

minimum time between the last bit of a slave response and the start of the first bit of the next master request

3.1.25

slave response

message from the slave to the master after a master request has been received and processed without error. The content of this response is either data or the result of a command

3.1.26

transaction

combination of a master request, master pause, slave response and send pause (see Figure 5)

3.1.27

volatile stored data

data that may change following power interruption

3.1.28

zero address

special address reserved for the online assignment of a new address to an AS-i slave

3.2 Symbols and abbreviations

APF	AS-i power failure
APM	Alternate Pulse Modulation
APO	AS-i Power-ON
AS-i	Actuator Sensor interface
T_{bit}	bit time
TS	Transaction Status
U_{b}	power supply voltage
U_{send}	peak value of the voltage pulses
$u(t)$	pulse waveform

4 Classification

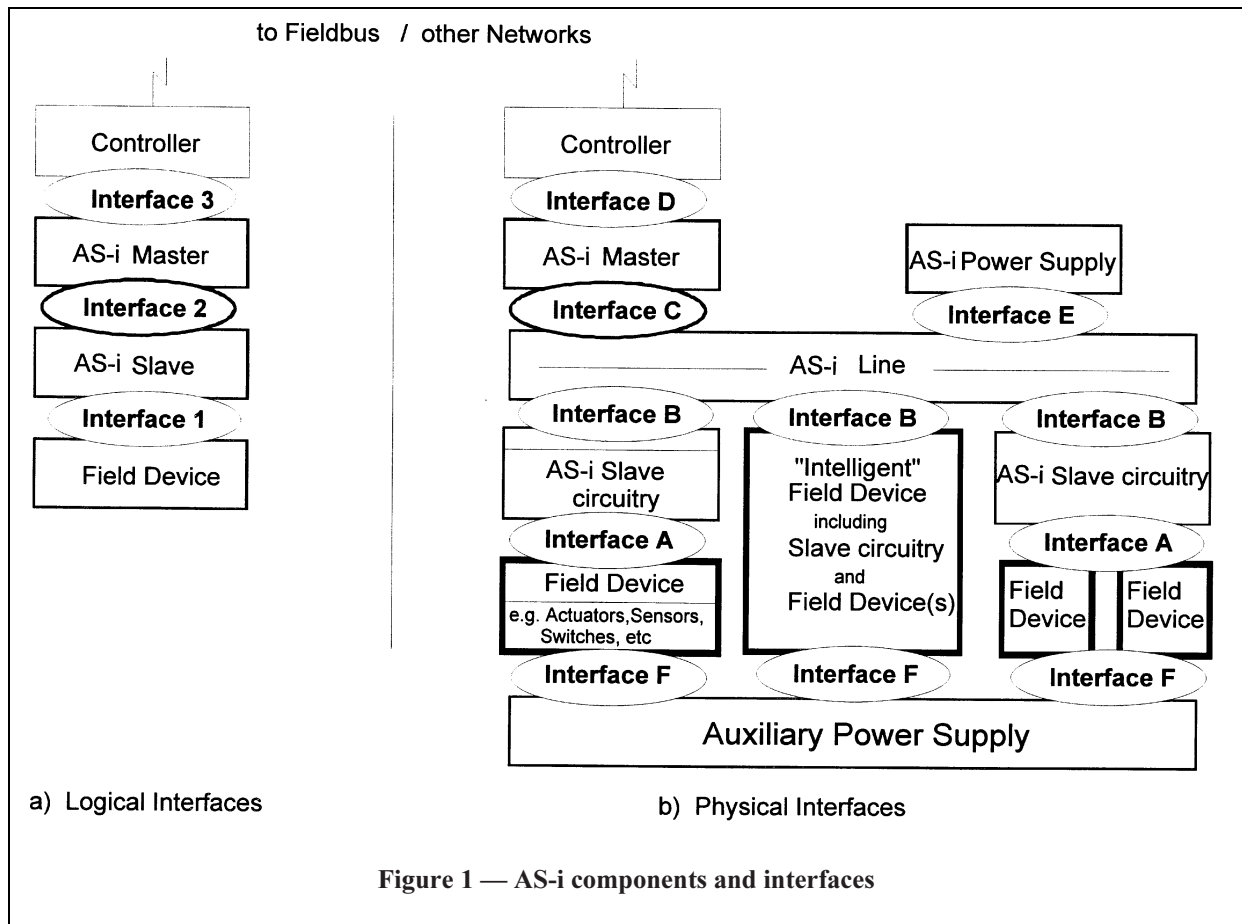
4.1 Overview

AS-i is usually applied at the lowest level in a multi-level automation hierarchy. AS-i concentrates on the typical requirements to connect binary elements with a controller.

AS-i can be used as an interface physically integrated into field devices e.g. actuators, sensors, or other devices and elements themselves, allowing design of “intelligent” binary actuators, sensors, or other devices and elements. Alternatively AS-i may be used in separate modules, each providing an interface for up to four conventional actuators and/or sensors or other devices and elements.

The AS-i structure contains two different types of interface, three logical and five physical as shown in Figure 1.

Logically, the AS-i system is a master-slave communication system composed of a single master and up to 31 slaves. The master sends data and parameters to each specific slave. The slave passes the data to the output ports or processes the requested procedure (e.g. reset_slave) and returns the input data or the result of the successfully processed procedure to the master.



The AS-I concept is independent of the specific field devices. It defines the mechanisms and all the components for the communication with a controlling device and it offers electromechanical structures for a standardized “interconnection system” for installation of actuators, sensors, or other devices and elements.

More than one standard field device may be connected via the physical interface A to the slave.

“Intelligent field devices” contain the slave circuitry, the physical interface A and the field device itself.

Annexes A and B define profiles for common types of devices that can be used in AS-i systems.

4.2 Components and interfaces (see Figure 1)

4.2.1 Components

4.2.1.1 AS-i slave

The AS-i slave includes the circuitry that determines the logical and functional behaviour of the unit and which can be accessed by the master via the AS-i line for data exchange, parameterization, and monitoring. It responds to a specific request from the master and it ensures that a malfunction of the attached actuator, sensor or other device or of the slave itself does not disturb the communication between the master and the other slaves in the network.

4.2.1.2 AS-i master

The AS-i master includes the circuitry that determines the logical and functional behaviour of the unit that organizes and monitors the network and schedules the exchange of data, parameters and commands with the AS-i slave via the AS-i line. The AS-i master sends master requests to an AS-i slave and receives slave responses from it.

4.2.1.3 AS-i power supply

The AS-i power supply provides power to the AS-i network and includes the decoupling circuitry.

4.2.1.4 AS-i line

The AS-i line provides the signalling and d.c. power connections between the AS-i devices.

4.2.2 Logical interfaces

4.2.2.1 Interface 1

Interface 1 is the slave interface that connects the AS-i slave with the actuators, sensors, or other devices and elements. It is characterized by several ports, which define the input, output or bi-directional input/output behaviour, the parameterization behaviour of the AS-i slave and the timing of the signals.

4.2.2.2 Interface 2

Interface 2 provides all logical definitions required for data exchange between the AS-i master and slaves. It comprises signalling of encoded information and the network management.

4.2.2.3 Interface 3

Interface 3 provides all functions used by the controller (host) to access the AS-i master for sending and receiving data to and from slaves, sending commands to a slave, to set or to get flags and values for several lists in the master. This interface allows the controller to manage the AS-i master's behaviour and thus the behaviour of the AS-i system. Typical functions include “set something” in the master or “get some information” from the master.

This interface is conceptual in nature and its definition is outside of the scope of this standard. The concrete representation of the interface depends on the implementation. To a large extent, it depends on features of the specific controller system.

4.2.3 Physical interfaces

4.2.3.1 Interface A

Interface A defines the physical connection between the field device and the AS-i slave circuitry including physical interface, signal levels and power requirements if any.

4.2.3.2 Interface B

Interface B defines the physical connection of the AS-i slave circuitry to the AS-i line including physical interface (mechanical and electrical), signal characteristics and power requirements.

4.2.3.3 Interface C

Interface C defines the physical connection of the AS-i master circuitry to the AS-i line including physical interface (mechanical and electrical), signal characteristics and power requirements.

4.2.3.4 Interface D

The definition of the physical interface between the AS-i master and the controller (interface D) is outside of the scope of this standard and shall be provided by the manufacturer.

4.2.3.5 Interface E

Interface E defines the physical connection of the AS-i power supply including the signal decoupling circuit, to the AS-i line.

4.2.3.6 Interface F

Interface F defines the physical interface between the field device and an external auxiliary power supply if any.

5 Characteristics

5.1 AS-i transmission system

5.1.1 General

The AS-i transmission system provides the communication between the AS-i slaves and the AS-i master, i.e. it represents interface 2 between a master and the slaves (see Figure 1).

The AS-i system is a digital, serial, multidrop, data communication with actuators and sensors including simultaneous power supply. Subclause 5.1.2 specifies the transmission of data between the master and a specific slave.

5.1.2 Signal characteristics

The characteristics of the transmitted signal and the modulation are defined in this subclause.

The bit time (T_{bit}) shall be 6 μs . Thus, the bit rate shall be $166\frac{2}{3}$ kbit/s. The maximum deviation from the nominal bit time shall not exceed $\pm 0,2\%$.

The transmission coding and encoding principle shall be as shown in Figure 2. Each master request or slave response shall include a start and an end bit. The idle state shall be represented by a “1”. Master request or slave response shall be encoded in Manchester II format with alternate pulse modulation (APM). The duration of each bit shall be 6 μs .

A “0” shall be encoded by a period of 3 μs high level followed by a period of 3 μs low level. A “1” shall be encoded by a period of 3 μs low level followed by a period of 3 μs high level. The transmitter shall be implemented as a current sink. The amplitude of the modulation current shall be between 55 mA and 68 mA. Together with the decoupling inductances of the decoupling circuit in the power supply, this current will lead to a negative voltage pulse at each rising edge and a positive voltage pulse at each falling edge. The ideal waveform of the pulses is:

$$u(t) \approx \pm U_{\text{send}} \times \sin^2 \left(\frac{2\pi}{6\mu\text{s}} t \right)$$

where U_{send} is a constant approximately equal to 2 V (see Figure 2).

NOTE In a real AS-i system, the falling edge of the pulses is flattened due to the behaviour of the decoupling circuit and the physical properties of the AS-i line.

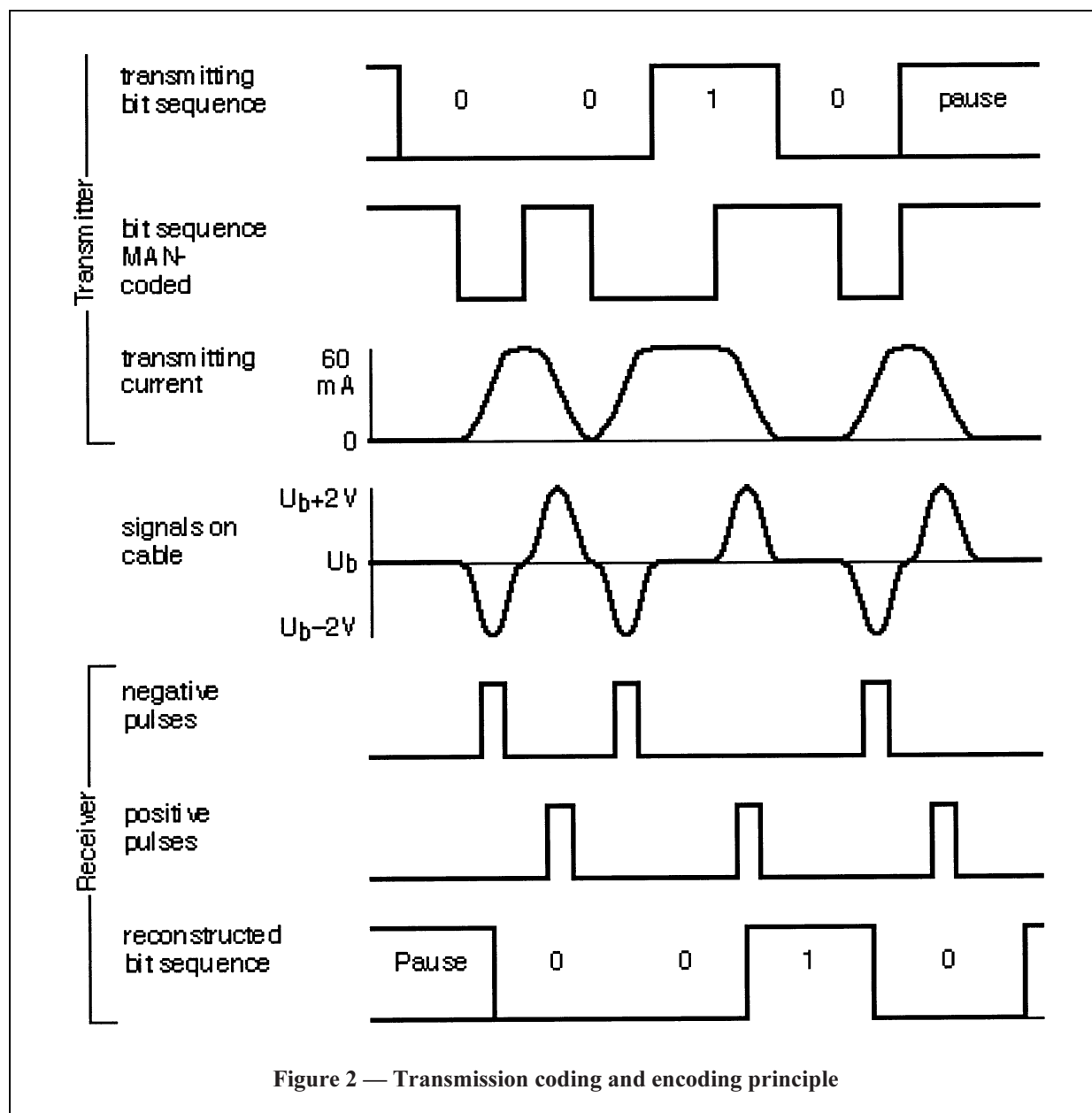


Figure 2 — Transmission coding and encoding principle

5.1.3 Power and data distribution

The simultaneous transmission of data and power on the AS-i line requires technical provisions for decoupling data and power.

The AS-i power supply provides d.c. power to devices on the AS-i line. Furthermore, it shall perform the main conditioning of physical data transmission within the system. This comprises the transmission signal forming and adaptation to the cable as well as ensuring the symmetry of the AS-i line. The adaptation is provided by a decoupling circuit.

NOTE Power and data distribution are not interdependent but are combined in the AS-i line to reduce cabling requirements.

The galvanic isolation of the AS-i line from the equipment ground shall be according to Figure 3. Externally connected components shall meet the PELV requirements of HD 384.4.41 S2.

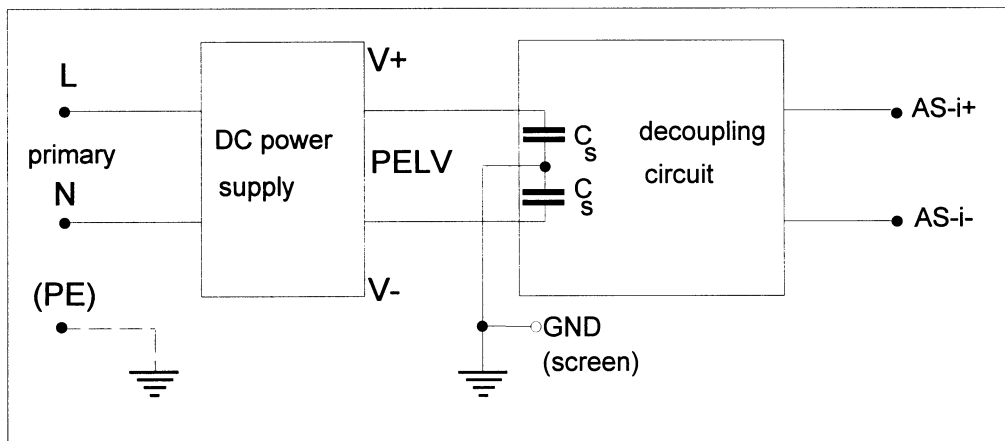


Figure 3 — AS-i power supply incorporating the decoupling circuit

5.2 AS-i topology

The AS-i system is a master-slave communication system composed of a single master and up to 31 slaves. Each slave shall have a unique address in the range 1 to 31. This address is called the operation address. The operation address shall be non-volatile.

The zero address is used during the change of a slave address. Normally, the zero address is non-volatile, for factory new slaves.

A single transaction shall be composed of a master request and a slave response. If a slave responds to a master request, it shall start its response within a period of 2,5 to 5,5 bit times after the end of a master request. The master shall be able to accept the start of a slave response within a period of 2,5 to 10 bit times after the end of its request, to allow for propagation delay on the line and the possible use of repeaters.

A slave shall not respond if it detects an erroneous master request. The slave shall not give any negative response. The master shall interpret the absence of a slave response as a negative response.

5.3 Data transmission

A data exchange shall be realised by the processing of transactions (see Figure 4). A transaction shall start with a master request (issued by the master to transfer data or a command to the slave). The master shall expect a slave response (issued by the slave to transfer data or a command result to the master) within a certain time. If the master does not receive a valid response from the slave within this time, it may retransmit the master request once. After receiving a valid response and after the send pause has elapsed, the master shall start the next transaction.

The AS-i master shall provide means for sending one master request by the master to a single slave and receiving a slave response from the slave. At a given time, the master shall process one, and only one, master request or slave response. After a transaction has been finished the next transfer can be processed by the master. In case of failure, no more than one re-transmission shall be processed in the same cycle.

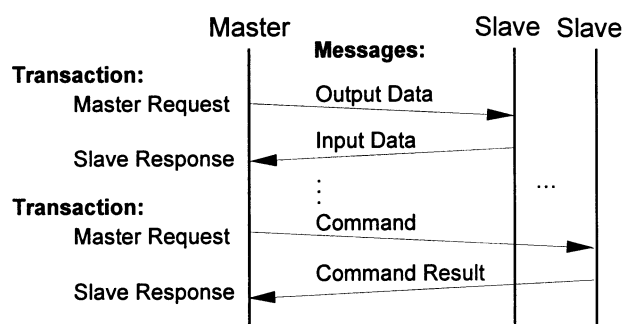


Figure 4 — Transactions

All times specified in this subclause are related to the signals on the AS-i line at the master terminals.

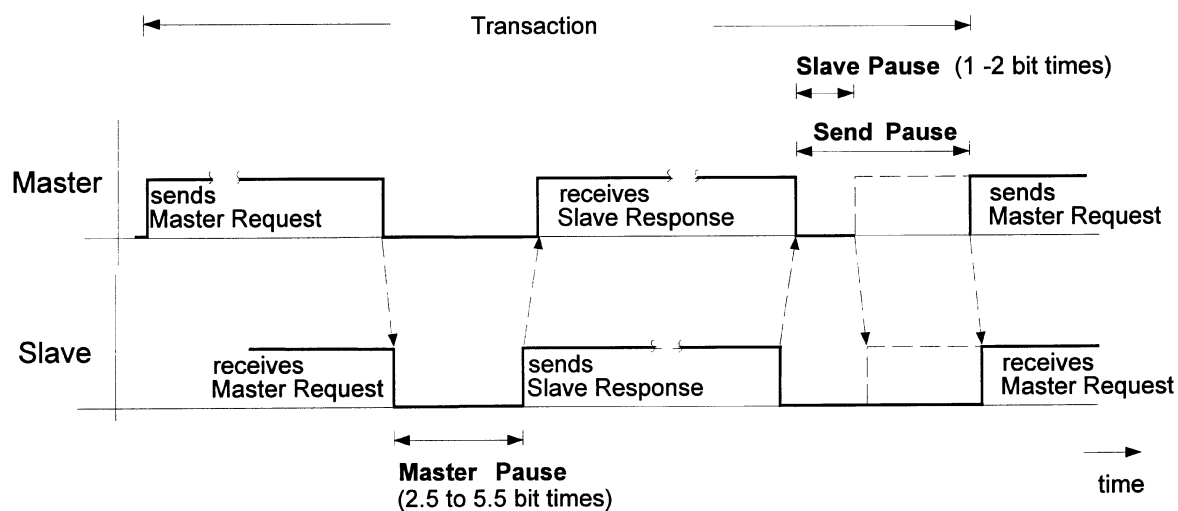


Figure 5 — Transaction cycle

A transaction shall be split into two actions (master request and slave response) and two time intervals (master pause and send pause) according to Figure 5. These actions and intervals consist of the following.

Master request:	sending a master request from the master to a single slave and expecting a response from the slave.
Master pause:	during this time the slave processes the requested function and produces the response data.
Slave response:	transmission of the slave data or the command result to the master.
Slave pause:	after receipt of the slave response there shall be a minimum period during which no subsequent transmission shall occur. This slave pause shall be 1 to 2 bit times.
Send pause:	after receipt of the slave response there shall be a minimum period during which no subsequent transmission shall occur. During normal operation with more than 30 transactions per AS-i cycle the time of this pause shall be one slave pause. If there are 30 or less transactions per AS-i cycle the send pause may be prolonged to a maximum of 500 μ s. In this case the AS-i cycle time shall not be longer than 5 ms.
Slave response time-out:	if no response is received from the slave within a defined time (the slave response time-out) the master shall either end the transaction or repeat the transmission. This time shall be a maximum of 10 bit times. This time shall be determined by the master pause, signal propagation on the line and the repeaters. The time-out timer shall start at the end of the transmission of the master request. Within the slave response time-out the master expects the beginning of a response frame from the slave. After this time, the transmission function determines the absence of a slave response.

During the send pause, the master shall not transmit any signal. It shall sense the AS-i line to allow the detection of an end bit error.

Subsequent data shall be transmitted only if the AS-i line was idle for at least the duration of a slave pause, after the beginning of the send pause. Every disturbance of this idle state shall cause a restart of the send pause.

A transaction shall be considered successfully processed if:

- **after** the minimum master pause; and
- **before** the time of slave response time-out + 7 T_{bit} has elapsed;
- **a valid** slave response has been received.

After Master Power On (MPO) the master shall process a send pause.

5.4 AS-i transactions

5.4.1 AS-i transaction types

Four AS-i transaction types are defined in Table 1 for data exchange, parameterization, network management, and diagnostics. All master requests and slave responses shall have the same structure and the same length of 14 bits (master request) and 7 bits (slave response).

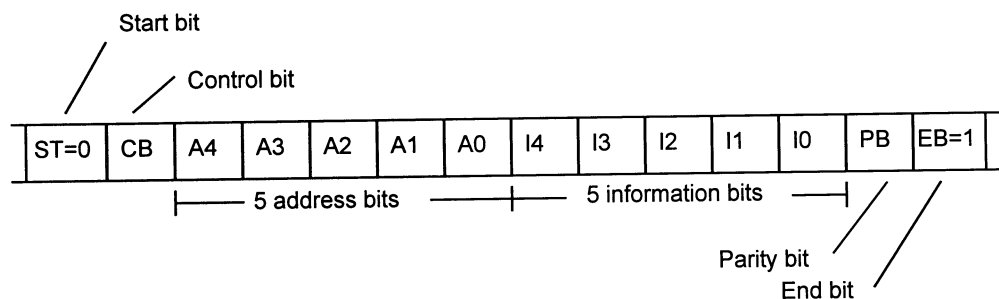
Table 1 — AS-i transaction types

Transaction type	Description
Data_exchange	Delivery and/or receipt of the bit pattern to/from the data output/input ports of the slave.
Write_parameter	Delivery of the bit pattern to the parameter ports of the slave.
Address_assignment	Assignment of a non-volatile address (1...31) to a slave to replace a zero address.
Commands	Miscellaneous functions: reset_slave delete_address read_I/O_configuration read_identification_code read_status read_reset_status reserve_R1

The master may be able to issue all or only some of the requests (according to a specific master profile), whereas any slave shall be able to respond to all master requests defined, except for the address_assignment request, which is optional.

5.4.2 Structure of the master request

The master request shall be composed as follows:



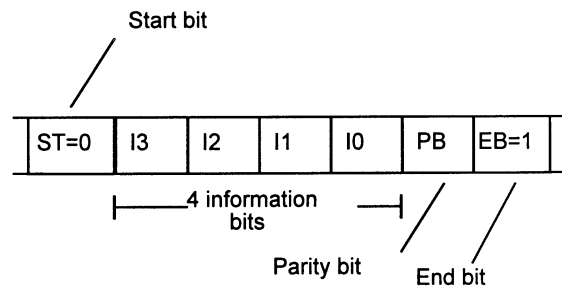
The meaning of each bit shall be as shown in Table 2.

Table 2 — Master request

Bit string	Semantic	Comments
ST	Start bit	Identifies the beginning of the master request, always 0.
CB	Control bit	Identifies the data/parameter transmission in the information cell. 0 = data/parameter transmission/address assignment. 1 = command transmission.
A4...A0	Address (5 bit)	To address the listed slaves. 0×00 = zero address. $0 \times 01...0 \times 1F$ = slave 1 through 31.
I4...I0	Information	These 5 bits contain the information to be transferred to the slave for every request type.
PB	Parity bit	For verification of master requests by the slave. The master request has even parity. 0 = even count of 1-symbols in (CB, A4...A0, I4...I0). 1 = odd count of the 1-symbols in (CB, A4...A0, I4...I0).
EB	End bit	Marks the end of the master request.

5.4.3 Structure of the slave response

The slave response shall be composed as follows.



The meaning of the each bit shall be as shown in Table 3.

Table 3 — Slave response

Bit string	Semantic	Comments
ST	Start bit	Marks the slave response beginning.
I3...I0	Information	Information of the slave response.
PB	Parity bit	For verification of master requests by the slave. The master request has even parity. 0 = even count of 1-symbols in (I3...I0). 1 = odd count of the 1-symbols in (I3...I0).
EB	End bit	Marks of the end of the slave response.

5.4.4 Individual AS-i transactions

5.4.4.1 General

Subclause 5.4.4 specifies requirements for the different transactions. The detailed functions of a slave after receiving a master request are defined in 8.2.

All other codes (bit patterns of transactions not defined in this standard) are reserved and shall not be used by any implementation.

5.4.4.2 Data_exchange

The data_exchange request shall be used by the master to transfer four bits of data (I3...I0) to the data output register of the slave and to get four bits of data from the slave input register.

The data_exchange request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0		EB
=0	=0	A4	A3	A2	A1	A0	=0	D3	D2	D1	D0	PB	=1

The bits A4...A0 shall contain an operation address (1...31).

The slave response shall have the following structure.

ST	I3	I2	I1	I0		EB
=0	D3	D2	D1	D0	PB	=1

If the slave is not activated, no response shall be generated.

If the I/O configuration of the slave is $0 \times 0F$, no response shall be generated.

5.4.4.3 Write_parameter

The write_parameter request shall be used by the master to transfer the four parameter bits (I3...I0) to the parameter output register of the slave and to get four parameter bits from the slave parameter ports.

The write_parameter request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0		EB
=0	=0	A4	A3	A2	A1	A0	=1	P3	P2	P1	P0	PB	=1

The bits A4...A0 shall contain an operation address (1...31).

The slave response shall have the following structure.

ST	I3	I2	I1	I0		EB
=0	P3	P2	P1	P0	PB	=1

The write_parameter request may affect the behaviour of the slave.

5.4.4.4 Address_assignment

The address_assignment request shall be used by the master to force the slave to store the given address (I4...I0) in non-volatile form and to use this address when responding to master requests.

The address_assignment request shall have the following structure.

ST	CB	A4	A3	A2	A1	A0	I4	I3	I2	I1	I0		EB
=0	=0	=0	=0	=0	=0	=0	=A4	=A3	=A2	=A1	=A0	PB	=1

The bits A4...A0 shall contain the zero address (0×00).

The slave response shall have the following structure.

ST	I3	I2	I1	I0	PB	EB
=0	=0	=1	=1	=0	PB	=1

After a successful address_assignment, a slave shall respond with the new address.

5.4.4.5 Reset_AS-i_slave

The reset_AS-i_slave request shall be used by the master to reset a specific slave.

This command shall be encoded in the information part of the master request by $0 \times 1C$. The reset_AS-i_slave command shall have the following structure.

ST	CB	A4	A3	A2	A1	A0	I4	I3	I2	I1	I0	PB	EB
=0	=0	A4	A3	A2	A1	A0	=1	=1	=1	=0	=0	PB	=1

The slave response shall have the following structure.

ST	I3	I2	I1	I0	PB	EB
=0	=0	=1	=1	=0	PB	=1

The reset_AS-i_slave request affects the slave's state machine.

5.4.4.6 Delete_address (temporary)

The delete_address request shall be used by the master to delete the operation address of a specific slave.

This command shall be encoded in the information part of the master request as 0×00 . The delete_address command shall have the following structure.

ST	CB	A4	A3	A2	A1	A0	I4	I3	I2	I1	I0	PB	EB
=0	=1	A4	A3	A2	A1	A0	=0	=0	=0	=0	=0	PB	=1

The slave response shall have the following structure.

ST	I3	I2	I1	I0	PB	EB
=0	=0	=0	=0	=0	PB	=1

After a successful delete_address, a slave shall respond with the zero address which is stored in a volatile form.

The delete_address request does not affect the slave's state machine.

A delete_address request to a slave with a zero address shall generate a slave response, but shall have no other effect.

A delete_address request shall not be issued by the master if the slave is in the process of storing its address into the non-volatile memory (processing the address_assignment request).

NOTE This is to prevent an undefined result of the storage process.

5.4.4.7 Read_I/O_configuration

The read_I/O_configuration request shall be used by the master to read the I/O configuration of a specific slave.

This command shall be encoded in the information part of the master request as 0×10 . The read_I/O_configuration request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0		EB
=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=0	=0	PB	=1

The slave response shall have the following structure.

ST	I3	I2	I1	I0		EB
=0	I3	I2	I1	I0	PB	=1

5.4.4.8 Read_identification_code

The command read_identification_code request shall be used by the master to read the identification code of a specific slave.

This command shall be encoded in the information part of the master request as 0×11 . The read_identification_code request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0		EB
=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=0	=1	PB	=1

The slave response shall have the following structure.

ST	I3	I2	I1	I0		EB
=0	I3	I2	I1	I0	PB	=1

5.4.4.9 Read_status

The read_status request shall be used by the master to read the status of a specific slave.

This command shall be encoded in the information part of the master request as $0 \times 1E$. The read_status request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0		EB
=0	=1	A4	A3	A2	A1	A0	=1	=1	=1	=1	=0	PB	=1

The slave response shall have the following structure.

ST	I3	I2	I1	I0	EB	
=0	S3	S2	S1	S0	PB	=1

The actual values of S0 to S3 of the status bits shall not be affected by the request.

The slave shall provide four bits for status values. These four bits are independent of each other and shall have the following semantics.

- S0: 0 – address (non-volatile)
1 – address (volatile)
- S1: 0 – no parity bit error detected
1 – parity bit error detected
- S2: 0 – no end bit error detected
1 – end bit error detected
- S3: 0 – no error_reading non-volatile memory
1 – error_reading non-volatile memory

The information given in the status register may be used for diagnostic purposes or for the master to determine what action can be taken to recover from a fault condition.

5.4.4.10 Read_reset_status

The read_reset_status shall be used by the master to read the status and to reset the status bits of a specific slave.

This command shall be encoded in the information part of the master request as $0 \times 1F$. The read_reset_status command request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0	EB	
=0	=1	A4	A3	A2	A1	A0	=1	=1	=1	=1	=1	PB	=1

The slave response shall have the following structure.

ST	I3	I2	I1	I0	EB	
=0	S3	S2	S1	S0	PB	=1

After transmitting the slave response, the values of S1 to S3 of the status bits shall be 0.

The semantics of the status bits shall be the same as defined for read_status.

5.4.4.11 Reserve_R1

NOTE The reserve_R1 request is under further consideration.

This command shall be encoded in the information part of the master request as 0×12 . The reserve_R1 request shall have the following structure.

ST	CB						I4	I3	I2	I1	I0	EB	
=0	=1	A4	A3	A2	A1	A0	=1	=0	=0	=1	=0	PB	=1

The slave response shall have the following structure:

ST	I3	I2	I1	I0	EB	
=0					PB	=1

5.5 Error detection

Any master request and slave response on the AS-i line shall be checked by the receiver in the slave or in the master for possible transmission errors including the following:

- Start_bit_error:** the initial pulse following a pause shall be of negative polarity. This pulse is the reference for bit decoding. The first bit detected shall be of the value 0. Violation of this rule shall be detected as a start bit error.
- Alternation_error:** two consecutive pulses shall be of different polarity. A negative pulse shall be followed by a positive pulse and vice versa. Violation of this rule shall be detected as alternation_error.
- No_information_error:** within a master request or slave response, pulses (of positive or negative polarity) shall be detected within a period of $(n \times 6 \mu\text{s}) \begin{smallmatrix} +1.0 \mu\text{s} \\ -0.5 \mu\text{s} \end{smallmatrix}$ after the initial pulse of a master request or slave response, where $n = 13$ for a master request and $n = 6$ for a slave response. Violation of this rule shall be detected as no_information_error.
- Parity_error:** the sum of all information bits of the master request or slave response (excluding start and end bits, including parity bit) shall be even. Violation of this rule shall be detected as parity_error.
- End_bit_error:** the pulse to be detected $n \times 6 \mu\text{s}$ after the start pulse shall be of positive polarity, where $n = 13$ for a master request and $n = 6$ for a slave response. This stop pulse shall end the master request or slave response. Violation of this rule shall be detected as an end_bit_error.
- Length_error:** a length_error shall be detected if a signal other than a pause is detected either:
- during the first bit time after the end pulse of a master request for synchronized slaves (during the first three bit times for non-synchronized slaves); or
 - during the first bit time after the end pulse of a slave response (i.e. during the minimum slave pause).

If any of these errors occur, the master request or slave response shall be treated as invalid.

6 Product information

6.1 Nature of information

The following information shall be given by the manufacturer.

6.1.1 Instructions for installation, operation and maintenance

The manufacturer shall specify in his documents or catalogues the conditions for installation, operation and maintenance of the interface components.

6.1.2 Identification

- a) The manufacturer's name or trade mark.
- b) A type designation or other marking which makes it possible to identify the product and to get the relevant information from the manufacturer or his catalogue.
- c) Reference to this standard if the manufacturer claims compliance.

Basic rated values and utilization

- d) Current ratings.
- e) Connection and wiring identification as specified in Table 4.

Table 4 — Connection and wiring identification

Physical interface	Type	Function	Wire colour	Terminal number
B, C, E	AS-i line	AS-i (+) AS-i (-)	Brown Blue	1 3
A	INPUT port (with connectors according to annex D of EN 60947-5-2)	Power supply (+) Input data 1 Power supply (-) Input data 2	*)	1 2 ¹⁾ 3 4 ¹⁾
A	INPUT port solid state (with terminals)	Power supply (+) (4×) Input data (4×) Power supply (-) (4×)		11...41 12/14...42/44 13...43
A	OUTPUT port solid state (with connectors. according to annex D of EN 60947-5-2)	Power supply (+) (npn) (4×) Power supply (-) (pnp) (4×) Output, parameter, etc. (4×)		1 3 4
A	OUTPUT port relays	Change-over contact Normally closed contact (NC) Normally open contact (NO)		1 2 4
A	OUTPUT port solid state (with terminals)	Power supply (+) (npn) (4×) Power supply (-) (pnp) (4×) Output data bit (4×)		11...41 13...43 14...44
F	Auxiliary power port	Aux. power (+) Aux. power (-)	Brown Blue	1 3
B + F	AS-i line + auxiliary power port ²⁾	AS-i (+) AS-i (-) U_{aux} (+) U_{aux} (-) PE ³⁾	Brown Blue Black White Green/Yellow	1 3 4 2 5

*) Wire colours for proximity switches shall conform to Table 3 of EN 60947-5-2.
¹⁾ When only one INPUT pin per connector is used, the connector pins 2 and 4 shall be bridged internally.
²⁾ When the same connector or cable is used for both voltages, the auxiliary power supply shall be of the SELV or PELV type.
³⁾ If used.

6.2 Marking

6.2.1 AS-i standard cable

The AS-i standard cable shall be coloured yellow and the “+” and “-” conductors shall be clearly identified. If colours are used for identification they shall be: brown = + and blue = -.

6.2.2 AS-i slave

The IP protection rating of the slave shall be stated in the data sheet according to EN 60947-1.

6.2.3 AS-i power supply

The connections of an AS-i power supply shall be identified as specified in Table 5 if it is a single phase a.c. power supply. This marking is mandatory.

Table 5 — AS-i power supply connection markings

Power supply	Marking	Specification
Primary (a.c. type)	L	Phase
	N	Neutral
	PE	Protective earth
Secondary (Interface E)	AS-i+	AS-i line positive
	AS-i -	AS-i line negative
	GND	Equipment earth and/or shield

6.2.4 AS-i master

The type of isolation between AS-i ports at the master and the controller shall be stated by the manufacturer.

6.2.5 Profiles and all other AS-i components

Masters and slaves shall be marked in order to permit the unambiguous identification of master and slave profiles as defined in annexes A and B.

Marking shall be indelible and easily readable, and shall not be placed on parts normally removable in service.

7 Normal service, mounting and transport conditions

7.1 Normal service conditions

7.1.1 General

Unless otherwise specified in this standard, AS-i components shall be capable of operating under the conditions specified in 7.1.2 to 7.1.4.

If the conditions for operation differ from those given in this standard, the user shall state the deviation from the following conditions and consult the manufacturer on the suitability for use under such conditions.

7.1.2 Ambient air temperature

AS-i components shall operate between the ambient temperatures of -5 °C to +40 °C if not otherwise specified, e.g. in conjunction with a specific actuator or sensor type. The operating characteristics shall be maintained over the permissible range of ambient temperatures.

7.1.3 Altitude

Subclause 6.1.2 of EN 60947-1 applies.

7.1.4 Climatic conditions

7.1.4.1 Humidity

AS-i components shall maintain the operating characteristics specified in this standard at a relative humidity (RH) of the air of up to 50 % at 40 °C. Higher relative humidities may occur at lower temperatures, e.g. 90 % at +20 °C.

NOTE Special measures may be necessary if occasional condensation is likely to occur due to variations in temperature.

7.1.4.2 Pollution degree

Unless otherwise stated by the manufacturer, an AS-i component directly connected to or incorporated into an actuator or sensor shall maintain the operating characteristics specified in this standard under environmental conditions of pollution degree 3 as defined in 6.1.3.2 of EN 60947-1.

NOTE Operating capability at other pollution degrees can be necessary, depending upon the micro-environment.

7.2 Conditions during transport and storage

A special agreement shall be made between the user and the manufacturer if the conditions during transport and storage, e.g. temperature and humidity conditions, differ from those defined in 7.1.