

Mechanical standardization of semiconductor devices —

**Part 6-5: General rules for the
preparation of outline drawings of
surface mounted semiconductor device
packages — Design guide for fine-pitch
ball grid array (FBGA)**

The European Standard EN 60191-6-5:2001 has the status of a
British Standard

ICS 31.080.01

National foreword

This British Standard is the official English language version of EN 60191-6-5:2001. It is identical with IEC 60191-6-5:2001.

The UK participation in its preparation was entrusted by Technical Committee EPL/47, Semiconductors, to Subcommittee EPL/47/4, Mechanical standardization, which has the responsibility to:

- aid enquirers to understand the text;
- present to the responsible European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
- monitor related international and European developments and promulgate them in the UK.

A list of organizations represented on this Subcommittee can be obtained on request to its secretary.

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Cross-references

The British Standards which implement international or European publications referred to in this document may be found in the BSI Standards Catalogue under the section entitled “International Standards Correspondence Index”, or by using the “Find” facility of the BSI Standards Electronic Catalogue.

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This British Standard, having been prepared under the direction of the Electrotechnical Sector Policy and Strategy Committee, was published under the authority of the Standards Policy and Strategy Committee on 15 November 2001

Summary of pages

This document comprises a front cover, an inside front cover, the EN title page, pages 2 to 10, an inside back cover and a back cover.

The BSI copyright date displayed in this document indicates when the document was last issued.

Amendments issued since publication

Amd. No.	Date	Comments

© BSI 15 November 2001

ISBN 0 580 38665 1

Mechanical standardization of semiconductor devices
Part 6-5: General rules for the preparation of outline drawings of
surface mounted semiconductor device packages -
Design guide for fine-pitch ball grid array (FBGA)
(IEC 60191-6-5:2001)

Normalisation mécanique des dispositifs
à semiconducteurs
Partie 6-5: Règles générales pour
la préparation des dessins
d'encombrement des dispositifs à
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Guide de conception pour les boîtiers
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(CEI 60191-6-5:2001)

Mechanische Normung von
Halbleiterbauelemente
Teil 6-5: Allgemeine Regeln für
die Erstellung von Gehäusezeichnungen
von SMD-Halbleitergehäusen -
Konstruktionsleitfaden für Feinraster-
Ball-Grid-Arrays (FBGA)
(IEC 60191-6-5:2001)

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 47D/437/FDIS, future edition 1 of IEC 60191-6-5, prepared by SC 47D, Mechanical standardization of semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60191-6-5 on 2001-10-01.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2002-07-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2004-10-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60191-6-5:2001 was approved by CENELEC as a European Standard without any modification.

MECHANICAL STANDARDIZATION OF SEMICONDUCTOR DEVICES –

Part 6-5: General rules for the preparation of outline drawings of surface mounted semiconductor device packages – Design guide for fine-pitch ball grid array (FBGA)

1 Scope

This part of IEC 60191 provides common outline drawings and dimensions for all types of structures and composed materials of fine-pitch ball grid array (hereinafter called FBGA), whose terminal pitch is less than, or equal to, 0,80 mm and whose package body outline is square.

The demand for area array style packages exists according to the multi-functioning and high performance of electrical equipment. The object of this design guide is to standardize outlines and secure interchangeability of FBGA packages. The terminal pitch and package outlines of these fine-pitch array packages are smaller than those of BGA packages.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 60191. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 60191 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60191-6:1990, *Mechanical standardization of semiconductor devices – Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages*

3 Definitions

For the purposes of this part of IEC 60191, the definitions contained in IEC 60191-6 as well as the following definitions apply.

3.1

flanged type

type whose package body size (body length and width) consists of its own flange which is composed around the encapsulation or lid

3.2

type of real chip size

type whose package body size (body length and width) consists of an encapsulation just around the real chip only