

Specification for

Synthetic testing of high-voltage alternating current circuit-breakers

The European Standard EN 60427:1992 has the status of a
British Standard

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Committees responsible for this British Standard

The preparation of this British Standard was entrusted by the Power Electrical Engineering Standards Policy Committee (PEL/-) to Technical Committee PEL/92, upon which the following bodies were represented:

- ASTA Certification Services
- Association of Manufacturers Allied to the Electrical and Electronic Industry (BEAMA Ltd.)
- British Railways Board
- Copper Development Association
- Department of the Environment (Property Services Agency)
- ERA Technology Ltd.
- Electricity Supply Industry in England and Wales
- GAMBICA (BEAMA Ltd.)
- Health and Safety Executive
- Transmission and Distribution Association (BEAMA Ltd.)

The following bodies were also represented in the drafting of the standard, through subcommittees and panels:

- Association of Consulting Engineers
- Association of Supervisory and Executive Engineers
- Electrical Installation Equipment Manufacturers' Association (BEAMA Ltd.)
- Engineering Equipment and Materials Users' Association

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National foreword

This British Standard has been prepared under the direction of the Electrotechnical Sector Board and is the English language version of EN 60427 “*Synthetic testing of high-voltage alternating current circuit-breakers*”, including Amendments A1 and A2, published by the European Committee for Electrotechnical Standardization (CENELEC). It is identical with IEC 427:1989 and its Amendment 1:1992 and Amendment 2:1995, published by the International Electrotechnical Commission (IEC).

As a consequence of implementing the European Standard this British Standard was renumbered as BS EN 60427. Any reference to BS 7441 should be read as a reference to BS EN 60427.

Cross-references

International Standard	Corresponding British Standard
IEC 56	BS 5311:1988 <i>Specification for high-voltage alternating-current circuit-breakers</i> (Identical)

A British Standard does not purport to include all the necessary provisions of a contract. Users of British Standards are responsible for their correct application.

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, pages 2 to 62, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

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English version

Report on synthetic testing of high voltage alternating current circuit-breakers

(includes amendments A1:1993 + A2:1995)

(IEC 427:1989)

Essais synthétiques des disjoncteurs à courant alternatif à haute tension

(inclut les amendements A1:1993 + A2:1995)

(CEI 427:1989)

Synthetische Prüfung von Hochspannungs-Wechselstrom-Leistungsschaltern

(enthält Änderungen A1:1993 + A2:1995)

(IEC 427:1989)

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
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Foreword

As a consequence of the IEC-CENELEC Agreement, HD 580 S1:1990 (IEC 427:1989) was submitted to the CENELEC voting procedure for conversion into a European Standard.

The text of the International Standard was approved by CENELEC as EN 60427 on 1992-06-16.

The following dates were fixed:

- latest date of publication of an identical national standard (dop) 1993-09-01
- latest date of withdrawal of conflicting national standards (dow) 1993-09-01

Annexes designated “normative” are part of the body of the standard. In this standard, Annex ZA is normative.

For products which have complied with HD 580 S1:1990 before 1993-09-01, as shown by the manufacturer or by a certification body, this previous standard may continue to apply for production until 1998-09-01.

Foreword to Amendment A1

The text of document 17A(CO)230, as prepared by Sub-Committee 17A: High-voltage switchgear and controlgear, of IEC Technical Committee No. 17: Switchgear and controlgear, was submitted to the IEC-CENELEC parallel vote in November 1991.

The reference document was approved by CENELEC as amendment A1 to EN 60427:1992 on 9 March 1993.

The following dates were fixed:

- latest date of publication of an identical national standard (dop) 1994-03-01
- latest date of withdrawal of conflicting national standards (dow) 1994-03-01

For products which have complied with EN 60427:1992 before 1994-03-01, as shown by the manufacturer or by a certification body, this previous standard may continue to apply for production until 1999-03-01.

Foreword to Amendment A2

The text of document 17A/435/DIS, future Amendment 2 to IEC 427:1989, prepared by SC 17A, High-voltage switchgear and controlgear, of IEC TC 17, Switchgear and controlgear, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as Amendment A2 to EN 60427:1992 on 1995-07-04

The following dates were fixed:

- latest date by which the amendment has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1996-07-01
- latest date by which the national standards conflicting with the amendment have to be withdrawn (dow) 1996-07-01

Annexes designated “normative” are part of the body of the standard.

In this standard, Annex ZA is normative. Annex ZA has been added by CENELEC.

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1 Introduction

During the past few decades experience has been gained with synthetic testing techniques and methods. It has been proven that synthetic testing is an economical and technically correct way to test high-voltage a.c. circuit-breakers according to the requirements of IEC Publication 56.

This is why it was decided to include synthetic testing methods, after a thorough revision of the first edition of IEC Publication 427, as equivalent to the direct test methods.

2 Scope

This standard applies to a.c. circuit-breakers within the scope of IEC Publication 56 (Clause 1). It provides the general rules for testing a.c. circuit-breakers, for making and breaking capacities over the range of test-duties described in Sub-clauses **6.102** to **6.111** of IEC Publication 56, by synthetic methods.

NOTE Circuits for the test duties described in Sub-clause **6.111** have not yet been standardized. However, present methods are given in Appendix GG.

The methods and techniques described are those in general use. The purpose of this standard is to establish criteria for synthetic testing and for the proper evaluation of results. Such criteria will establish the validity of the test method without imposing restraints on innovation of test circuitry.

3 Normative reference

The following normative document contains provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the edition indicated was valid. All normative documents are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent edition of the normative document indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 1633:1995, *High-voltage alternating current circuit-breakers — Guide for short-circuit and switching test procedures for metal-enclosed and dead tank circuit-breakers*¹⁾.

4 Definitions

The definitions of IEC Publication 56 and the following definitions apply:

4.1

direct test

a test in which the applied voltage, the current and the transient and power-frequency recovery voltages are all obtained from a circuit having a single-power source, which may be a power system or special alternators as used in short-circuit testing stations or a combination of both

4.2

synthetic test

a test in which all of the current, or a major portion of it, is obtained from one source (current circuit), and in which the applied voltage and/or the recovery voltages (transient and power-frequency) are obtained wholly or in part from one or more separate sources (voltage circuits)

4.3

test circuit-breaker

the circuit-breaker under test (see Sub-clause **6.102.2** of IEC Publication 56)

4.4

auxiliary circuit-breaker(s)

the circuit-breaker(s) forming part of a synthetic test circuit used to put the test circuit-breaker into the required relation with various circuits

¹⁾ The IEC 1633 is a technical report of type 2.

4.5

current circuit

that part of the synthetic test circuit from which all or the major part of the power-frequency current is obtained

4.6

voltage circuit

that part of the synthetic test circuit from which all or the major part of the test voltage is obtained

4.7

prospective current (of a circuit and with respect to a circuit-breaker) (IEV 441-17-01 modified)

the current that would flow in the circuit if each pole of the test and auxiliary circuit-breakers were replaced by a conductor of negligible impedance

4.8

actual current

the current through the test circuit-breaker (prospective current modified by the arc-voltage of the test and auxiliary circuit-breakers)

4.9

distortion current

a calculated current equal to the difference between the prospective current and the actual current

4.10

post-arc current

the current which flows through the arc-gap of a circuit-breaker immediately after the current and arc-voltage have fallen to zero and the transient recovery voltage has begun to rise

4.11

current-injection method

a synthetic test method in which the voltage circuit is applied to the test circuit-breaker before power-frequency current-zero

4.12

injected current

the current supplied by the voltage circuit of a current injection circuit when it is connected to the circuit-breaker under test

4.13

voltage-injection method

a synthetic test method in which the voltage circuit is applied to the test circuit-breaker after power-frequency current-zero

4.14

reference system conditions

the conditions of an electrical system having the parameters from which the rated and test values of IEC Publication 56 are derived

Section 1. Synthetic testing techniques and methods

5 Short-circuit breaking tests

5.1 Basic principles and general requirements for synthetic breaking test methods

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally, the adequacy is established when the test method meets the requirements set forth in the following sub-clauses.

Basic intervals

A circuit-breaker has two basic positions: closed and open. In the closed position a circuit-breaker conducts full current with negligible voltage drop across its contacts. In the open position it conducts negligible current but with full voltage across the contacts. This defines the two main stresses, the current stress and the voltage stress, which are separated in time.

If closer attention is paid to the voltage and current stresses during the interrupting process (Figure 1), three main intervals can be recognized:

- High-current interval

The high-current interval is the time from contact separation to the start of the significant change in arc-voltage. The high-current interval precedes the interaction and high-voltage intervals.

- Interaction interval

The interaction interval is the time from the start of the significant change in arc-voltage prior to current-zero to the time when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker. (See also Appendix **BB.2**).

- High-voltage interval

The high-voltage interval is the time from the moment when the current including the post-arc current, if any, ceases to flow through the test circuit-breaker to the end of the test.

5.1.1 High-current interval

During this interval the test circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the interaction interval, within tolerances to be specified, are the same as under reference system conditions.

In synthetic test circuits the ratio of the power-frequency voltage of the current circuit to the arc-voltage is low in comparison with tests at reference system conditions due to:

- the voltage of the current circuit being a fraction of the system voltage;
- the fact that the arc-voltages of the test circuit-breaker and of the auxiliary circuit-breaker are added.

As a result the duration of the current loop and the peak value of the current will be reduced. This distortion of the current is outlined in Appendix AA.

Considerations with respect to the arc-energy released in the test circuit-breaker lead to a maximum permissible influence in terms of tolerances on two characteristic values of the shape of the current, i.e. current-peak value and current-loop duration (see Appendix AA).

The tolerance on the amplitude and the power frequency of the prospective breaking current, as given in Sub-clauses **6.103.2** and **6.104.3** of IEC Publication 56, shall not be exceeded by the actual current through the test circuit-breaker. Therefore the following conditions shall be met:

- the actual current amplitude during the last loop in the test circuit-breaker shall comply with the requirements for the prospective current stated in Sub-clause **6.104.3** of IEC Publication 56. The amplitude of the final loop of the actual test current in a single phase circuit shall be not less than 90 % of the value specified;
- the duration of the final loop of the actual power-frequency test current shall be not less than 90 % of the loop duration given by the rated frequency after taking into account, where this is appropriate, the effect of the specified d.c. component;
- when performing synthetic tests on circuit-breakers possessing arc-voltage characteristics which would significantly modify the current in service, the influence of the arc-voltage on the current amplitude and loop duration may be allowed for when considering the tolerances given above.

The detailed procedure for estimating these corrections with examples for establishing the tolerances is given in Appendix AA.

To keep within the tolerances for the test current, it is acceptable to increase the current by increasing the voltage or reducing the reactance of the current circuit, or to apply a current with an increased d.c. component or a reduced power frequency. For this purpose the specified tolerances for d.c. component and power frequency may be exceeded subject to the consent of the manufacturer.

5.1.2 Interaction interval

During the interaction interval, the short-circuit current stress changes into high-voltage stress and the circuit-breaker performance can significantly influence the current and voltages in the circuit. As the current decreases to zero, the arc voltage may rise to charge parallel capacitance and distort current passing through the arc. After the current-zero the post-arc conductivity may result in additional damping of the transient recovery voltage and thus influence the voltage across the circuit-breaker and the energy supplied to the ionised contact gap. The interaction between the circuit and the circuit-breaker immediately before and after current-zero (i.e. during the interaction interval) is of extreme importance to the interrupting process.

During the interaction interval the current and voltage wave forms shall be the same for a synthetic test as under reference system conditions (Sub-clause 4.14), taking into account the possible deviations of the current and voltage from the prospective values due to the interaction between the circuit-breaker and the circuit.

The interaction interval presents the critical time for the thermal failure mode of the circuit-breaker. Therefore, it is of extreme importance that the shape and magnitude of the prospective transient recovery voltage (TRV) corresponds to that associated with the prospective current of the relevant test-duty.

The above implies strict requirements for the test circuit. The requirements are given for the current injection method in Sub-clause 5.2.1 and for the voltage injection method in Sub-clause 5.2.2.

NOTE Depending on the test circuit used, the interaction between circuit and test circuit-breaker may be disturbed by the behaviour of the auxiliary circuit-breaker during the critical interval around current-zero.

The arc-voltage of the auxiliary circuit-breaker should be less than or equal to the arc-voltage of the test circuit-breaker.

If an auxiliary circuit-breaker with a higher arc-voltage is used, a higher power-frequency voltage of the current circuit may be necessary.

5.1.3 High-voltage interval

During the high-voltage interval the gap of the test circuit-breaker is stressed by the recovery voltage.

The prospective TRV shall comply with the requirements of Sub-clauses 4.102, 4.105, 4.106 and 6.104.5 of IEC Publication 56. Suitable methods for determining the prospective TRV in synthetic test circuits can be selected from Appendix GG of IEC Publication 56.

The impedance of the voltage circuit shall be low enough to give clear evidence of breakdown, if any.

NOTE 1 If the test circuit-breaker is fitted with low ohmic parallel resistors, a special procedure may be necessary (see Appendix FF).

NOTE 2 If the TRV is obtained from more than one source the overall wave shape should not show any appreciable discontinuity.

In principle, the power-frequency recovery voltage for the basic short-circuit test-duties shall equate with the requirements of Sub-clause 6.104.7 of IEC Publication 56. In synthetic testing the recovery voltage is supplied from the voltage circuit, either directly or in series with the current circuit. This gives a d.c. voltage, or a combined a.c. and d.c. voltage, or an a.c. voltage, which in most cases decays due to the limited energy of the voltage source. It may thus not be possible to maintain the recovery voltage for at least 0,1 s as specified in Sub-clause 6.104.7 of IEC Publication 56. Deviations from the specified recovery voltage are acceptable if the following conditions are met:

- The instantaneous value of the recovery voltage during a period equal to 1/8 of a cycle of the rated frequency of the circuit-breaker shall be not less than the equivalent instantaneous value of the power-frequency recovery voltage specified in Sub-clause 6.104.7 of IEC Publication 56 which starts with a minimum peak value of $0,95 h\sqrt{2} U/\sqrt{3}$.

h = first pole-to-clear factor (1,3 or 1,5).

U = rated voltage of the circuit-breaker.

- Whether an exponentially decaying d.c., an a.c. or a combined a.c. and d.c. recovery voltage is used, its instantaneous value (for d.c.) or its peak value (or a.c. or combined a.c. and d.c.) should in principle be kept as close as possible to $\sqrt{2} U/\sqrt{3}$ and in any case must not fall below $0,5\sqrt{2} U/\sqrt{3}$ in less than 0,1 s (see Figure 2).

- If an exponentially decaying d.c. or a combined a.c. and d.c. recovery voltage imposes an inappropriate stress on the circuit-breaker compared to that due to the specified a.c. recovery voltage in reference system conditions, then a more appropriate circuit may be used taking into account Sub-clause 6.104.7 of IEC Publication 56 and also the limits stated above.

5.2 Synthetic test circuits and related specific requirements for breaking tests

5.2.1 Current injection methods

These methods can be described in terms of general principles as follows (see Appendix BB):

- the current from the voltage source is superimposed on the current in the test circuit-breaker prior to the interaction interval;
- an auxiliary circuit-breaker interrupts the current from the current circuit prior to the interaction interval.

During the interaction interval the test circuit-breaker is exposed to the voltage of the voltage circuit having an impedance which is representative of the reference system conditions. This explains the validity of current injection methods. Several current injection methods are known but only the conditions for parallel current injection are given below since this method is used by the majority of the test laboratories. The following conditions shall be met:

a) TRV wave-shaping circuit

- 1) The shape and magnitude of the prospective TRV shall comply with the specified values.
- 2) Ideally the equivalent surge impedance Z_h (see Figure 3) shall be equal to $(du/dt)/(di/dt)$ during the interaction interval, du/dt is the rate of rise of the specified transient recovery voltage and di/dt is the rate of decrease of the specified short-circuit current.
- 3) The combination of the stray and lumped capacitance C_{dh} in parallel with Z_h gives rise to the delay time $t_d = Z_h C_{dh}$.

b) Inductance of the voltage circuit

The value of the inductance of the voltage circuit shall be between 1,0 and 1,5 times the inductance derived from the equivalent power-frequency voltage divided by the prospective current.

c) Frequency of the injected current and the injection timing

The frequency of the injected current shall preferably be of the order of 500 Hz with a lower limit of 250 Hz and an upper limit of 1 000 Hz.

The initiation of the injected current shall be adjusted such that the time, during which the test circuit-breaker is fed only by the injected current, is not more than a quarter of the period of the injected current frequency with a maximum of 500 μ s.

In order to prevent undue influence on the wave shape of the power-frequency current, the lower limit of the frequency of the injected current is 250 Hz.

The maximum frequency of the injected current is determined by the interval of significant change of arc-voltage, which interval shall be smaller than the time for which the arc is fed only by the injected current. To achieve this, the period of the injected frequency should be at least four times the interval of significant change of arc-voltage (see Appendix BB).

NOTE Attention should be paid to the possible overstressing of the circuit-breaker if the time that the test circuit-breaker is fed by the injected current only is less than 200 μ s.

d) Waveshape of the injected current

The prospective rate of decrease (di/dt) of the injected current shall correspond to that of the prospective power-frequency current.

The injected current shall be practically free of superimposed oscillations for a time not less than 100 μ s before current-zero.

5.2.2 Voltage injection method

Several voltage injection methods are known but only series voltage injection is described here in general terms as follows (see also Appendix CC):

- The voltage from the voltage circuit is applied to the test circuit-breaker after the interaction interval.
- An auxiliary circuit-breaker with a parallel capacitor is used to apply the recovery voltage to the test circuit-breaker.
- During the high-current and interaction intervals the test circuit-breaker is exposed to the current circuit only.

If the voltage injection method is to be used to check the thermal behaviour of the circuit-breaker, i.e. to test under terminal fault conditions with initial transient recovery voltage (ITRV) stress or under short-line-fault conditions, it is necessary to demonstrate the validity of the test circuit for the interaction interval. This is subject to agreement between manufacturer, testing station and user.

When used for tests relating to the dielectric behaviour of the circuit-breaker, the following conditions shall be met:

- the auxiliary circuit-breaker should have an arc-voltage less than or equal to that of the test circuit-breaker. This condition is met if the extinction peaks of both circuit-breakers are approximately the same (see note in Sub-clause 5.1.2);
- the impedance of the voltage circuit shall be low enough to provide for reignitions or restrikes if they occur.

Therefore, the capacitance across the auxiliary circuit-breaker shall be at least 10 nF. Care should be taken to avoid undue distortion of the current before power-frequency current-zero;

- no pause shall be introduced by the combining of the current circuit and the voltage circuit.

NOTE For short-line fault tests, in addition to the voltage injection circuit supplying the source side TRV, a current injection circuit which is connected to the line-side terminal of the test circuit-breaker can be used to supply the line-side transient voltage.

5.2.3 Duplicate circuit method (transformer or Skeats circuit)

This method can be described in terms of general principles as follows (see also Appendix DD):

- the current and voltage are supplied from the same source;
- the a.c. recovery voltage is supplied from a step-up transformer the primary of which is connected to the current circuit;
- the recovery voltage is applied to the test circuit-breaker through an impedance (normally a resistance).

The auxiliary circuit-breaker interrupts the current prior to the test circuit-breaker by a short time interval (usually about 10 μ s). During this short interval the value of di/dt of the current in the test circuit-breaker is decreased.

The test circuit is therefore not valid for tests where attention is paid to the thermal failure mode of the test circuit-breaker.

The test circuit is suitable for testing the dielectric behaviour of a circuit-breaker.

The test circuit can be used for making tests.

The test circuit can easily be adapted to supply full voltage stresses in two (or more) operations e.g. at both closing and opening in a CO operation, at both openings in an O – t – CO operation or even at consecutive current-zeros in an opening operation. See Appendix DD.

5.2.4 Other synthetic test methods

Other methods may prove correct and advantageous for testing of circuit-breakers with specific characteristics or for testing of a circuit-breaker for specific performance. Even though these methods are not covered by this standard, they can be used subject to understanding of their application and agreement between the manufacturer and the user.

Synthetic methods for three-phase short-circuit breaking tests are reported in IEC 1633.

A method available for testing circuit-breakers having parallel resistors is reported in Appendix FF — Special procedures for testing circuit-breakers having parallel breaking resistors.

6 Short-circuit making tests

6.1 Basic principles and general requirements for synthetic making test methods

During a closing operation onto a short-circuit, the circuit-breaker contact gap is subjected to the applied voltage corresponding to the r.m.s. value of the rated voltage divided by $\sqrt{3}$ which causes its breakdown. After this moment, the circuit-breaker is subjected to the making current which is expressed by its maximum amplitude $\hat{i}$ in Figure 4 (see Sub-clause 4.103 of IEC Publication 56).

In a synthetic test circuit the applied voltage is supplied by a separate voltage source and the short-circuit current is supplied by a reduced voltage current circuit. This latter is connected to the circuit-breaker immediately after breakdown of the contact gap by means of a fast making device, e.g. a triggered spark gap.

Any particular synthetic method chosen for testing shall adequately stress the test circuit-breaker. Generally the adequacy is established when the test method meets the requirements set forth in the following sub-clauses.

Basic intervals

Prior to making, a circuit-breaker withstands the rated phase-to-earth voltage applied across its terminals: during making, it carries the rated short-circuit current. If closer attention is paid to the voltage and current stresses during the making test — Figure 4 — three main intervals can be recognised:

— High-voltage interval

The high-voltage interval is the time from the commencement of the test, with the circuit-breaker in the open position, to the moment of breakdown across the contact gap.

— Pre-arcing interval

The pre-arcing interval is the time, during the closing stroke of the circuit-breaker, from the moment of breakdown across the contact gap to the touching of the contacts.

— Latching interval

The latching interval is the time, during the closing stroke of the circuit-breaker, from the touching of the contacts to the moment when the contacts reach the fully closed (latched) position.

6.1.1 High-voltage interval

During this interval the circuit-breaker shall be stressed by the test circuit in such a way that the starting conditions for the pre-arcing interval, within the tolerances to be specified, are the same as under reference system conditions.

Therefore the following conditions shall be met:

— The applied voltage shall comply with the requirement set forth in Sub-clause **6.104.1** of IEC Publication 56.

— The phase relationship between the applied voltage and the short-circuit current shall correspond to the rated power factor of the test circuit within the tolerances given in Sub-clause **6.103.1** of IEC Publication 56.

However, when performing synthetic tests on circuit-breakers having a high closing speed and consequently a short pre-arcing time a reduced applied voltage can be used provided that the maximum pre-arcing time determined in accordance with Sub-clause **6.3** does not exceed $1/\omega$ s (3.2 ms for 50 Hz and 2.7 ms for 60 Hz) as shown in Figure 5.

6.1.2 Pre-arcing interval

During pre-arcing the circuit-breaker is subjected to electrodynamic forces due to the current and to deteriorating effects due to arc-energy. In general the current is composed of three components:

- the initial transient making current, ITMC,
- the d.c. and a.c. components of the short-circuit current.

Two typical cases may occur depending on the moment of closing and on the circuit-breaker design:

- Breakdown occurs near the crest of the applied voltage; an almost symmetrical current is established. Pre-arc energy and ITMC are relatively high.
- Breakdown occurs near zero of the applied voltage; an asymmetrical current is established. Pre-arc energy and ITMC are negligible with the exception of the case of non-simultaneous closing in a multi-unit pole.

NOTE The ITMC is not defined in Sub-clause **4.103** of IEC Publication 56; a value sufficient to maintain pre-arcing is adequate.

6.1.3 Latching interval and fully closed position

During these intervals the circuit-breaker has to close in presence of the electrodynamic forces due to the current and contact friction forces. Therefore during these intervals the making current shall comply with Sub-clause **4.103** of IEC Publication 56.

6.2 Synthetic test circuit and related specific requirements for making tests

6.2.1 Test circuit

The test circuit is made up with two sources namely the current and the voltage circuit as shown in Figure 6.

- The voltage circuit, which mainly consists of a low power transformer, supplies:
 - the applied voltage during the high-voltage interval;
 - the ITMC during the pre-arcing interval, by the discharge of the ITMC-circuit.
- The current circuit supplies the making current during the pre-arcing, and latching intervals.

6.2.2 Specific requirements

During a synthetic making test the phase relationship between the applied test voltage and the short-circuit current depends on the following parameters:

- phase displacement between the current source voltage u_1 and the voltage source voltage u_2 ;
- delay time of making gap;
- minimum sparkover voltage of making gap.

The phase displacement between the applied voltage and the short-circuit current shall be 90 ± 27 electrical degrees.

The injected current supplied by the voltage circuit ensures pre-arcing before the closing of the fast make gap. Therefore the time constant of ITMC-circuit shall be longer than the make gap delay time.

NOTE The voltage source u_2 may be an a.c. or a d.c. source.

6.3 Evaluation of the maximum pre-arcing time

To determine whether a reduced applied voltage can be used for the making test, the maximum pre-arcing time of the circuit-breaker has to be established. (See Sub-clause 5.1.1). This maximum pre-arcing time shall be determined by preliminary direct tests carried out at full voltage and at the maximum short-circuit current available. To ensure this, pre-arcing should commence at the peak of the voltage wave. The current should ensure decisive breakdown during the pre-strike.

During rated operating sequences making operations are preceded by breaking operations, e.g. O – t – CO – t' – CO or CO – t'' – CO.

Therefore the following tests shall be carried out:

O – t – CO – t' – CO with:

t = 3 min for circuit-breakers not intended for rapid auto-reclosing

t = 0,3 s for circuit-breakers intended for rapid auto-reclosing

t' = 3 min.

or CO – t'' – CO with:

t'' = 15 s.

Section 2. Specific requirements for synthetic tests for making and breaking performance related to the requirements of sub-clauses 6.102 to 6.111 inclusive of IEC Publication 56

Sub-clauses 6.102 to 6.111 inclusive of IEC Publication 56 are also applicable for synthetic testing. However, in some cases special techniques are necessary. These cases are mentioned in the sub-clauses of this section. The numbering of the sub-clauses corresponds to that of IEC Publication 56.

7.102.1.3 Multi-part testing

For synthetic methods for the testing of circuit-breakers fitted with low-ohmic parallel resistors see Appendix FF.

7.102.2 Arrangement of circuit-breaker for tests

| For synthetic methods for three-phase testing refer to IEC 1633.

7.102.9 *Circuit-breakers with short arcing times*

In order to be able to perform synthetic tests on the same basis as direct tests, normally it will be necessary to apply special reignition methods to prolong the arcing of the test circuit-breaker through the necessary number of zeros of the power-frequency current. See Appendix JJ for reignition methods to prolong arcing.

NOTE A method with multiple application of the voltage source involves practically the same procedure as for direct testing. The voltage source is connected to the test circuit-breaker at each current-zero. If the test circuit-breaker clears at a zero, the procedure is stopped. If the test circuit-breaker reignites, then the current source is reconnected by reigniting the auxiliary breaker. At the same time, the voltage source will be disconnected and then reconnected at the next current-zero, with its polarity reversed appropriately. However, such a procedure is rarely used, because of its complexity.

The “step-by-step” method is the method used on most synthetic tests. The method is considered to be a sufficiently close approximation of the direct testing procedure.

The arcing is prolonged by means of thermal reignitions. As this method makes it possible to force the test circuit-breaker to reignite in all conditions, special care shall be taken not to reignite the circuit-breaker at the instant of a current-zero when the circuit-breaker can clear. For this purpose it is necessary to determine, for each terminal fault, short-line fault and out-of-phase test duty, the minimum arcing time of the circuit-breaker. At least two breaking tests, one clearance and one reignition, are necessary for this determination. The arcing time difference between these two tests is limited to about 1 ms.

The clearance at the minimum arcing time is the first valid breaking operation.

The other test is also performed to demonstrate that a reignition at an early current zero, for example with an arcing time just below the minimum arcing time, as during a breaking operation at maximum arcing time, would take place between the arcing contacts.

NOTE 1 The extra tests necessary to demonstrate correct behaviour at early current zeros will usually contribute insignificantly to contact wear etc., due to the short arcing times. Therefore, no reconditioning should be necessary because of these tests.

NOTE 2 The reignition(s) obtained when determining the minimum arcing time do(es) not indicate a fault of the circuit-breaker. However, it is important to establish that this reignition has taken place between the arcing contacts only. This may demonstrate the voltage withstand co-ordination at dielectric reignition, at least for the actual contact position. When using a current injection method the interruption of the injected current a few loops after the reignition is often a useful means for the judgement. Thorough inspection of screens, arcing and main contacts, etc., should also be made to verify correct behaviour.

For short-line-fault tests the reignition will usually be due to thermal failure, so that the voltage withstand co-ordination will not be involved.

NOTE 3 Although this subclause refers to circuit-breakers with short arcing times, the same requirements are in principle valid for circuit-breakers with longer arcing times.

7.106 Basic short-circuit test-duties

The operating sequences for test-duties Nos. 1, 2, 3 and 5 together with the various methods of carrying out test-duty No. 4 are shown in Table I.

Symbols: C_S = Making operation with specified parameters in a synthetic circuit.

O_S = Breaking operation with specified parameters in a synthetic circuit.

C_D = Making operation with reduced applied voltage of the current source only and the specified making current.

O_D = Breaking operation with reduced transient and power-frequency recovery voltages of the current source only and with the specified breaking current.

NOTE 1 Due to the characteristics of synthetic testing it may be difficult to comply with the specified time intervals of the rated operating sequence. See Sub-clause 6.105.1 of IEC Publication 56.

NOTE 2 In order to comply with all test requirements it may be necessary to make more operations than provided for in the rated operating sequence. In such cases the circuit-breaker may be reconditioned after the number of operations provided for in the rated operating sequence.

7.106.1

7.106.2 *Test-duties Nos. 1, 2 and 3*

7.106.3

For test-duties Nos. 1, 2, and 3, only breaking tests are specified.

7.106.4 *Test-duty No. 4*

Procedures are known to carry out the rated operating sequence synthetically with the specified parameters (see Table I).

If, due to limitations of the testing station, it is not possible to apply these procedures, the following methods are available:

Method 1

The first breaking operation before the time interval $t = 0,3$ s or $t'' = 15$ s may be carried out as an O_D -operation.

The purpose of the additional single breaking test O_s is:

- to comply with the requirement to have two or three breaking operations at specified values,
- to provide the necessary information for the relevant requirements for the setting of the control of the tripping impulse during the subsequent operating sequence.

The conditions of this two-part test are:

- the breaking operation O_D shall be performed under the same arcing time conditions as if direct tests were performed at specified values. Normally, reignition methods (see Appendix JJ) are necessary to achieve this;
- the control of the tripping impulse for the breaking operations of the operating sequence shall be in accordance with the requirements of Sub-clause 6.102.9 B)1) of IEC Publication 56;
- the setting of the control of the tripping impulse for the single breaking operation O_s shall be such, that the arcing time is the same as for the O_D operation. It may be necessary to make more than one test to realise this.

Methods 2a and 2b

The making and breaking tests may be made separately as test-duties Nos. 4a and 4b according to Sub-clauses 6.106.4.1 and 6.106.4.2 of IEC Publication 56.

If it is impossible to carry out method 2a for circuit-breakers with time intervals $t = 0,3$ s or $t'' = 15$ s, method 2b can be applied with the first breaking operation O_D and arcing time conditions as specified for method 1.

Closing operations at values of applied voltage lower than those given in Sub-clause 6.104.1 of IEC Publication 56 are only allowed if the requirements of Sub-clause 5.1.1 are fulfilled.

Methods 3a and 3b

If it is not possible to carry out methods 2a or 2b with making operations at the specified applied voltage, it is under certain conditions permissible (see Sub-clause 5.1.1) to use method 3a.

If it is impossible to carry out method 3a for circuit-breakers with time intervals $t = 0,3$ s or $t'' = 15$ s, method 3b can be used with the first breaking operation O_D and arcing time conditions as specified for method 1.

7.106.5 Test-duty No. 5

On circuit-breakers having short arcing times three breaking operations shall be made irrespective of the rated operating sequence.

During tests with asymmetrical current both di/dt and the TRV are modified due to the d.c. component. In synthetic tests these modifications have to be pre-arranged by:

- a) Control of the d.c. component of the current

The d.c. component may be controlled by selection of the point on the wave at which the short-circuit is initiated

- b) Reduction of di/dt at current-zero

The reduction of di/dt may for current injection methods be obtained by reducing the charging voltage of the voltage circuit.

The formula to be applied for the determination of the reduced charging voltage is:

$$U_{HA} = U_{HS} \left[\sqrt{1 - p^2} \pm \frac{p}{2\pi f \cdot \tau} \right] \quad \begin{array}{l} + \text{ for major loop} \\ - \text{ for minor loop} \end{array}$$

where:

U_{HA} = reduced charging voltage at asymmetrical test

U_{HS} = charging voltage for equivalent symmetrical test

p = the per unit value of the d.c. component at current zero

τ = time constant according to IEC Publication 56 (45 ms).

p can be calculated from the asymmetry at contact separation p_{cs} :

$$p = p_{cs} \cdot e^{-\frac{t_a}{\tau}}$$

where:

t_a = arcing time

c) Correction of TRV

1) Simplified method

For TRV's with time t_2 not exceeding 500 μ s, a simplified method can be used. This method is based upon the supposition that the correction of TRV (u_1, t_1, u_c, t_2) is proportional, to the correction for di/dt .

This means that the correction of TRV is automatically covered by the reduced di/dt according to b).

2) For TRV's with time t_2 exceeding 500 μ s other corrections and/or circuit modifications have to be used. The required prospective TRV values are given in Table II.

NOTE Table III, Table IV and Table V give information with respect to TRV values for a first-pole-to-clear factor of 1.5 and/or a time constant of 120 ms. These values are not IEC Publication 56 ratings. TRV values for time constants other than those given in the tables may be obtained with sufficient accuracy by linear inter and extrapolation.

d) Correction of recovery voltage

When a test is made for clearance at the end of a major loop the d.c. form of the reduced recovery voltage will adequately cover the first quarter loop of the recovery voltage (of an equivalent direct test).

For clearance at the end of a minor loop of current the d.c. form of the reduced recovery voltage will not cover reference system conditions since in the system the power-frequency recovery voltage continues to rise after the onset of the TRV.

Subject to agreement between testing station, manufacturer and user it may be considered that taken together with the symmetrical test-duties the evidence is sufficient to prove the performance of the circuit-breaker. An asymmetrical test with clearance after a minor loop with reduced di/dt and the resulting reduced TRV is assumed to be less severe than an equivalent symmetrical test. However, if it is required to prove fully this test condition, there are three possibilities:

- 1) the test is performed with asymmetrical current conditions with the voltage source charged as for the symmetrical test. It must be recognised that this represents a considerable increase in severity above that of an equivalent direct test since both di/dt and the TRV are higher;
- 2) the test is performed as under 1) except that the inductance of the injection circuit is increased in inverse proportion to di/dt . In this case, the di/dt value is correct but the TRV higher;
- 3) the test is performed with an a.c. recovery voltage.

7.109 Short-line fault tests

For short-line fault synthetic testing the parameters of the short-line circuit shall be those given in IEC Publication 56 and the line circuit shall be in the current carrying circuit during the whole interaction interval.

With current injection circuits the short-line circuit may be connected in series with the voltage circuit, its inductance becoming part of L_h e.g. as shown in Figure BB.1.

The presence of the short-line fault circuit in the voltage circuit may cause oscillations to be superimposed on the injected current wave. These oscillations should be damped out (to satisfy the requirements of Sub-clause 4.2.1 d), so as not to affect the current during the interval of significant change of arc-voltage or at least 100 μ s before current-zero.

A resistance may be connected in series with the TRV shaping circuit. In most cases this resistance, selected to control the initial rate of rise of recovery voltage, is sufficient to supply the necessary damping.

NOTE If, for short line fault tests, the line is connected to the same side of the test circuit-breaker as the voltage circuit impedance, special attention should be given to voltage distribution and measurement of prospective TRV.

7.111 Synthetic methods for capacitive-current switching

See Appendix GG.

Table I — Synthetic test sequences for test-duties 1, 2, 3, 4 and 5

Test-duty No.	Synthetic test		Rated operating sequence	
			$O - t - CO - t' - CO$ $t = 0,3 \text{ s or } 3 \text{ min}$ $t' = 3 \text{ min}$	$CO - t'' - CO$ $t'' = 15 \text{ s}$
1, 2, 3	Breaking operations ^a	a)	$O_S - t - O_S - t' - O_S$	$O_S - t'' - O_S$
		b)	O_S $O_D - t - O_S - t' - O_S$	O_S $O_D - t'' - O_S$
4	Complete rated operating sequence		$O_S - t - C_S O_S - t' - C_S O_S$	$C_S O_S - t'' - C_S O_S$
	Method 1		O_S $O_D - t - C_S O_S - t' - C_S O_S$	$C_S O_S$ $C_S O_D - t'' - C_S O_S$
	Method 2	a)	$C_S - t' - C_S$ $O_S - t - C_D O_S - t' - C_D O_S$	$C_S - t'' - C_S$ $C_D O_S - t'' - C_D O_S$
		b)	$C_S - t' - C_S$ O_S $O_D - t - C_D O_S - t' - C_D O_S$	$C_S - t'' - C_S$ $C_D O_S$ $C_D O_D - t'' - C_D O_S$
	Method 3	a)	$O_S - t - C_D O_S - t' - C_D O_S$	$C_D O_S - t'' - C_D O_S$
		b)	O_S $O_D - t - C_D O_S - t' - C_D O_S$	$C_D O_S$ $C_D O_D - t'' - C_D O_S$
	5	Breaking operations ^a b		O_S O_S O_S

^a For convenience in testing, it is permissible to introduce a closing operation before any opening operation in test-duties Nos. 1, 2, 3, and 5.
^b For short arcing times only.

Table II — TRV after breaking asymmetrical current

Frequency (Hz)		50												60											
Voltage (kV)		245		300		362		420		525		765		245		300		362		420		525		765	
Time co-ordinate (µs)		t_1 130	t_2 390	t_1 159	t_2 477	t_1 192	t_2 576	t_1 223	t_2 669	t_1 279	t_2 837	t_1 406	t_2 1 218	t_1 130	t_2 390	t_1 159	t_2 477	t_1 192	t_2 576	t_1 223	t_2 669	t_1 279	t_2 837	t_1 406	t_2 1 218
	%	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c	u_1	u_c
		Voltage (kV)																							
After major-loop: asymmetry at current zero	0	260	364	318	446	384	538	446	624	557	780	812	1 137	260	364	318	446	384	538	446	624	557	780	812	1 137
	5	260	363	319	445	385	536	446	621	557	775	811	1 124	260	363	319	444	384	535	445	620	557	773	810	1 121
	10	260	362	318	442	384	532	445	616	556	768	808	1 109	260	361	318	441	383	530	444	614	555	764	806	1 102
	15	259	359	317	439	382	527	443	610	553	758	804	1 091	258	358	316	436	381	525	442	606	551	753	801	1 080
	20	257	356	315	434	380	521	440	602	549	747	797	1 070	257	354	314	431	378	517	438	597	547	740	793	1 055
	25	255	351	312	428	376	514	436	593	543	734	788	1 046	254	349	311	424	374	509	434	586	540	724	783	1 027
	30	252	346	308	421	371	504	430	581	536	718	776	1 019	251	343	307	417	369	498	428	574	533	707	770	996
	35	248	339	303	412	365	494	423	568	527	701	763	988	247	336	302	407	363	487	420	560	523	688	756	962
	40	244	332	298	403	358	481	415	553	517	681	746	954	242	327	296	397	356	473	412	543	512	666	738	925
	45	238	323	291	391	350	467	405	536	504	658	728	916	236	318	289	385	347	458	401	525	499	641	719	883
	50	232	313	283	379	341	451	394	517	490	633	706	875	230	308	280	371	337	441	390	505	484	614	696	838
	55	224	301	274	364	329	433	381	496	474	604	681	829	222	296	271	356	326	422	376	482	467	584	670	788
	60	216	288	263	348	317	413	366	471	455	572	653	778	213	282	260	339	313	401	361	456	448	550	641	733
	65	206	273	251	329	302	390	349	444	433	537	621	721	203	267	248	320	298	377	344	428	426	512	608	673
	70	195	256	238	308	285	364	329	413	408	497	584	658	192	249	234	298	280	350	324	395	400	471	570	607
	75	182	237	222	284	266	334	307	378	380	451	541	587	179	229	218	273	261	319	300	359	371	423	526	532
	80	166	214	203	256	243	299	280	337	346	399	492	506	163	206	198	244	237	284	273	317	337	369	476	447
After minor-loop: asymmetric at current zero	0	260	364	318	446	384	538	446	624	557	780	812	1 137	260	364	318	446	384	538	446	624	557	780	812	1 137
	5	259	364	317	446	383	539	444	626	556	783	811	1 146	259	364	318	447	383	540	445	627	556	785	812	1 150
	10	257	363	315	445	381	538	442	626	553	785	807	1 153	258	364	316	446	381	540	443	628	554	789	809	1 160
	15	255	361	313	443	378	536	438	624	549	784	802	1 157	256	362	313	445	379	539	440	628	550	790	805	1 168
	20	252	358	309	440	373	533	434	621	543	782	795	1 158	253	360	310	443	375	537	435	626	545	789	798	1 172
	25	249	354	305	435	368	528	428	616	536	777	785	1 156	250	356	306	439	370	533	430	622	539	786	790	1 174
	30	244	349	299	430	362	522	421	609	527	770	773	1 150	245	352	301	434	364	528	423	617	531	781	779	1 172
	35	239	343	293	423	355	514	412	601	517	761	759	1 142	240	346	295	428	357	521	415	610	521	774	766	1 168
	40	233	336	286	414	346	505	402	591	505	750	742	1 130	235	340	288	420	349	513	406	601	509	764	750	1 159
	45	226	327	278	405	336	494	391	578	491	736	723	1 114	228	332	280	411	339	502	395	590	496	752	732	1 147
	50	219	318	269	393	325	481	378	564	475	719	700	1 094	221	323	271	401	328	490	382	576	481	737	710	1 131
	55	210	307	258	380	312	465	364	547	457	699	675	1 070	212	313	261	388	316	476	368	561	463	720	686	1 111
	60	200	294	246	365	298	448	347	527	437	676	646	1 041	203	301	249	374	302	460	352	542	444	698	658	1 085
	65	189	280	233	348	282	428	328	504	414	649	613	1 007	192	287	236	358	286	441	334	521	421	673	626	1 055
	70	177	264	217	329	264	405	307	478	387	618	576	966	179	271	221	339	268	418	313	496	395	644	590	1 017
	75	162	245	200	306	243	378	283	448	357	581	533	917	165	252	204	317	248	393	289	467	366	609	548	972
	80	146	223	179	279	218	346	255	412	322	537	483	858	149	231	184	291	224	362	261	432	332	567	499	917

First pole to clear factor 1,3

Time constant of d.c. decrement 45 ms