

Semiconductor devices —

Part 16-10: Technology Approval Schedule (TAS) for monolithic microwave integrated circuits

The European Standard EN 60747-16-10:2004 has the status of a
British Standard

ICS 31.200

National foreword

This British Standard is the official English language version of EN 60747-16-10:2004. It is identical with IEC 60747-16-10:2004.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors, which has the responsibility to:

- aid enquirers to understand the text;
- present to the responsible international/European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
- monitor related international and European developments and promulgate them in the UK.

A list of organizations represented on this committee can be obtained on request to its secretary.

Cross-references

The British Standards which implement international or European publications referred to in this document may be found in the *BSI Catalogue* under the section entitled “International Standards Correspondence Index”, or by using the “Search” facility of the *BSI Electronic Catalogue* or of British Standards Online.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 9 November 2004

Summary of pages

This document comprises a front cover, an inside front cover, the EN title page, pages 2 to 54, an inside back cover and a back cover.

The BSI copyright notice displayed in this document indicates when the document was last issued.

Amendments issued since publication

Amd. No.	Date	Comments

© BSI 9 November 2004

ISBN 0 580 44731 6

Semiconductor devices
Part 16-10: Technology Approval Schedule (TAS)
for monolithic microwave integrated circuits
(IEC 60747-16-10:2004)

Dispositifs à semiconducteurs
Partie 16-10: Format-cadre
pour agrément de technologie (TAS)
pour circuits intégrés monolithiques
hyperfréquences
(CEI 60747-16-10:2004)

Halbleiterbauelemente
Teil 16-10: Prüfplan für die
Technikanerkennung
(Technology Approval Schedule - TAS)
für monolithische integrierte
Mikrowellenschaltkreise
(IEC 60747-16-10:2004)

This European Standard was approved by CENELEC on 2004-09-01. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 47E/257/FDIS, future edition 1 of IEC 60747-16-10, prepared by SC 47E, Discrete semiconductor devices, of IEC TC 47, Semiconductor devices, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 60747-16-10 on 2004-09-01.

The following dates were fixed:

- | | | |
|--|-------|------------|
| – latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement | (dop) | 2005-06-01 |
| – latest date by which the national standards conflicting with the EN have to be withdrawn | (dow) | 2007-09-01 |

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 60747-16-10:2004 was approved by CENELEC as a European Standard without any modification.

CONTENTS

INTRODUCTION.....	5
1 General	6
1.1 Scope.....	6
1.2 Normative documents.....	6
1.3 Units, symbols and terminology	7
1.4 Standard and preferred values	7
1.5 Definitions	7
2 Definition of the component technology	9
2.1 Scope.....	9
2.2 Description of activities and flow charts	10
2.3 Technical abstract	10
2.4 Requirements for control of subcontractors	13
3 Component design of MMICs.....	15
3.1 Scope.....	15
3.2 Description of activities and flow charts	15
3.3 Interfaces	16
3.4 Validations and control of the processes	18
4 Mask manufacture	20
4.1 Scope.....	20
4.2 Description of activities and flow charts	20
4.3 Validation and control of the processes	20
4.4 Subcontractors, vendors and internal suppliers	20
5 Wafer fabrication of MMICs	20
5.1 Scope.....	20
5.2 Description of activities and flow charts	21
5.3 Equipment	23
5.4 Materials	23
5.5 Re-work	23
5.6 Validation methods and control of the processes	24
5.7 Interrelationship	25
6 Wafer probing of MMICs.....	27
6.1 Scope.....	27
6.2 Description of activities and flow charts	27
6.3 Equipment	27
6.4 Test procedures	27
6.5 Interrelationship	27
7 Back-side process for bare chip delivery	29
7.1 Scope.....	29
7.2 Description of activity and flow charts.....	29
7.3 Equipment	30
7.4 Materials	30
7.5 Validation methods and control of the processes	30
7.6 Interrelationship	30
7.7 Validity of release.....	31
8 Assembly of MMICs.....	33

8.1	Scope.....	33
8.2	Description of activities and flow charts.....	33
8.3	Materials, inspection and handling.....	34
8.4	Equipment.....	34
8.5	Re-work	34
8.6	Validation and control of the processes	34
8.7	Interrelationships.....	35
9	Testing of MMICs	37
9.1	Scope.....	37
9.2	Description of activities and flow charts.....	37
9.3	Equipment.....	37
9.4	Test procedures	38
9.5	Interfaces	39
9.6	Validation and control of the processes	40
9.7	Process boundary verification.....	43
9.8	Product verification.....	47
10	Process characterization	47
10.1	Identification of process characteristics	47
10.2	Description of activities	48
10.3	Characterization procedures.....	49
11	Packaging and shipping.....	50
11.1	Description of activities and flow charts.....	50
11.2	Interfaces	51
11.3	Validity of release.....	51
12	Withdrawal of Technology Approval.....	53
Figure 1 – Example flow chart of design/manufacture/test.....		14
Figure 2 – Example flow chart of a design.....		19
Figure 3 – Technology flow chart of the process		26
Figure 4 – Example flow chart for a wafer probing.		28
Figure 5 – Example flow chart for a back-side process for bare chip delivery		32
Figure 6 – Example flow chart for an assembly		36
Figure 7 – Example flow chart for a testing		42
Figure 8 – Typical flow chart for packaging and shipping		52

INTRODUCTION

The requirements for Technology Approval for manufacturers of electronic and electro-mechanical components are given in QC 001002-3, Clause 6. The procedures for approval defined in that clause require the manufacturer to have available an appropriate Technology Approval Schedule (TAS).

This schedule defines how the principles and requirements of QC 001002-3, Clause 6 are applied to monolithic microwave integrated circuits.

SEMICONDUCTOR DEVICES –

Part 16-10: Technology Approval Schedule (TAS) for monolithic microwave integrated circuits

1 General

1.1 Scope

This TAS specifies the terms, definitions, symbols, quality system, test, assessment and verification methods and other requirements relevant to the design, manufacture and supply of monolithic microwave integrated circuits in compliance with the general requirements of the IECQ-CECC System for electronic components of assessed quality.

1.2 Normative documents

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60027 (all parts): *Letter symbols to be used in electrical technology*

IEC 60050: *International Electrotechnical Vocabulary*

IEC 60068 (all parts): *Environmental testing*

IEC 60191-2: *Mechanical standardisation of semiconductor devices – Part 2: Dimensions*

IEC 60617-DB¹ (all parts): *Graphical symbols for diagrams*

IEC 60747-1: *Semiconductor devices – Discrete devices and integrated circuits – Part 1: General*

IEC 60747-16-1: *Semiconductor devices – Part 16-1: Microwave integrated circuits – Amplifiers*

IEC 60747-16-2: *Semiconductor devices – Part 16-2: Microwave integrated circuits – Frequency prescalers*

IEC 60747-16-3: *Semiconductor devices – Part 16-3: Microwave integrated circuits – Frequency converters*

IEC 60747-16-4: *Semiconductor devices – Part 16-4: Microwave integrated circuits – Switches²*

IEC 60748-1: *Semiconductor devices – Integrated circuits – Part 1: General*

ISO 1000: *SI units and recommendations for the use of their multiples and certain other units*

¹ "DB" refers to the IEC on-line database.

² To be published.

1.3 Units, symbols and terminology

Units, graphical symbols, letter symbols and terminology shall, whenever possible, be taken from the following documents:

IEC 60027: *Letter symbols to be used in electrical technology*

IEC 60050: *International electrotechnical vocabulary*

IEC 60617-DB: *Graphical symbols for diagrams*

ISO 1000: *SI units and recommendations for the use of their multiples and certain other units*

Any other units, symbols and terminology specific to the scope of this TAS shall be taken from the relevant IEC or ISO documents listed under Normative documents.

1.4 Standard and preferred values

Technology Approval allows the customization of the component or process to suit each customer. The conventional concept of preferred values may thus have limited application. However, when internationally recognized preferred values apply these should be used, e.g. voltage, temperature and dimensions. Reference shall be made to the appropriate IEC or ISO publications, i.e.:

- voltage IEC 60747-1
- temperature IEC 60747-1
- dimensions IEC 60191-2.

1.5 Definitions

For the purposes of this document, the following definitions apply.

1.5.1 General terms for monolithic microwave integrated circuits

1.5.1.1 microelectronics

(IEC 60748-1, definition 4.1.5)

1.5.1.2 microcircuit

(IEC 60748-1, definition 4.2.2)

1.5.1.3 integrated circuit

(IEC 60748-1, definition 4.2.3)

1.5.1.4 integrated microcircuit

microcircuit in which a number of circuit elements are inseparably associated and electrically interconnected such that for the purpose of specification and testing and commerce and maintenance, it is considered indivisible

NOTE 1 For this definition, a circuit element does not have an envelope or external connection and is not specified or sold as a separate item.

NOTE 2 Where no misunderstanding is possible, the term "integrated microcircuit" may be abbreviated to "integrated circuit".

NOTE 3 Further qualifying terms may be used to describe the technique used in the manufacture of a specific integrated microcircuit. Examples to the use of qualifying terms: semiconductor monolithic integrated circuit; semiconductor multi-chip integrated circuit; thin film integrated circuit; thick film integrated circuit; hybrid integrated circuit.

1.5.1.5**micro-assembly**

microcircuit consisting of various components and/or integrated microcircuits which are constructed separately and which can be tested before being assembled and packaged

NOTE 1 For this definition, a component has external connections and possibly an envelope as well and it also can be specified and sold as a separate item.

NOTE 2 Further qualifying terms may be used to describe the form of the components and/or the assembly techniques used in the construction of a specific micro-assembly. Examples of use of qualifying terms: semiconductor multi-chip micro-assembly; discrete component micro-assembly.

1.5.2 List of abbreviations

- ASIC: Application Specific Integrated Circuit
- BDS: Blank Detail Specification
- BICMOS: Bipolar and Complementary Metal Oxide Silicon
- CAD: Computer Aided Design
- CAE: Computer Aided Engineering
- CECC: CENELEC Electronic Components Committee
- CMB: Contract Management Branch
- Cpk: Index of critical process capability
- Die Shear: Test on die attach
- DIL: Dual In Line Package
- DRC: Design Rules Check
- Dye Penetrant (ZYGLO): Seal test
- EDP: Electronic Data Processing
- EFR: Electrical Failure Rate
- ERC: Electrical Rules Check
- ESD: Electro Static Discharge
- GaAs: Gallium Arsenide
- HBT: Hetero-junction Bipolar Transistor
- HEMT: High Electron Mobility Transistor
- ISO 9000: ISO International Quality Rules
- JFET: Junction Field Effect Transistor
- LRM: Line Reflect Match
- LSSD: Level Sensitive Scan Design
- LVS: Layout Versus Schematics
- MESFET: Metal Semiconductor Field Effect Transistor
- MMIC: Monolithic Microwave Integrated Circuits
- MODFET: Modulation Doped Field Effect Transistor
- MTF: Mean Time to Failure
- MTBF: Mean Time Between Failures
- MTTR: Mean Time To Repair
- NMOS: Metal Oxide Silicon N channel

- OS: Operating System
- PAS: Publicly Available Specification
- PCM: Process Control Monitor
- PDA: Percentage Defectives Allowed
- PM: Parametric Monitor
- PMOS: Metal Oxide Silicon P channel
- POST CAP: Inspection after Encapsulation
- PRE CAP: Inspection before Encapsulation
- QA: Quality Assurance
- QCI: Quality Conformance Inspection
- QML: Qualified Manufacturer List
- RIE: Reactive Ion Etching
- SEC: Standard Evaluation Circuit
- SEM: Scanning Electron Microscope
- SI: Supervising Inspectorate
- SOI: Silicon on Insulator
- SOLT: Short Open Load Thru
- SOS: Silicon on Sapphire
- SPC: Statistical Process Control
- Si: Silicon
- TADD: Technology Approval Declaration Document
- TCI: Technology Conformance Inspection
- TCV: Technology Characterization Vehicle
- TDDB: Time Dependent Dielectric Breakdown
- TQM: Total Quality Management
- TRB: Technology Review Board
- TRL: Thru Reflect Line
- VT: Threshold Voltage for FET
- ZYGLO: see Dye Penetrant.

NOTE PCM and PM have the same meaning; however, PCM is the term used in the following subclauses.

1.5.3 Definitions relevant to the scope of the TAS

See QC 001002-3, Clause 6 for definitions specific to Technology Approval.

2 Definition of the component technology

2.1 Scope

The Technology Approval for the declared range or family of components shall include their design and manufacturing processes and their interfaces. The overall management of these interfaces by the Control Site shall be included. These processes and interfaces shall be declared within the Technology Approval Declaration Document (TADD).

More detailed requirements for the listed processes and interfaces to be included within the Technology Approval are given in the relevant clauses of this TAS. The processes are listed below with the identification of the MAIN TECHNICAL PROCESS:

- Process characterization
- Integrated circuit design – This is a MAIN TECHNICAL PROCESS
- Mask manufacture
- Wafer fabrication – This is a MAIN TECHNICAL PROCESS
- Back-side process
- Wafer probe
- Assembly – This is a MAIN TECHNICAL PROCESS
- Test and release – This is a MAIN TECHNICAL PROCESS
- Packaging and shipping

Shipping includes the temporary storage of finished products before shipment to the customer.

2.2 Description of activities and flow charts

2.2.1 Description of activities

All the activities (processes) shall be identified with the relevant flow charts included. This information may include different processes for different types of components but covered by the same technology. Where applicable, these should address all the processes listed in 2.1.

The design and manufacturing cycle of integrated circuits may involve one or more qualified company or facility handling different tasks within the “life cycle” of an MMIC.

Design, development or specification of an MMIC is performed to the specific requirements of a customer, which may be an external customer (such as for an application-specific MMIC), or an internal department.

The prime contractor is that organization which undertakes the responsibility for the management of all tasks prior to the supply of an MMIC to the specified requirements.

2.2.2 Flow charts

The flow chart in Figure 1 is an example showing such operations, where the specific stages are expected to be defined, referencing the relevant internal documentation.

2.3 Technical abstract

2.3.1 TADD abstract (not for publication)

The Technology Approval technical abstract shall be declared by the technology approval declaration document (TADD).

For each technology declared the following shall be identified:

- Description of design tools used e.g. CAD systems, software;
- Description of wafer fabrication processes including feature size, technology, types and number of interconnects
 - e.g. 0,5 µm gate, GaAs MESFET, double layer metal;

- Description/list of products and/or family of products
 - e.g. low noise amplifiers; power amplifiers; switches;
- Description of packaging types/materials and range of pincounts
 - e.g. chip form: ceramic, DIL 8, 16 pin;
- Description of test equipment, i.e. type of test equipment and scope.

An example of a Technology Approval technical abstract is given in 2.3.3.

2.3.2 QC 001005 abstract

The information to be published within QC 001005:2000, Register of Firms, Products and Services approved under the IECQ-CECC System, including ISO 9000, may be based on the information given to satisfy the Technology Approval technical abstract of 2.3.1. Information marked with an asterisk (“*”) may be omitted in the published “Abstract of Technology Approval” if requested by Control Site.

2.3.3 Example of a Technology Approval technical abstract

TECHNOLOGY DESCRIPTION: MONOLITHIC MICROWAVE INTEGRATED CIRCUIT

Manufacture [Control Site]: *Name and location*
 IEC Reference: *QC 210021 – TAS for Monolithic Microwave Integrated Circuits*
 Certificate Number: *Reference of the local SI*
 TADD Generic: *Control Site's Document Reference*
(Cross references to other TADD shall exist in the Generic Specification where applicable).

LIBRARY/DESIGN

Manufacturer's name of the library:
 Information on the library (where applicable):
 Purpose: ☐ Microwave Design ☐ Digital Design ☐ Others
 Types: ☐ Standard Cells ☐ Element Cells
 Contents: ☐ Types of cells

WAFER FABRICATION:

Wafer Fabrication Process Name: *(e.g. "AMES0.5" etc.)*
 Wafer Fabrication Process Type: *(e.g. FET/Bipolar etc.)*
 Function: *(e.g. Standard Cell/Custom etc.)*
 Production Families: *(e.g. Low Noise/High Power/Control etc.)*
 Details:
 Wafer Size: *(e.g. 100 mm)*
 Gate Length: *(e.g. 0,5 μ m)*
 Maximum Interconnect Levels:* *(Triple/Double/Single Level/Metal etc.)**
 Transmission line structure: *(e.g. microstrip/coplanar waveguide etc.)*
 Metal Compositions:* *(Al/Si/Al/Cu etc.)**
 Gate Material:* *(Metal/Polysilicon etc.)**
 Passivation Material:* *(1,2 μ m Compressive Nitride etc.)**
 Substrate Material:* *(e.g. GaAs)**
 Number of masks:* *(e.g. 8)**

ASSEMBLY:

Package types: *(e.g. Thin Plastic Quad Flat Pack, 7,6 mm Small Outline (SO) etc.)*
 Details:
 Maximum Die Size: *(e.g. TPQFP – 9 x 9 mm: SO300 – 2,3 mm x 2,3 mm)*
 Package materials: *(e.g. Ceramic/Epoxy/Plastic etc.)*
 Header/Leadframe:* *(e.g. Copper/Alloy 42 etc.)**
 Pin/Lead Finish: *(e.g. Gold/Solder Dipped etc.)*
 Die Attachment:* *(e.g. Silicon-Gold Eutectic etc.)**
 Bond Wire Attachment:* *(e.g. Aluminium, Ultrasonic etc.)**
 Package assembly

ELECTRICAL CHARACTERISTICS OF PRODUCTS:

Supply Voltage Range:
 Maximum Input Power:
 Total Power Dissipation:
 Maximum Operating Frequency:
 Operating Temperature Range:
 Storage Temperature Range:

ENVIRONMENTAL/RELIABILITY LIMITS:

Endurance Test Performance: *(e.g. > x year at 55 °C or > 1 000 h at 125 °C)*
 Accelerated Damp Heat Severity: *(e.g. > x year at 55 °C/60 % RH or 1 000 h at 85 °C/85 % RH)*
 Temperature Cycling Extremes: *(e.g. –65 °C / +150 °C)*
 etc.
 AND
 Expected Failure Rate *(under specified environments)*
 Quality Factor (π_Q).

(The limits of approval shall be made available to the customer, and any tests should correlate to IEC test methods and should be suitable for the intended application.)

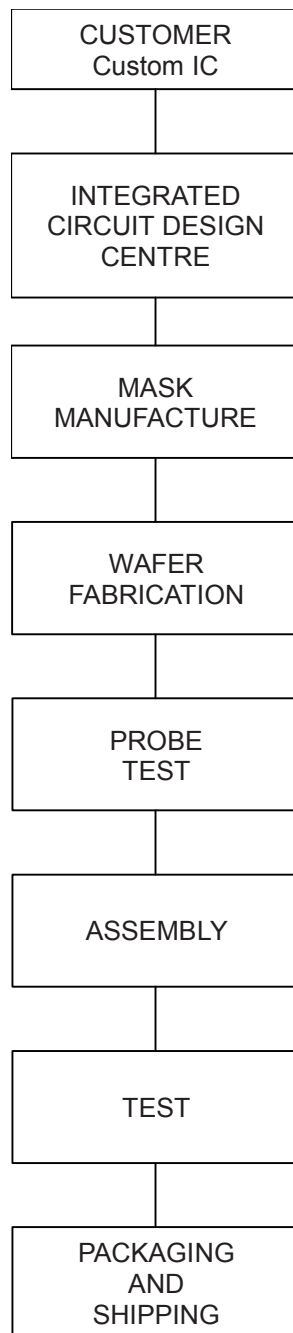
2.4 Requirements for control of subcontractors

Where a technical process as defined in 2.1 is subcontracted, the procedures and criteria employed to demonstrate control shall be specified. This may be achieved either by the demonstration of conformance to the requirements of the appropriate PAS (Publicly Available Specification) in the IECQ-CECC 200000 series, or by demonstrating that the processes have been satisfactorily performed in accordance with criteria defined or referenced from the TADD. Such criteria shall be capable of demonstrating compliance with the declaration of reliability and environmental performance.

The following items shall be specified:

- Reason for subcontracting
- Name and address
- IECQ-CECC Process and Approval or Technology Approval certificate reference (where appropriate)
- Name of CMB (Contract Management Branch) contract within the subcontractor
- Documentation
- Interrelationship documentation.

NOTE Design, mask manufacture, wafer fabrication, wafer probe, assembly, testing, packaging and shipping may be subcontracted provided that the control site has the capability for at least one of the MAIN TECHNICAL PROCESSES as defined in 6.2.1.3 of QC 001002-3.



IEC 876/04

NOTE This is an example of a packaged device.

Figure 1 – Example flow chart of design/manufacture/test

3 Component design of MMICs

3.1 Scope

Design information relevant to the technology for which approval is sought shall be included in the TADD.

This shall include design of the semiconductor process incorporating modification and publication of the process parameters and related process design rules in the form of written and computer files suitable for use in CAD tools at either internal customers or independent design centres.

Process characterization and circuit design are, in general, separate though inter-related tasks, and so their interfaces with the process design task shall be specified in detail, including management responsibilities, transfer specifications, requirements and deliverables.

The IC design centre is responsible for the design of integrated circuits in accordance with customer requests as defined by product or other specifications, generally by translation from received data into IC specifications, then design and simulation phases followed by production of data, specifications, and computer files (or equivalent) required for manufacturing. This shall generally employ data from the process design task.

Activities may include mask making and writing product test programmes or test data suitable for development into test programmes by a test centre or task.

3.2 Description of activities and flow charts

3.2.1 Description of activities

The activities of design for integrated circuits shall be declared, including flow charts showing all activities, critical steps, check points and quality indicators, referencing the relevant internal documentation. These shall include any or all of items a) to e) below, as appropriate:

a) Feasibility

The availability of equipment and of the design/manufacturing capacity to cover the required production lot quantities shall be verified.

b) Process design

- i) Physical characteristics (required for circuit design)
- ii) Electrical characteristics
- iii) Layout rules.

c) Design services and support

- i) Design Rule Checker (DRC)
- ii) Layout Versus Schematic (LVS)
- iii) Process rules (wafer fab and assembly)
- iv) CAD Models.

d) Circuit design tools

- i) Linear simulation (frequency domain)
- ii) Harmonic balance
- iii) SPICE
- iv) Electromagnetic analysis
- v) Other.

e) Conversion or adaptation of existing designs

Any activities not so described shall be stated with reference to the relevant documentation and interface controls. The information to be listed, where applicable, concerns:

- i) basic technologies (processes, layers, elements, geometries, described in design book, etc.);
- ii) design rules identification (including physical, electrical and layout for wafer fab and assembly also described in design book);
- iii) CAD data and tools for each type of component e.g. hardware, software and cell libraries generally part of the design kit;
- iv) verification and validation procedures;
- v) package selection or design procedures;
- vi) test programmes (e.g. test description language, test parameters, etc.).

3.2.2 Flow charts

For an example of a typical flow chart, see Figure 2.

3.3 Interfaces

3.3.1 Design/manufacture

The manufacturing interrelationship during the design stages shall be declared, including those with

- manufacturing (mask manufacture and/or fabrication),
- management of software configuration and library updates,
- upward compatibility,
- documentation,
- traceability,
- usage limits (model, accuracy),
- usage of verification tools (DRC, ERC, LVS),
- assembly (including package suppliers),
- prototyping (if applicable),
- characterization and test (including equipment and specifications),
- any other requirements.

3.3.2 Customer/user

The design centre defines its policy related to the involvement of the customer during the various design steps:

- Specifications
 - writing the technical need specification.
- Design reviews
 - functional simulation,
 - test oriented simulation ,
 - place and electromagnetic simulation.