

Specification for

Domestic Digital Bus (D2B) for audio, video and audiovisual systems

The European Standard EN 61030:1993 has the status of a
British Standard

UDC 681.3.02:681.3.037.37

NO COPYING WITHOUT BSI PERMISSION EXCEPT AS PERMITTED BY COPYRIGHT LAW



Document Sharing Hub

Committees responsible for this British Standard

The preparation of this British Standard was entrusted by the Electronic Equipment Standards Policy Committee (EEL/-) to Technical Committee EEL/32, upon which the following bodies were represented:

- Association for Consumer Research (ACRE)
- Association of British Theatre Technicians
- Audio Engineering Society
- British Broadcasting Corporation
- British Educational Equipment Association
- British Kinematograph Sound and Television Society
- British Radio and Electronic Equipment Manufacturers' Association
- British Telecommunications plc
- Consumer Policy Committee of BSI
- Federation of British Audio
- Independent Broadcasting Authority
- Independent Television Association
- Institution of Electrical Engineers
- National Council for Educational Technology (NCET)
- Professional Lighting and Sound Association
- Radio Electrical and Television Retailers' Association
- Royal Institute of British Architects
- Royal National Institute for the Deaf
- Society of Cable Television Engineers
- Sound and Communication Industries Federation

This British Standard, having been prepared under the direction of the Electronic Equipment Standards Policy Committee, was published under the authority of the Standards Board and comes into effect on 20 December 1991

© BSI 01-2000

The following BSI references relate to the work on this standard:
Committee reference EEL/32
Draft for comment 88/32207 DC

ISBN 0 580 20286 0

Amendments issued since publication

Amd. No.	Date of issue	Comments
7902	October 1993	Indicated by a sideline in the margin

Contents

	Page
Committees responsible	Inside front cover
National foreword	iv
Foreword	2
1 Scope and main features of the Domestic Digital Bus (D2B)	3
2 Normative reference	3
3 Definitions and abbreviations	4
3.1 Definitions	4
3.2 Abbreviations	4
4 Modes	5
5 Main transmission features of D2B	6
5.1 Communication-related functions	6
5.2 Characteristics of transmitted signals	6
6 Frame structure	6
7 Frame exchange protocols	8
7.1 Frame sequences and acknowledgements	8
7.1.1 Write sequence	9
7.1.2 Read sequence	10
7.2 Description of the frame protocol	11
7.2.1 Start bit	11
7.2.2 Mode bits	11
7.2.3 Master address bits	12
7.2.4 Slave address bits	12
7.2.4.1 Slave address acknowledge	12
7.2.5 Control bits	12
7.2.5.1 Interpretation of the four control bits	13
7.2.5.2 Control acknowledge	13
7.2.6 Data field	13
7.2.6.1 Data bits	13
7.2.6.2 End of data bit	13
7.2.6.3 Data parity bit	14
7.2.6.4 Data acknowledge bit	14
7.2.7 Acknowledgement data	14
7.2.8 Activating the lock/unlock function	14
7.2.9 Medium access protocol	14
7.2.9.1 Physical characteristics	14
7.2.9.2 Carrier sense	14
7.2.9.3 Collision detection	14
8 Bit formats	14
8.1 General bit format	14
8.2 Detailed description of the bit formats	16
8.2.1 Introduction	16
8.2.2 Start bit (see Figure 8)	16
8.2.3 Arbitration bits (see Figure 9)	19
8.2.4 Master to Slave bits (see Figure 10)	23
8.2.5 Slave to Master bits (see Figure 11)	26
9 Address allocation	28
9.1 Address space definition	28

	Page
9.2 Allocation of AV/C address codes (Service code 0001)	29
9.3 Sub-devices	30
10 Data interpretation	32
10.1 Slave status	32
10.2 Lock address	32
10.3 Property memory	33
10.4 Data	33
10.5 Commands	33
10.5.1 Principles of the command table	33
10.5.2 The service classification commands	34
10.5.3 Addressing of sub-devices	34
10.5.4 The “END” command	35
11 Gateway communication	35
11.1 Gateway communication in the Japanese home bus system (HBS) format	36
11.2 Gateway communication in the format specified with the OPR	38
11.3 Gateway addresses	38
12 Command extension	38
13 Multiple frame message format	39
14 Electrical specification of a D2B system	39
14.1 Typical circuit configuration (see Figure 21)	40
14.2 Logical and electrical state relationship	40
14.3 Driver specification	40
14.4 Receiver specification	41
14.5 Cable specification	42
Annex A (normative) The command table	43
Function commands — group	44
Video commands	44
Audio commands	45
Deck/player commands	47
Tuner commands	49
Text function commands	51
Function commands — specific	52
Camera video commands	52
Timer commands	53
Annex ZA (normative) Other international publications quoted in this standard with the references of the relevant European publications	57
National annex NA (informative) Cross-references	Inside back cover
Figure 1 — Configuration	3
Figure 2 — Structure of D2B frame	7
Figure 3 — Flow chart showing frame exchange protocol	8
Figure 4 — Sequence of frame bits during a Master to Slave transfer — Write action	9
Figure 5 — Sequence of frame bits during a Slave to Master transfer — Read action	10
Figure 6 — Frame format	11
Figure 7 — Example of a D2B digital filter	15

	Page
Figure 8 — Start bit	19
Figure 9 — Arbitration bit	22
Figure 10 — Master to Slave bit	25
Figure 11 — Slave to Master bit	28
Figure 12 — D2B Address Space	29
Figure 13 — Typical D2B address for an AV/C device	29
Figure 14 — Example of configuration with devices and sub-devices	30
Figure 15 — Principles of the command table	34
Figure 16 — Frame format of sub-device address	34
Figure 17 — Format of SSDA and DSDA	35
Figure 18 — D2B as sub system in a configuration with a Home Electronic Bus	36
Figure 19 — Format of SA' and DA'	37
Figure 20 — Frame format	39
Figure 21 — Reference circuit	40
Figure 22 — Driver delay times	41
Figure 23 — Receiver delay times	42
Table 1 — D2B mode parameters	6
Table 2 — Mode bit allocation	12
Table 3 — Control code allocation	13
Table 4 — Allocation of type codes for AV/C device or sub-device (Service code 0001)	31
Table 5 — Allocation of type codes for additional devices or sub-devices (Service code 0011)	31
Table 6 — Slave status bit allocation	32
Table 7 — Bit allocation for mid and least significant lock address nibbles	32
Table 8 — Bit allocation for most significant lock address nibble	33
Table 9 — Bit allocation of the OPR associated with the OPC "Begin 2"	35
Table 10 — SA' and DA' definition	36
Table 11 — Bit allocation of the OPR association with the OPC "Begin 1"	36
Table 12 — Address allocation of gateways	38

National foreword

This British Standard has been prepared under the direction of the Electronic Equipment Standards Policy Committee and is the English version of EN 61030:1993 *Audio, video and audiovisual systems — Domestic Digital Bus (D2B)*, published by the European Committee for Electrotechnical Standardization (CENELEC). It is identical with IEC 1030:1991 and its amendment 1:1993, published by the International Electrotechnical Commission (IEC). As a consequence of implementing the European Standard this British Standard is renumbered as BS EN 61030 and any reference to BS 7536 should be read as a reference to BS EN 61030.

A British Standard does not purport to include all the necessary provisions of a contract. Users of British Standards are responsible for their correct application.

Compliance with a British Standard does not of itself confer immunity from legal obligations.

Summary of pages

This document comprises a front cover, an inside front cover, pages i to iv, the EN title page, pages 2 to 58, an inside back cover and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

EUROPEAN STANDARD

EN 61030

NORME EUROPÉENNE

EUROPÄISCHE NORM

March 1993

UDC 681.3.02:681.3.037.37

Descriptors: Recording apparatus, video recording, sound recording, data recording, appliance interconnections, home electronic systems, data bus, data transmission, information interchange, data blocks, mode of data transmission, characteristics, protocols, structures, dimensions

English version

Audio, video and audiovisual systems Domestic Digital Bus (D2B)

(IEC 1030:1991 + A1:1993)

Systèmes audio, vidéo et audiovisuels — Bus
Numérique Domestique (D2B)
(CEI 1030:1991 + A1:1993)

Audio-, Video- und audiovisuelle Anlagen —
Digitaler Bus für Heimanwendung (D2B)
(IEC 1030:1991 + A1:1993)

This European Standard was approved by CENELEC on 1992-12-09. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

© 1993 Copyright reserved to CENELEC members

Foreword

At the request of the CENELEC Technical Committee TC 103, Electronic entertainment and educational systems for household and similar use, the International Standard IEC 1030:1991 + 84 (C.O.) 98 was submitted to the CENELEC Unique Acceptance Procedure (UAP) in February 1992 for acceptance as a European Standard.

NOTE Document 84(C.O.) 98 was published as amendment 1 in February 1993.

The text of the reference document was approved by CENELEC as EN 61030 on 9 December 1992.

The following dates were fixed:

- latest date of publication
of an identical national
standard (dop) 1993-09-15
- latest date of withdrawal
of conflicting national
standards (dow) 1993-09-15

Annexes designated “normative” are part of the body of the standard. In this standard, Annex A and Annex ZA are normative.

1 Scope and main features of the Domestic Digital Bus (D2B)

This International Standard gives the modes of transmission, the communication protocols, the addressing procedures, the command language and electrical characteristics for the Domestic Digital Bus (D2B) System.

The audio-video cluster (TV set, VCR, etc.) needs a practical bus for interconnecting devices and exchanging messages. D2B was developed for this purpose.

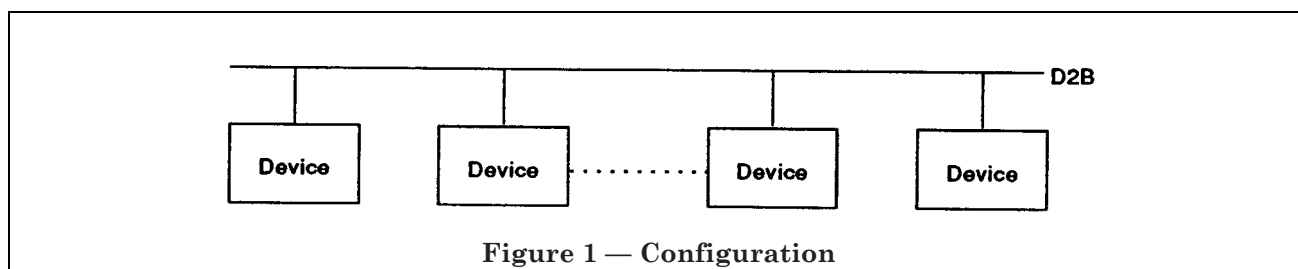
The capabilities of D2B can be described as follows:

- It is appropriate for audio and video, for controllers and for home computers. It can be used as a local independent system for this application or as an audio, video and control subsystem connected via an appropriate gateway to a main bus.
- Following the same scheme, D2B can also be used as a local independent system or as an integrated subsystem for any other application.

In order to allow exchange of digital data in a system made up of devices of various manufacturing origins, it is necessary to have a “standardized communication protocol” suitable for the specific needs of this system.

Within the Home Electronic Bus environment (HEB), D2B can be used as a subsystem. For this reason, the address and command tables for audio, video and control are harmonized with those of the Japanese Home Bus (HBS) and of the European Home Bus (IHS).

The structure of the Domestic Digital Bus (D2B), the transmission speeds, the format and the structure of the frames have therefore been chosen to meet the requirements of the home and small office application area. See Figure 1.



In the D2B system, devices perform as masters and slaves during data transfers. A master device is able to initiate and control a data transfer using D2B.

Depending on the direction of transfer, devices also perform as transmitters or receivers.

The D2B is a multi-master bus, which means that any device capable of controlling the bus can do so. D2B is based on Carrier Sense Multiple Access with Collision Detection (CSMA/CD) with arbitration, based on the unique identification of each device. Each transfer is restricted in time to avoid monopolisation of the bus.

The bus allows a self-configuring network to be built up. D2B allows devices to contain a number of sub-devices.

2 Normative reference

The following standard contains provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the edition indicated was valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent edition of the standard indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 94-5:1988, *Magnetic tape sound recording and reproducing systems — Part 5: Electrical magnetic tape properties*.

3 Definitions and abbreviations

3.1 Definitions

For the purposes of this International Standard, the following definitions apply:

frame

block of information, transferred across the D2B data link. The frame consists of the header field, the master address field, the slave address field, the control field and the message field

header field

field indicating the start of a frame and identifying the mode of a frame (transmission speed)

master address field

field identifying the device which seeks to take control, this being called the “Master”

slave address field

field identifying the device addressed by the master, this being called the “Slave”

control field

field controlling the direction of the message and defining the interpretation of the message

message field

field containing data bytes which carry the message

master (during a particular frame)

device that initiates a D2B frame and controls its timing. Several masters may simultaneously try to initiate a frame, but only one of these masters can gain exclusive access to the medium for the duration of a frame, i.e. be the winning master. D2B devices may or may not be capable of master operation

slave (during a particular frame)

device that responds to a D2B frame, initiated by a master, after being addressed in that frame. All devices capable of slave operation, shall accept and interpret all frames, at least up to and including the slave address field. D2B devices may or may not be capable of slave operation

transmitter (during a particular frame)

device that transmits the information content of the data fields in that frame. In a D2B frame, either the master or the slave can be the transmitter. If the master is the transmitter, then the slave is the receiver, and vice versa

receiver (during a particular frame)

device that receives the information content of that frame

message

information, carried by the data bits of one frame

multiple frame message

message using more than one frame

3.2 Abbreviations

A:	Acknowledge bit
AMS:	Acknowledge from Master to Slave
ARB:	ARbitration Bit
ASCII:	American Standard Code for Information Interchange
ASM:	Acknowledge from Slave to Master
AV/C:	Audio, Video and Control
CSMA/CD:	Carrier Sense Multiple Access with Collision Detection
CT:	Communication Telephony
D2B:	Domestic Digital Bus
DSDA:	Destination Sub-Device Address
EOD:	End Of Data bit

HBS:	Home Bus System, the Japanese home bus system
HEB:	Home Electronic Bus, a home bus system
HK:	HouseKeeping
IHS:	Integrated Home bus System, the European home bus system
LAN:	Local Area Network
LSB:	Least Significant Bit
MS:	Master to Slave bit
MSB:	Most Significant Bit
OPC:	OPeration Code
OPR:	OPeRand
P:	Parity bit
SB:	Start Bit
SCC:	System Common Commands
SM:	Slave to Master bit
SSDA:	Source Sub-Device Address
VCR:	Video Cassette Recorder

4 Modes

D2B is designed to perform in a number of different environments and can transfer data with performance appropriate to each application area. It is thus an “adaptive” transmission channel allowing an optimal use of this resource.

Two main parameters control the data transfer performance:

- a) The maximum number of useful data bytes per frame (bytes contained in the message field).
- b) The nominal data rate for a string of identical frames at the maximum number of bytes per frame.

Operations with a given set of these two parameters define a “D2B mode”.

The D2B modes are ordered and numbered by increasing performance, the lowest basic mode being 0. Currently, 3 modes are defined: modes 0, 1 and 2. These all allow bidirectional exchanges.

A device using D2B, may allow communication in modes 0, 1 or 2, but shall keep the ability to deal with the lower modes. That is to say, it is permitted to provide in the device only mode 0, or mode 0 and mode 1, or mode 0, mode 1 and mode 2.

It is also permitted to provide only the slave function or only the master function or both.

Mode parameters are shown in Table 1.

Table 1 — D2B mode parameters

	Mode 0	Mode 1	Mode 2
Clock frequency	0,75 MHz $\pm$ 25 %	3 MHz $\pm$ 25 %	6 MHz $\pm$ 0,5 %
<i>Master to Slave</i>			
Maximum number of bytes per frame	2	32	128
Useful data rate for:			
One-byte frame	126 bytes/s	395 bytes/s	725 bytes/s
Full frame	209 bytes/s	2 457 bytes/s	7 760 bytes/s
Single-byte frame duration	7,9 ms	2,5 ms	1,4 ms
Full frame duration	9,6 ms	13,0 ms	16,5 ms
<i>Slave to Master</i>			
Maximum number of bytes per frame	2	16	64
Useful data rate for:			
One-byte frame	122 bytes/s	368 bytes/s	700 bytes/s
Full frame	198 bytes/s	1 497 bytes/s	5 355 bytes/s
Single-byte frame duration	8,2 ms	2,7 ms	1,4 ms
Full frame duration	10,1 ms	10,7 ms	12,0 ms
NOTE The figures for “Master to Slave” and “Slave to Master” are related to the nominal value of clock frequency.			

5 Main transmission features of D2B

The D2B shall allow each connected device having a master function to take control of the bus and to exchange data with other devices within the system.

5.1 Communication-related functions:

- the timing protocol of each bit includes checks on timing error, for Master as well as for Slave;
- arbitration, when various devices simultaneously endeavour to take control of the bus;
- Master address, Slave address, control field and each data byte are accompanied by a parity check;
- acknowledgement of the availability of the slave (slave address acknowledge), acceptance of the control code and of the receipt of data bytes during the transmission of a frame.

5.2 Characteristics of transmitted signals

D2B is defined as one logical channel. Signal specifications are indicated for a “balanced cable pair and return” transmission medium. With the use of a suitable electrical or optical and mechanical interface, other media such as coaxial cable or optical fibre can be used.

The relationship between the logic states of the bits is described in clause 7; the timing requirements for balanced cable pairs are described in clause 14.

Transmission shall be bidirectional and bit-synchronized. Logic “0” shall override “1”.

6 Frame structure

Each frame is restricted in time.

The frame, i.e. all the data for communication between Master and Slave, includes the following components, in time sequence (see Figure 2).

Header field:

Start bit Includes a test period for establishing availability of the bus followed by a 1 to 0 transition for synchronisation of all devices, with a special duration of the 0 period, longer than the 0 period of any other bit.

Mode bits Define the transmission speed of the following fields and the maximum number of data bytes of the data field.

Arbitration is requested when more than one device attempts to use the bus at the same time, in which case the lowest mode prevails. The mode parameters (maximum number of bytes per frame, transmission speed, etc.) are indicated in Table 1.

Master address field:

Master bits Define the address number of the device attempting to obtain control of the bus. A parity bit for the address data is included.

When arbitration takes place, the device with the lowest address number prevails.

Slave address field:

Slave bits Define the address number of the device called by the Master. A parity check bit of the address data is included.

The Slave device called shall respond with an acknowledgement of receipt.

Control field:

Control bits Define the type of data to be exchanged and their direction. A parity check bit is included.

A responding Slave device shall acknowledge receipt of the control data when able to perform the requested operation.

Data field:

Data bits Carry the actual data for transmission, in byte organized form.

The receiver of the data byte shall acknowledge the byte to indicate that it has been properly received. The maximum number of bytes in each frame depends upon mode and direction ("Master to Slave" or "Slave to Master" see Table 1).

Each data byte is followed by an end of data bit, a parity bit and an acknowledge bit.

The End of Data bit indicates whether or not this byte is the last one of the frame.

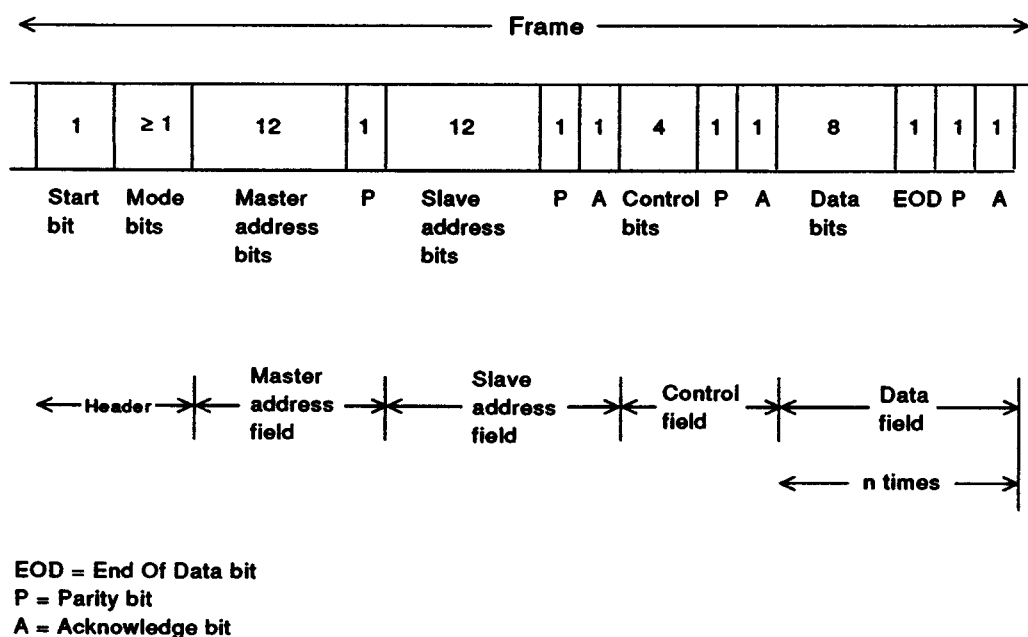
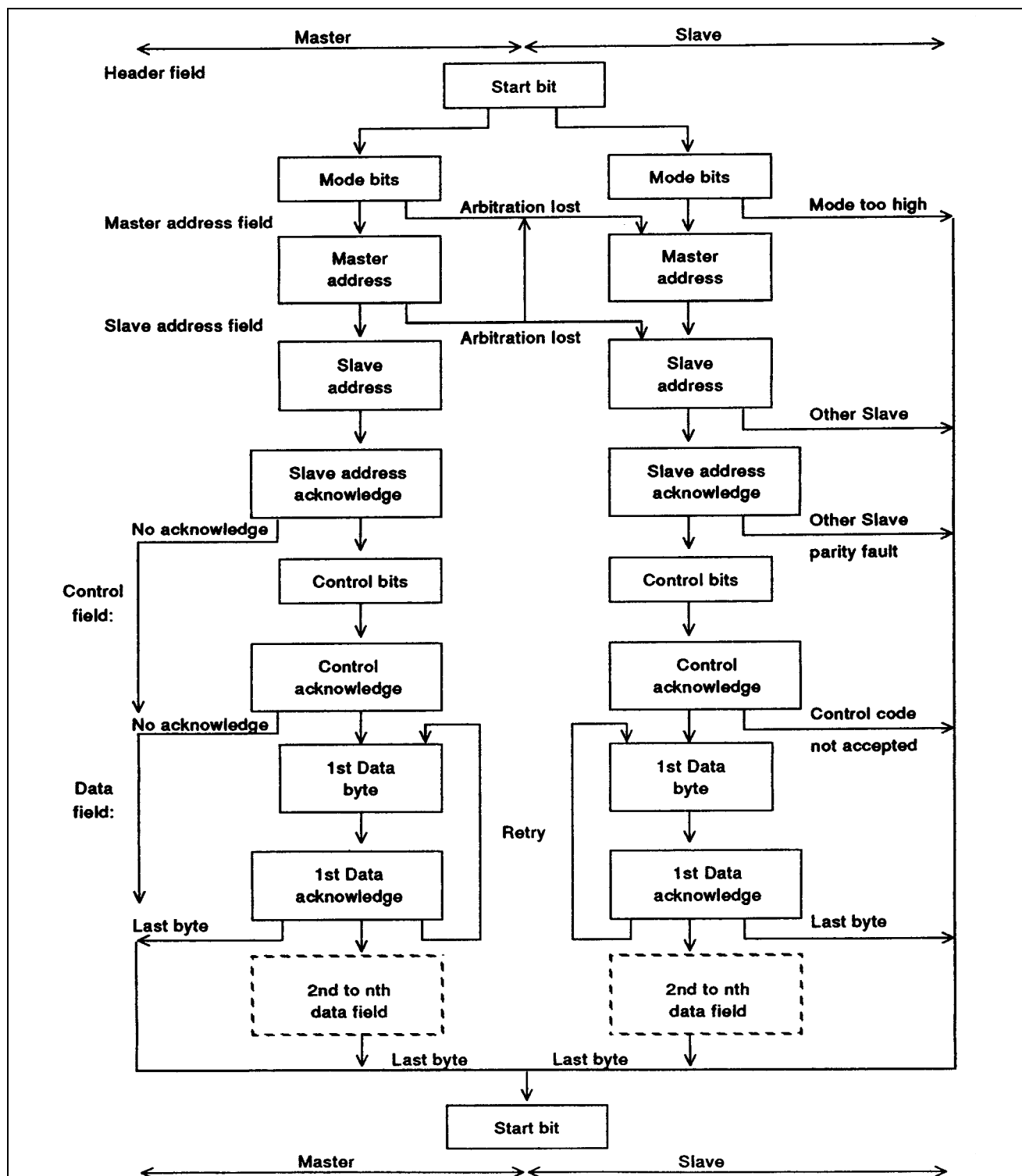


Figure 2 — Structure of D2B frame

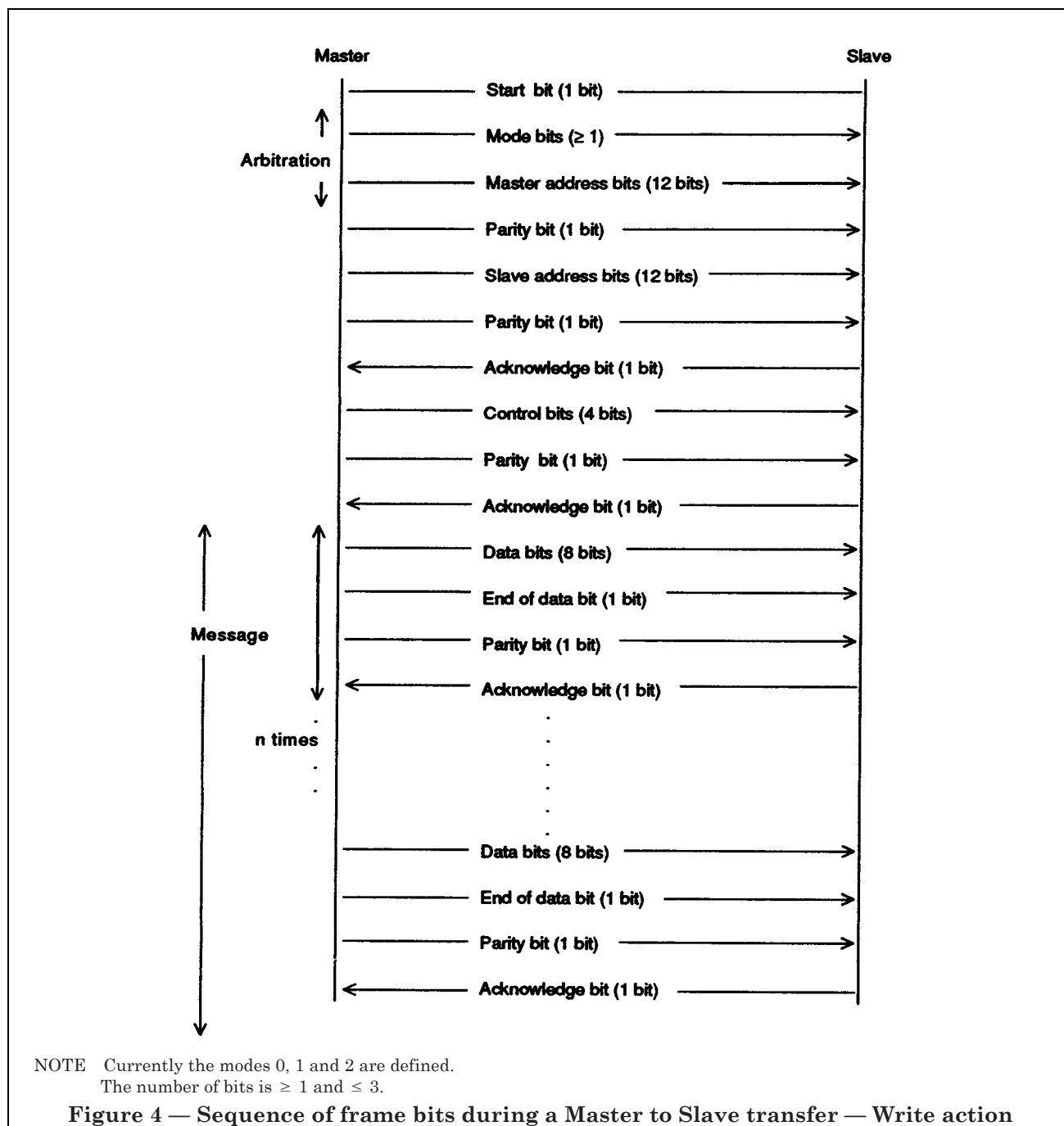
The protocol used to exchange D2B frames between devices is described as follows:

Co-operation takes place between the Master and Slave during the transmission of a frame. Figure 3 is a flowchart showing the interaction between the Master and a Slave for both writing (Master to Slave) data, and reading (Slave to Master) data.



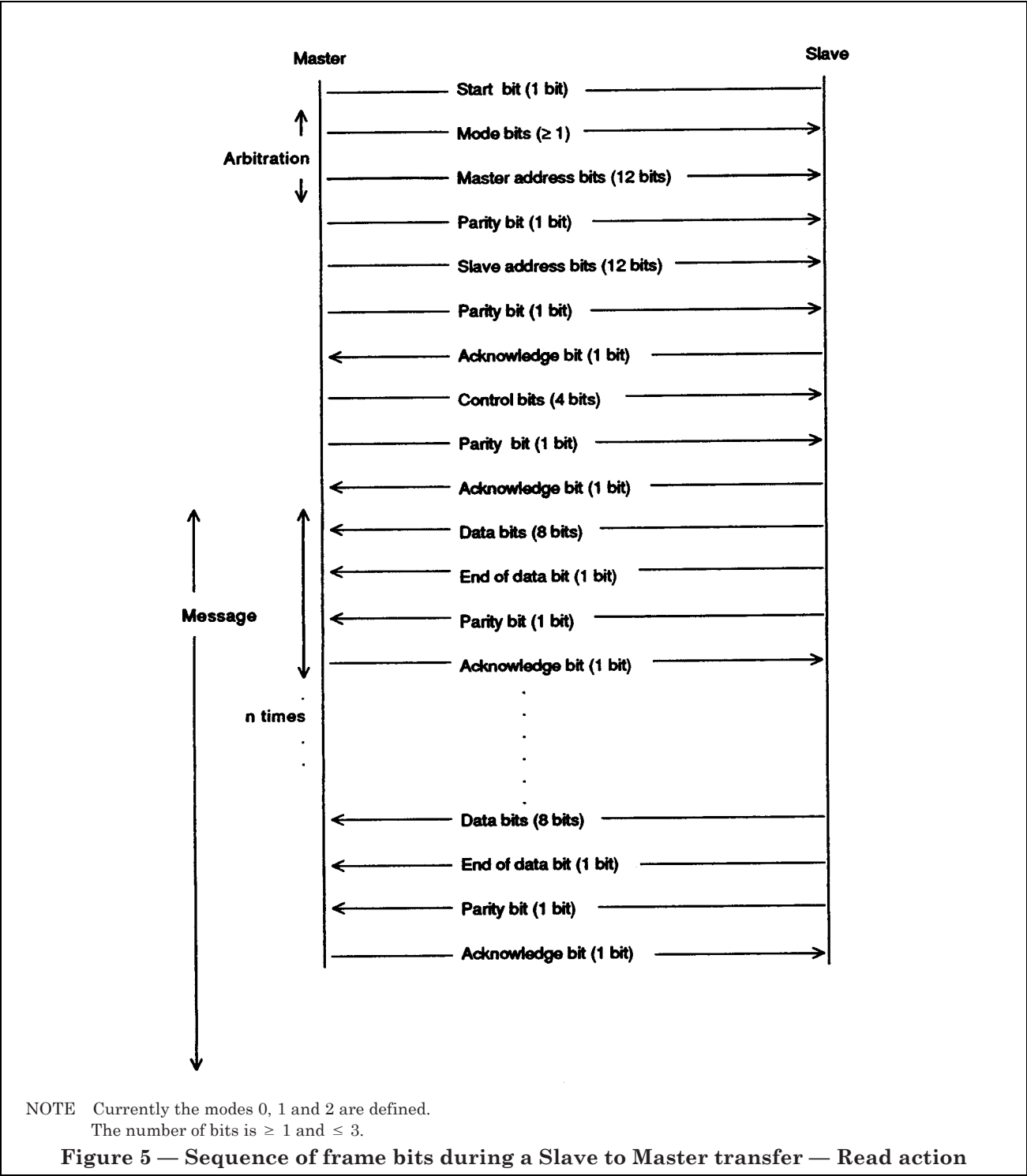
7.1.1 Write sequence

A Master sends (writes) data to a Slave which acknowledges the data, in the sequence shown in Figure 4.



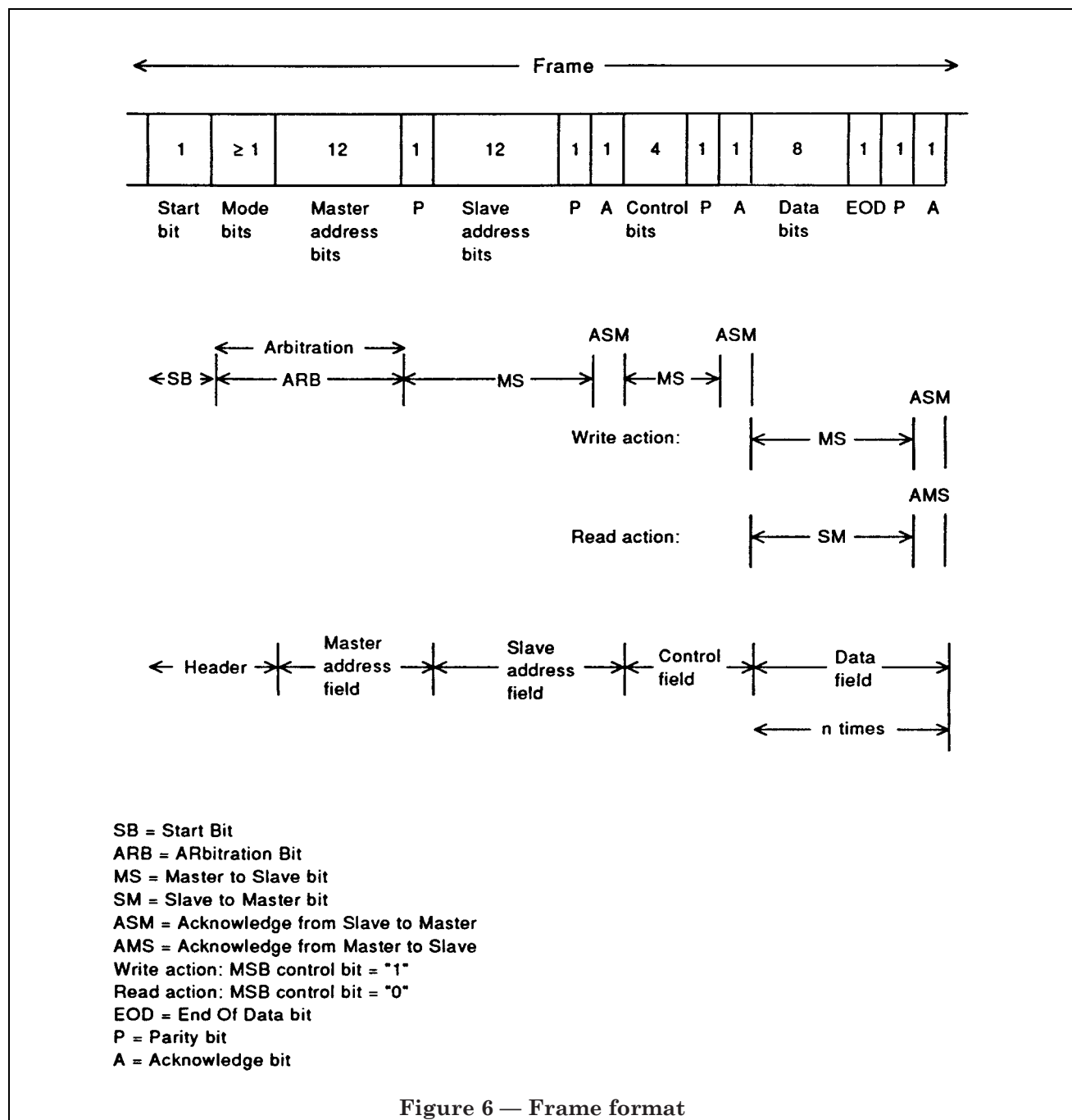
7.1.2 Read sequence

A Master receives (reads) data from a Slave, and acknowledges the data, in the sequence shown in Figure 5.



7.2 Description of the frame protocol

Figure 6 gives an overall view of the frame format.



7.2.1 Start bit

The start bit checks if the bus is free and indicates the start of a frame by a "1" to "0" transition and a defined period for the "0" state.

7.2.2 Mode bits

Number of bits: depends upon the mode.

Number of "1"s preceding the "0" gives the number of the mode (see Table 2).

Table 2 — Mode bit allocation

Mode	Mode bit value
0	0
1	10
2	110
.	111... (reserved for future standardization)

Mode arbitration is automatically in favour of the lowest mode since “0” overrides “1”.
Each frame will start in the lowest mode; so the start bit and the first bit of the mode field are at mode 0 signalling speed.
If the first bit of the mode field is “0” all the remaining bits of the frame are at mode 0 signalling speed.
If the first bit of the mode field is “1” then the second bit of the mode field is at mode 1 signalling speed.
If the second bit of the mode field is “0” all the remaining frame bits are at mode 1 signalling speed.
If the second bit of the mode field is “1” then the third bit of the mode field is at mode 2 signalling speed.
If the third bit of the mode field is “0” all the remaining bits of the frame are at mode 2 signalling speed.
If the third bit of the mode field is “1”, all the remaining bits of the frame are reserved to be specified for compatibility with future higher modes.

7.2.3 Master address bits

Number of bits: 12 for address number plus 1 for odd parity
The parity bit is therefore:
— logical “1” when the 12 address bits comprise an even number of “1”s;
— logical “0” when the 12 address bits comprise an odd number of “1”s.

The address number is a binary number defined by the 12 bits with the most significant bit first.
Master arbitration is automatically in favour of the lowest address number since “0” overrides “1”.

7.2.4 Slave address bits

The same as for Master address number, except that there is no arbitration.

7.2.4.1 Slave address acknowledge

Acknowledge is transmitted from Slave to Master indicating that the following conditions are simultaneously met:
— Slave is present and able to handle the mode;
— no parity failure on received Master address number;
— no parity failure on received Slave address number;
— no timing error.

If no acknowledgement is received the transmitter will stop transmitting.

7.2.5 Control bits

Number of bits: 4 for control code plus 1 odd parity, followed by the period for acknowledgement by the Slave, most significant bit first.
The parity will be:
— logical “1” when the 4 bit control code comprises an even number of “1”s,
— logical “0” when the 4 bit control code comprises an odd number of “1”s.

The control data define:
— direction of transfer: Master to Slave or Slave to Master;
— type of transfer: not locked, transfer and lock, transfer and unlock. When the Slave is locked, no interruption is allowed by other devices, except by means of a “not locked” control code (see Table 3).

Consequently only the locking Master can unlock the Slave. For the Slave, only the slave function is locked. The master function remains enabled e.g. a locked slave device can temporarily become a master but, as a slave, it remains locked to its locking master.

7.2.5.1 Interpretation of the four control bits

B3 is the most significant bit and is transmitted first.

Table 3 — Control code allocation

B3	B2	B1	B0	Direction of the message	Operation	Locking
0	0	0	0	From Slave to Master	Read slave status	Not locked
0	0	0	1		Reserved for future standardization	
0	0	1	0		Read slave status	Lock
0	0	1	1		Read data	Lock
0	1	0	0		Read mid and least significant lock address nibbles	Not locked
0	1	0	1		Read most significant lock address nibble	Not locked
0	1	1	0		Read slave status	Unlock
0	1	1	1		Read data	Unlock
1	0	0	0	From Master to Slave	Write property memory address	Lock
1	0	0	1		Reserve for future standardization	
1	0	1	0		Write command	Lock
1	0	1	1		Write data	Lock
1	1	0	0		Reserved for future standardization	
1	1	0	1		Reserved for future standardization	
1	1	1	0		Write command	Unlock
1	1	1	1		Write data	Unlock

When the control data specify a “not locked” function, all slaves must be able to respond even when locked to another master.

A “not locked” function has no influence on the subsequent lock status of the slave.

7.2.5.2 Control acknowledge

An acknowledgement transmitted from Slave to Master indicates that the following conditions are simultaneously met:

- no parity failure on control bits;
- Slave receiver buffer is empty in case of a transfer from Master to Slave;
- Slave transmitter buffer contains data in case of a transfer from Slave to Master;
- Slave is not locked to another Master, except when a “not locked” function is requested;
- a property memory is implemented in the Slave and a “Write Property memory address” is transmitted;
- no timing error.

If no acknowledgement is received, the transmitter will stop transmitting.

7.2.6 Data field

The 8-bit data bytes are transmitted most significant bit first. The interpretation is specified by the control code, (see 7.2.5.1).

7.2.6.1 Data bits

Number of bits: 8 data bits plus 1 End of Data bit plus odd parity bit, followed by 1 Acknowledgement bit.

7.2.6.2 End of data bit

Interpretation of end of data bit:

- “0” indicates that this was the last data byte of the current frame;
- “1” indicates that a further data byte will follow.

7.2.6.3 Data parity bit

The parity bit is either:

- logical “1” if the 9 bits comprising the 8 bits of the data byte plus the End of Data bit include an even number of “1”s;
- logical “0” if the 9 bits comprising the 8 bits of the data byte plus the End of Data bit include an odd number of “1”s.

7.2.6.4 Data acknowledge bit

Acknowledgement is transmitted either from Slave to Master (following a Master to Slave transfer) indicating:

- no parity failure on last data transfer;
 - slave receiver buffer is not full;
 - no timing error on last data transfer;
- or from Master to Slave (following a Slave to Master transfer) indicating:
- no parity failure on last data transfer;
 - master receiver buffer not full;
 - no timing error on last data transfer.

If no acknowledgement is received the transmitter shall attempt retransmission of the byte, except when this byte was the last byte allowed for in a frame.

A positive data acknowledge means that the byte has been properly received.

7.2.7 Acknowledgement data

A “0” value indicates acknowledgement.

A “1” value indicates no acknowledgement.

7.2.8 Activating the lock/unlock function

The lock status (slave status bit 2) shall be set when the first data acknowledge with value “0” occurs and when the control field of the frame specifies lock.

The lock status (slave status bit 2) shall be reset when the first data acknowledge with value “0” occurs and when the control field of the frame specifies unlock.

7.2.9 Medium access protocol

7.2.9.1 Physical characteristics

Medium access in D2B employs Carrier Sense Multiple Access with Collision Detection (CSMA/CD).

7.2.9.2 Carrier sense

A device acquires the medium by issuing the start bit: – a “1” followed by a transition to “0”. If at any time, while the start bit is “1”, a device senses a “0” on the medium, it yields the medium to the device(s) transmitting the “0”. The “0” overrides the “1” on a medium.

7.2.9.3 Collision detection

Once a device issues the start bit transition to the “0” state it shall then monitor the medium until it completes the transmission of the Master address field. If at any time during this period, the device transmits a “1” while monitoring a “0” on the medium, a collision is detected. The transmitting device detecting a collision shall at once cease transmission.

8 Bit formats

8.1 General bit format

All bits placed on the data bus have four sections transmitted sequentially:

- an initial high period at logic level “1”, the Preparation Period;
- a following low period at logic level “0”, the Synchronization and Start Period;
- a period containing the actual bit value, the Data Period;
- a final period containing logic level “1”, the Stop Period.