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Programmable controllers

Part 9: Single-drop digital
communication interface for small
sensors and actuators (SDCI)

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The UK participation in its preparation was entrusted by Technical Committee GEL/65, Measurement and control, to Subcommittee GEL/65/2, Elements of systems.

A list of organizations represented on this committee can be obtained on request to its secretary.

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© The British Standards Institution 2014.
Published by BSI Standards Limited 2014

ISBN 978 0 580 76607 7
ICS 25.040.40; 35.240.50

Compliance with a British Standard cannot confer immunity from legal obligations.

This British Standard was published under the authority of the Standards Policy and Strategy Committee on 28 February 2014.

Amendments/corrigenda issued since publication

Date	Text affected
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EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN 61131-9

December 2013

ICS 25.040.40; 35.240.50

English version

**Programmable controllers -
Part 9: Single-drop digital communication interface for small sensors and
actuators (SDCI)
(IEC 61131-9:2013)**

Automates programmables -
Partie 9: Interface de communication
numérique point à point pour petits
capteurs et actionneurs (SDCI)
(CEI 61131-9:2013)

Speicherprogrammierbare Steuerungen -
Teil 9: Schnittstelle für die Kommunikation
mit kleinen Sensoren und Aktoren über
eine Punkt-zu-Punkt-Verbindung
(IEC 61131-9:2013)

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Ref. No. EN 61131-9:2013 E

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Foreword

The text of document 65B/874/FDIS, future edition 1 of IEC 61131-9, prepared by SC 65B, "Measurement and control devices", of IEC/TC 65, "Industrial-process measurement, control and automation" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN 61131-9:2013.

The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2014-07-16
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2016-10-16

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In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60870-5-1:1990	NOTE	Harmonised as EN 60870-5-1:1993 (not modified).
IEC 61158-2	NOTE	Harmonised as EN 61158-2 (not modified).
IEC/TR 62453-61	NOTE	Harmonised as CLC/TR 62453-61 (not modified).
ISOIEC 7498-1	NOTE	Harmonised as EN ISOIEC 7498-1 (not modified).

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

NOTE When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 60947-5-2	-	Low-voltage switchgear and controlgear - Part 5-2: Control circuit devices and switching elements - Proximity switches	EN 60947-5-2	-
IEC 61000-4-2	-	Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test	EN 61000-4-2	-
IEC 61000-4-3	-	Electromagnetic compatibility (EMC) - Part 4-3: Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test	EN 61000-4-3	-
IEC 61000-4-4	-	Electromagnetic compatibility (EMC) - Part 4-4: Testing and measurement techniques - Electrical fast transient/burst immunity test	EN 61000-4-4	-
IEC 61000-4-5	-	Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test	FprEN 61000-4-5	-
IEC 61000-4-6	-	Electromagnetic compatibility (EMC) - Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields	FprEN 61000-4-6	-
IEC 61000-4-11	-	Electromagnetic compatibility (EMC) - Part 4-11: Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests	EN 61000-4-11	-
IEC 61000-6-2	-	Electromagnetic compatibility (EMC) - Part 6-2: Generic standards - Immunity for industrial environments	EN 61000-6-2 + corr. September	-
IEC 61000-6-4	-	Electromagnetic compatibility (EMC) - Part 6-4: Generic standards - Emission standard for industrial environments	EN 61000-6-4	-
IEC 61076-2-101	-	Connectors for electronic equipment - Product requirements - Part 2-101: Circular connectors - Detail specification for M12 connectors with screw-locking	EN 61076-2-101	-
IEC 61131-1	-	Programmable controllers - Part 1: General information	EN 61131-1	-

<u>Publication</u>	<u>Year</u>	<u>Title</u>	<u>EN/HD</u>	<u>Year</u>
IEC 61131-2	-	Programmable controllers - Part 2: Equipment requirements and tests	EN 61131-2 ¹⁾	-
IEC/TR 62390	-	Common automation device - Profile guideline	-	-
ISO/IEC 646	1991	Information technology - ISO 7-bit coded character set for information interchange	-	-
ISO/IEC 2022	-	Information technology - Character code structure and extension techniques	-	-
ISO/IEC 10646	-	Information technology - Universal Coded Character Set (UCS)	-	-
ISO/IEC 10731	-	Information technology - Open Systems Interconnection - Basic reference model - Conventions for the definition of OSI services	-	-
ISO 1177	-	Information processing - Character structure for start/stop and synchronous character-oriented transmission	-	-
IEEE 754	2008	Binary floating-point arithmetic	-	-

¹⁾ EN 61131-2 is superseded by EN 61010-2-201:2013, which is based on IEC 61010-2-201:2013.

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INTRODUCTION

0.1 General

IEC 61131-9 is part of a series of standards on programmable controllers and the associated peripherals and should be read in conjunction with the other parts of the series.

Where a conflict exists between this and other IEC standards (except basic safety standards), the provisions of this standard should be considered to govern in the area of programmable controllers and their associated peripherals.

The increased use of micro-controllers embedded in low-cost sensors and actuators has provided opportunities for adding diagnosis and configuration data to support increasing application requirements.

The driving force for the SDCI (IO-Link™¹) technology is the need of these low-cost sensors and actuators to exchange this diagnosis and configuration data with a controller (PC or PLC) using a low-cost, digital communication technology while maintaining backward compatibility with the current DI/DO signals.

In fieldbus concepts, the SDCI technology defines a generic interface for connecting sensors and actuators to a Master unit, which may be combined with gateway capabilities to become a fieldbus remote I/O node.

Any SDCI compliant Device can be attached to any available interface port of the Master. SDCI compliant Devices perform physical to digital conversion in the Device, and then communicate the result directly in a standard format using "coded switching" of the 24 V I/O signalling line, thus removing the need for different DI, DO, AI, AO modules and a variety of cables.

Physical topology is point-to-point from each Device to the Master using 3 wires over distances up to 20 m. The SDCI physical interface is backward compatible with the usual 24 V I/O signalling specified in IEC 61131-2. Transmission rates of 4,8 kbit/s, 38,4 kbit/s and 230,4 kbit/s are supported.

The Master of the SDCI interface detects, identifies and manages Devices plugged into its ports.

Tools allow the association of Devices with their corresponding electronic I/O Device Descriptions (IODD) and their subsequent configuration to match the application requirements.

The SDCI technology specifies three different levels of diagnostic capabilities: for immediate response by automated needs during the production phase, for medium term response by operator intervention, or for longer term commissioning and maintenance via extended diagnosis information.

The structure of this standard is described in 4.8.

Conformity with IEC 61131-9 cannot be claimed unless the requirements of Annex G are met.

Terms of general use are defined in IEC 61131-1 or in the IEC 60050 series. More specific terms are defined in each part.

¹ IO-Link™ is a trade name of the "IO-Link Consortium". This information is given for the convenience of users of this international Standard and does not constitute an endorsement by IEC of the trade name holder or any of its products. Compliance to this standard does not require use of the registered logos for IO-Link™. Use of the registered logos for IO-Link™ requires permission of the "IO-Link Consortium".

0.2 Patent declaration

The International Electrotechnical Commission (IEC) draws attention to the fact that it is claimed that compliance with this document may involve the use of patents concerning the point-to-point serial communication interface for small sensors and actuators as follows, where the [xx] notation indicates the holder of the patent right:

DE 10030845B4 EP 1168271B1 US 6889282B2	[AB]	Fieldbus connecting system for actuators or sensors
EP 1203933 B1	[FE]	Sensor device for measuring at least one variable
DE 10 2004 035 831.1	[SI]	Operational status of a computer system is checked by comparison of actual parameters with reference values and modification to software if needed
DE 102 119 39 A1 US 2003/0200323 A1	[SK]	Coupling apparatus for the coupling of devices to a bus system

IEC takes no position concerning the evidence, validity and scope of these patent rights.

The holders of these patents rights have assured the IEC that they are willing to negotiate licences either free of charge or under reasonable and non-discriminatory terms and conditions with applicants throughout the world. In this respect, the statements of the holders of these patent rights are registered with IEC.

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[AB]	ABB AG Heidelberg Germany
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ISO (www.iso.org/patents) and IEC (<http://patents.iec.ch>) maintain on-line data bases of patents relevant to their standards. Users are encouraged to consult the databases for the most up to date information concerning patents.

PROGRAMMABLE CONTROLLERS –

Part 9: Single-drop digital communication interface for small sensors and actuators (SDCI)

1 Scope

This part of IEC 61131 specifies a single-drop digital communication interface technology for small sensors and actuators SDCI (commonly known as IO-Link™²), which extends the traditional digital input and digital output interfaces as defined in IEC 61131-2 towards a point-to-point communication link. This technology enables the transfer of parameters to Devices and the delivery of diagnostic information from the Devices to the automation system.

This technology is mainly intended for use with simple sensors and actuators in factory automation, which include small and cost-effective microcontrollers.

This part specifies the SDCI communication services and protocol (physical layer, data link layer and application layer in accordance with the ISO/OSI reference model) for both SDCI Masters and Devices.

This part also includes EMC test requirements.

This part does not cover communication interfaces or systems incorporating multiple point or multiple drop linkages, or integration of SDCI into higher level systems such as fieldbuses.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60947-5-2, *Low-voltage switchgear and controlgear – Part 5-2: Control circuit devices and switching elements – Proximity switches*

IEC 61000-4-2, *Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test*

IEC 61000-4-3, *Electromagnetic compatibility (EMC) – Part 4-3: Testing and measurement techniques – Radiated, radio-frequency, electromagnetic field immunity test*

IEC 61000-4-4, *Electromagnetic compatibility (EMC) – Part 4-4: Testing and measurement techniques – Electrical fast transient/burst immunity test*

IEC 61000-4-5, *Electromagnetic compatibility (EMC) – Part 4-5: Testing and measurement techniques – Surge immunity test*

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IEC 61000-4-6, *Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques – Immunity to conducted disturbances, induced by radio-frequency fields*

IEC 61000-4-11, *Electromagnetic compatibility (EMC) – Part 4-11: Testing and measurement techniques – Voltage dips, short interruptions and voltage variations immunity tests*

IEC 61000-6-2, *Electromagnetic compatibility (EMC) – Part 6-2: Generic standards – Immunity for industrial environments*

IEC 61000-6-4, *Electromagnetic compatibility (EMC) – Part 6-4: Generic standards – Emission standard for industrial environments*

IEC 61076-2-101, *Connectors for electronic equipment – Product requirements – Part 2-101: Circular connectors – Detail specification for M12 connectors with screw-locking*

IEC 61131-1, *Programmable controllers – Part 1: General information*

IEC 61131-2, *Programmable controllers – Part 2: Equipment requirements and tests*

IEC/TR 62390, *Common automation device – Profile guideline*

ISO/IEC 646:1991, *Information technology – ISO 7-bit coded character set for information interchange*

ISO/IEC 2022, *Information technology – Character code structure and extension techniques*

ISO/IEC 10646, *Information technology – Universal Multiple-Octet Coded Character Set (UCS)*

ISO/IEC 10731, *Information technology – Open Systems Interconnection – Basic Reference Model – Conventions for the definition of OSI services*

ISO/IEC 19505 (all parts), *Information technology – Object Management Group Unified Modeling Language (OMG UML)*

ISO 1177, *Information processing – Character structure for start/stop and synchronous character oriented transmission*

IEEE Std 754-2008, *IEEE Standard for Floating-Point Arithmetic*

Internet Engineering Task Force (IETF): RFC 5905 – *Network Time Protocol Version 4: Protocol and Algorithms Specification*; available at < www.ietf.org >

3 Terms, definitions, symbols, abbreviated terms and conventions

3.1 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 61131-1 and IEC 61131-2, as well as the following apply.

3.1.1 address

part of the M-sequence control to reference data within data categories of a communication channel

3.1.2

application layer

AL

<SDCI> part of the protocol responsible for the transmission of Process Data objects and On-Request Data objects

3.1.3

block parameter

consistent parameter access via multiple Indices or Subindices

3.1.4

checksum

<SDCI> complementary part of the overall data integrity measures in the data link layer in addition to the UART parity bit

3.1.5

CHKPDU

integrity protection data within an ISDU communication channel generated through XOR processing the octets of a request or response

3.1.6

coded switching

SDCI communication, based on the standard binary signal levels of IEC 61131-2

3.1.7

COM1

SDCI communication mode with transmission rate of 4,8 kbit/s

3.1.8

COM2

SDCI communication mode with transmission rate of 38,4 kbit/s

3.1.9

COM3

SDCI communication mode with transmission rate of 230,4 kbit/s

3.1.10

COMx

one out of three possible SDCI communication modes COM1, COM2, or COM3

3.1.11

communication channel

logical connection between Master and Device

Note 1 to entry: Four communication channels are defined: process channel, page and ISDU channel (for parameters), and diagnosis channel.

3.1.12

communication error

unexpected disturbance of the SDCI transmission protocol

3.1.13

cycle time

time to transmit an M-sequence between a Master and its Device including the following idle time

3.1.14

Device

single passive peer to a Master such as a sensor or actuator

Note 1 to entry: Uppercase "Device" is used for SDCI equipment, while lowercase "device" is used in a generic manner.

3.1.15

Direct Parameters

directly (page) addressed parameters transferred acyclically via the page communication channel without acknowledgement

3.1.16

dynamic parameter

part of a Device's parameter set defined by on-board user interfaces such as teach-in buttons or control panels in addition to the static parameters

3.1.17

Event

instance of a change of conditions in a Device

Note 1 to entry: Uppercase "Event" is used for SDCI Events, while lowercase "event" is used in a generic manner.

Note 2 to entry: An Event is indicated via the Event flag within the Device's status cyclic information, then acyclic transfer of Event data (typically diagnosis information) is conveyed through the diagnosis communication channel.

3.1.18

fallback

transition of a port from coded switching to switching signal mode

3.1.19

inspection level

degree of verification for the Device identity

3.1.20

interleave

segmented cyclic data exchange for Process Data with more than 2 octets through subsequent cycles

3.1.21

ISDU

indexed service data unit used for acyclic acknowledged transmission of parameters that can be segmented in a number of M-sequences

3.1.22

legacy Device or Master

Device or Master designed in accordance with [8]³

3.1.23

M-sequence

sequence of two messages comprising a Master message and its subsequent Device message

3.1.24

M-sequence control

first octet in a Master message indicating the read/write operation, the type of the communication channel, and the address, for example offset or flow control

³ Numbers in square brackets refer to the Bibliography.

3.1.25**M-sequence error**

unexpected or wrong message content, or no response

3.1.26**M-sequence type**

one particular M-sequence format out of a set of specified M-sequence formats

3.1.27**Master**

active peer connected through ports to one up to n Devices and which provides an interface to the gateway to the upper level communication systems or PLCs

Note 1 to entry: Uppercase "Master" is used for SDCI equipment, while lowercase "master" is used in a generic manner.

3.1.28**message**

<SDCI> sequence of UART frames transferred either from a Master to its Device or vice versa following the rules of the SDCI protocol

3.1.29**On-request Data**

acyclically transmitted data upon request of the Master application consisting of parameters or Event data

3.1.30**physical layer**

first layer of the ISO-OSI reference model, which provides the mechanical, electrical, functional and procedural means to activate, maintain, and de-activate physical connections for bit transmission between data-link entities

Note 1 to entry: Physical layer also provides means for wake-up and fallback procedures.

[SOURCE: ISO/IEC 7498-1:1994, 7.7.2, modified – text extracted from subclause, note added]

3.1.31**port**

communication medium interface of the Master to one Device

3.1.32**port operating mode**

state of a Master's port that can be either INACTIVE, DO, DI, FIXEDMODE, or SCANMODE

3.1.33**Process Data**

input or output values from or to a discrete or continuous automation process cyclically transferred with high priority and in a configured schedule automatically after start-up of a Master

3.1.34**Process Data cycle**

complete transfer of all Process Data from or to an individual Device that may comprise several cycles in case of segmentation (interleave)

3.1.35**single parameter**

independent parameter access via one single Index or Subindex

3.1.36

SIO

port operation mode in accordance with digital input and output defined in IEC 61131-2 that is established after power-up or fallback or unsuccessful communication attempts

3.1.37

static parameter

part of a Device's parameter set to be saved in a Master for the case of replacement without engineering tools

3.1.38

switching signal

binary signal from or to a Device when in SIO mode (as opposed to the "coded switching" SDCI communication)

3.1.39

system management

SM

<SDCI> means to control and coordinate the internal communication layers and the exceptions within the Master and its ports, and within each Device

3.1.40

UART frame

<SDCI> bit sequence starting with a start bit, followed by eight bits carrying a data octet, followed by an even parity bit and ending with one stop bit

3.1.41

wake-up

procedure for causing a Device to change its mode from SIO to SDCI

3.1.42

wake-up request

WURQ

physical layer service used by the Master to initiate wake-up of a Device, and put it in a receive ready state

3.2 Symbols and abbreviated terms

Δf_{DTRM}	permissible deviation from data transfer rate (measured in %)
ΔV_S	power supply ripple (measured in V)
AL	application layer
BEP	bit error probability
C/Q	connection for communication (C) or switching (Q) signal (SIO)
CL_{eff}	effective total cable capacity (measured in nF)
CQ	input capacity at C/Q connection (measured in nF)
DI	digital input
DL	data link layer
DO	digital output
f_{DTR}	data transfer rate (measured in bit/s)
H/L	high/low signal at receiver output
I/O	input / output
I_{LL}	input load current at input C/Q to V_0 (measured in A)
IODD	IO Device Description (see 10.8)
I_Q	driver current in saturated operating status ON (measured in A)

<i>I_{QH}</i>	driver current on high-side driver in saturated operating status ON (measured in A)
<i>I_{QL}</i>	driver current on low-side driver in saturated operating status ON (measured in A)
<i>I_{QPK}</i>	maximum driver current in unsaturated operating status ON (measured in A)
<i>I_{QPKH}</i>	maximum driver current on high-side driver in unsaturated operating status ON (measured in A)
<i>I_{QPKL}</i>	maximum driver current on low-side driver in unsaturated operating status ON (measured in A)
<i>I_{QQ}</i>	quiescent current at input C/Q to <i>V₀</i> with inactive output drivers (measured in A)
<i>I_{QWU}</i>	amplitude of Master's wake-up request current (measured in A)
<i>I_S</i>	supply current at <i>V₊</i> (measured in A)
<i>I_{SIR}</i>	current pulse supply capability at <i>V₊</i> (measured in A)
LED	light emitting diode
L-	power supply (-)
L+	power supply (+)
N24	24 V extra power supply (-)
<i>n_{WU}</i>	wake-up retry count
On/Off	driver's ON/OFF switching signal
OD	on-request data
OVD	signal overload detect
P24	24 V extra power supply (+)
PD	process data
PDCT	port and device configuration tool
PL	physical layer
PLC	programmable logic controller
<i>P_S</i>	power supply (measured in V)
<i>r</i>	time to reach a stable level with reference to the beginning of the start bit (measured in <i>T_{BIT}</i>)
<i>RL_{eff}</i>	loop resistance of cable (measured in Ω)
<i>s</i>	time to exit a stable level with reference to the beginning of the start bit (measured in <i>T_{BIT}</i>)
SDCI	single-drop digital communication interface
SIO	standard input output (digital switching mode) [IEC 61131-2]
SM	system management
<i>t₁</i>	UART frame transfer delay on Master (measured in <i>T_{BIT}</i>)
<i>t₂</i>	UART frame transfer delay on Device (measured in <i>T_{BIT}</i>)
<i>t_A</i>	response delay on Device (measured in <i>T_{BIT}</i>)
<i>T_{BIT}</i>	bit time (measured in s)
<i>t_{CYC}</i>	cycle time on M-sequence level (measured in s)
<i>t_{DF}</i>	fall time (measured in s)
<i>T_{DMT}</i>	delay time while establishing Master port communication (measured in <i>T_{BIT}</i>)
<i>T_{DR}</i>	rise time (measured in s)
<i>T_{DSIO}</i>	delay time on device for transition to SIO mode following wake-up request (measured in s)
<i>T_{DWU}</i>	wake-up retry delay (measured in s)
<i>t_{M-sequence}</i>	M-sequence duration (measured in <i>T_{BIT}</i>)
<i>t_{idle}</i>	idle time between two M-sequences (measured in s)
<i>t_H</i>	detection time for high level (measured in s)
<i>t_L</i>	detection time for low level (measured in s)
<i>t_{ND}</i>	noise suppression time (measured in s)
<i>T_{RDL}</i>	wake-up readiness following power ON (measured in s)
<i>T_{REN}</i>	receive enable (measured in s)

T_{SD}	device detect time (measured in s)
T_{WU}	pulse duration of wake-up request (measured in s)
UART	universal asynchronous receiver transmitter
UML	Unified Modelling Language [ISO/IEC 19505]
V_+	voltage at L+
V_0	voltage at L-
VD_{+L}	voltage drop on the line between the L+ connections on Master and Device (measured in V)
VD_{0L}	voltage drop on the line between the L- connections on Master and Device (measured in V)
VD_{QL}	voltage drop on the line between the C/Q connections on Master and Device (measured in V)
V_{HYS}	hysteresis of receiver threshold voltage (measured in V)
V_I	input voltage at connection C/Q with reference to V_0 (measured in V)
V_{IH}	input voltage range at connection C/Q for high signal (measured in V)
V_{IL}	input voltage range at connection C/Q for low signal (measured in V)
VR_Q	residual voltage on driver in saturated operating status ON (measured in V)
VR_{QH}	residual voltage on high-side driver in operating status ON (measured in V)
VR_{QL}	residual voltage on low-side driver in saturated operating status ON (measured in V)
V_{TH}	threshold voltage of receiver with reference to V_0 (measured in V)
V_{THH}	threshold voltage of receiver for safe detection of a high signal (measured in V)
V_{THL}	threshold voltage of receiver for safe detection of a low signal (measured in V)
WURQ	wake-up request pulse

3.3 Conventions

3.3.1 General

The service model, service primitives, and the diagrams shown in this standard are entirely abstract descriptions. The implementation of the services may reflect individual issues and can be different.

3.3.2 Service parameters

Service primitives are used to represent service provider/consumer interactions (ISO/IEC 10731). They convey parameters which indicate the information available in the provider/ consumer interaction. In any particular interface, not each and every parameter needs to be explicitly stated.

The service specification in this standard uses a tabular format to describe the component parameters of the service primitives. The parameters which apply to each group of service primitives are set out in tables. Each table consists of up to five columns:

- 1) parameter name;
- 2) request primitive (.req);
- 3) indication primitive (.ind);
- 4) response primitive (.rsp); and
- 5) confirmation primitive (.cnf).

One parameter (or component of it) is listed in each row of each table. Under the appropriate service primitive columns, a code is used to specify the type of usage of the parameter on the primitive specified in the column.

M Parameter is mandatory for the primitive.

U Parameter is a user option and can or cannot be provided depending on dynamic usage of the service user. When not provided a default value for the parameter is assumed.

- C Parameter is conditional upon other parameters or upon the environment of the service user.
- Parameter is never present.
- S Parameter is a selected item.

Some entries are further qualified by items in brackets. These may be:

- a) a parameter-specific constraint "(=)" indicates that the parameter is semantically equivalent to the parameter in the service primitive to its immediate left in the table;
- b) an indication that some note applies to the entry "(n)" indicates that the following note "n" contains additional information related to the parameter and its use.

3.3.3 Service procedures

The procedures are defined in terms of:

- the interactions between application entities through the exchange of protocol data units; and
- the interactions between a communication layer service provider and a communication layer service consumer in the same system through the invocation of service primitives.

These procedures are applicable to instances of communication between systems which support time-constrained communications services within the communication layers.

3.3.4 Service attributes

The nature of the different (Master and Device) services is characterized by attributes. All services are defined from the view of the affected layer towards the layer above.

- I Initiator of a service (towards the layer above)
- R Receiver (responder) of a service (from the layer above)

3.3.5 Figures

For figures that show the structure and services of protocol layers, the following conventions are used:

- an arrow with just a service name represents both a request and the corresponding confirmation, with the request being in the direction of the arrow;
- a request without confirmation, as well as all indications and responses are labelled as such (i.e. service.req, service.ind, service.rsp).

Figure 1 shows the example of a confirmed service.

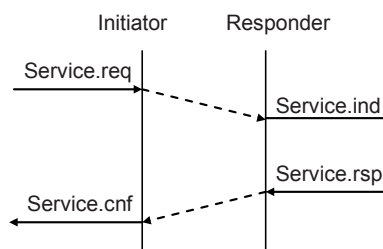
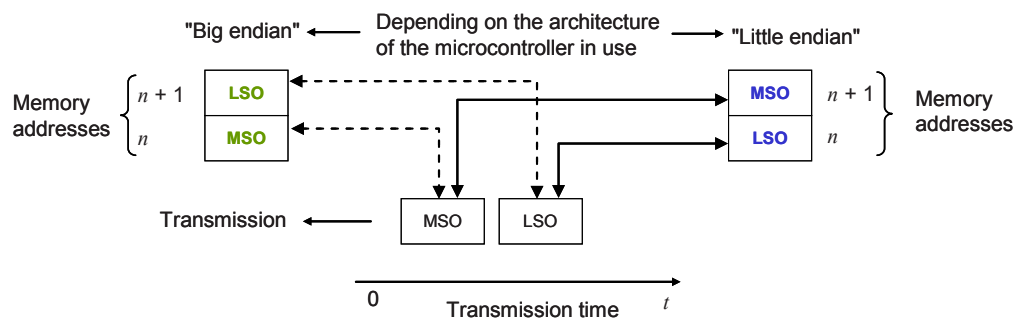


Figure 1 – Example of a confirmed service

3.3.6 Transmission octet order

Figure 2 shows how WORD based data types are transferred from memory to transmission medium and vice versa (i.e. most significant octet transmitted first, see 7.3.3.2 and 7.3.3.3).



Key

MSO = Most significant octet
LSO = Least significant octet

Figure 2 – Memory storage and transmission order for WORD based data types

3.3.7 Behavioral descriptions

For the behavioral descriptions, the notations of UML 2 (ISO/IEC 19505) are used (e.g. state, sequence, activity, timing diagrams, guard conditions). The layout of the associated state-transition tables is following IEC/TR 62390.

Due to design tool restrictions the following exceptions apply. For state diagrams, a service parameter (in capital letters) is attached to the service name via an underscore character, such as for example in DL_SetMode_INACTIVE. For sequence diagrams, the service primitive is attached via an underscore character instead of a dot, and the service parameter is added in parenthesis, such as for example in DL_Event_ind (OPERATE). Timing constraints are labelled "tm(time in ms)".

Asynchronously received service calls are not modelled in detail within state diagrams.

4 Overview of SDCl (IO-Link™⁴)

4.1 Purpose of technology

Figure 3 shows the basic concept of SDCl.

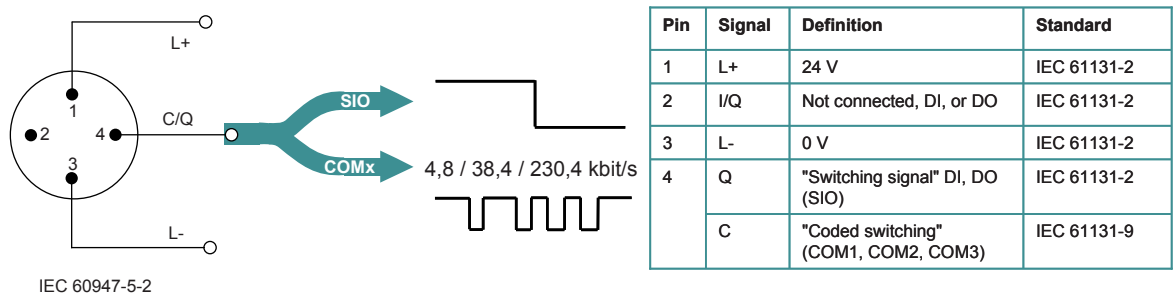


Figure 3 – SDCl compatibility with IEC 61131-2

⁴ IO-Link™ is a trade name of the "IO-Link Consortium". This information is given for the convenience of users of this international Standard and does not constitute an endorsement by IEC of the trade name holder or any of its products. Compliance to this standard does not require use of the registered logos for IO-Link™. Use of the registered logos for IO-Link™ requires permission of the "IO-Link Consortium".

The single-drop digital communication interface technology for small sensors and actuators SDCI (commonly known as IO-Link™) defines a migration path from the existing digital input and digital output interfaces for switching 24 V Devices as defined in IEC 61131-2 towards a point-to-point communication link. Thus, for example, digital I/O modules in existing fieldbus peripherals can be replaced by SDCI Master modules providing both classic DI/DO interfaces and SDCI. Analog transmission technology can be replaced by SDCI combining its robustness, parameterization, and diagnostic features with the saving of digital/analog and analog/digital conversion efforts.

4.2 Positioning within the automation hierarchy

Figure 4 shows the domain of the SDCI technology within the automation hierarchy.

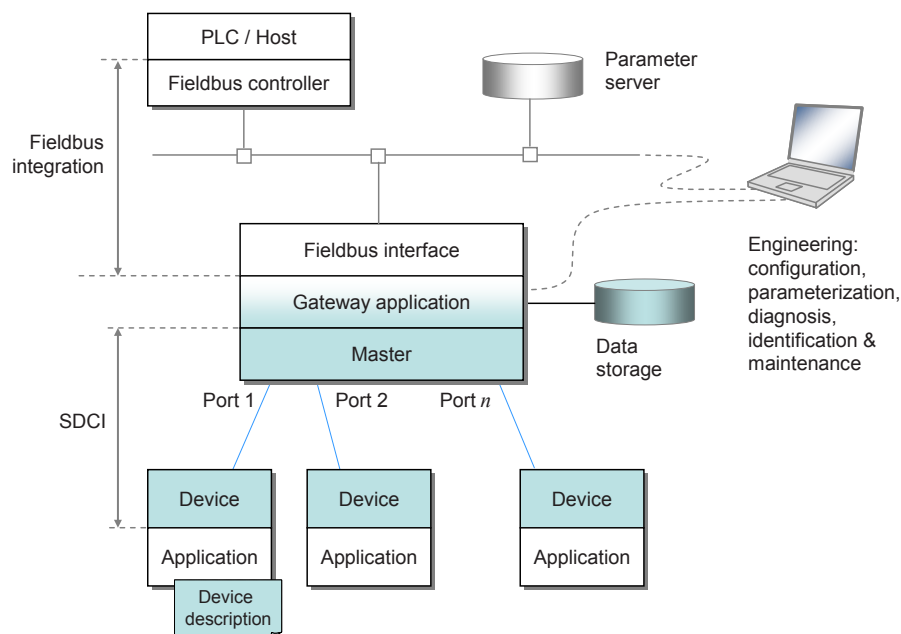


Figure 4 – Domain of the SDCI technology within the automation hierarchy

The SDCI technology defines a generic interface for connecting sensors and actuators to a Master unit, which may be combined with gateway capabilities to become a fieldbus remote I/O node.

Starting point for the design of SDCI is the classic 24 V digital input (DI) defined in IEC 61131-2 and output interface (DO) specified in Table 6. Thus, SDCI offers connectivity of classic 24 V sensors ("switching signals") as a default operational mode. Additional connectivity is provided for actuators when a port has been configured into "single-drop communication mode".

Many sensors and actuators nowadays are already equipped with microcontrollers offering a UART interface that can be extended by addition of a few hardware components and protocol software to support SDCI communication. This second operational mode uses "coded switching" of the 24 V I/O signalling line. Once activated, the SDCI mode supports parameterization, cyclic data exchange, diagnosis reporting, identification & maintenance information, and external parameter storage for Device backup and fast reload of replacement devices. Sensors and actuators with SDCI capability are referred to as "Devices" in this standard. To improve start-up performance these Devices usually provide non-volatile storage for parameters.

NOTE Configuration and parameterization of Devices is supported through an XML-based device description (see [6]), which is not part of this standard.

4.3 Wiring, connectors and power

The default connection (port class A) comprises 4 pins (see Figure 3). The default wiring for port class A complies with IEC 60947-5-2 and uses only three wires for 24 V, 0 V, and a signal line. The fourth wire may be used as an additional signal line complying with IEC 61131-2.

Five pins connections (port class B) are specified for Devices requiring additional power from an independant 24 V power supply.

NOTE A port class A Device using the fourth wire is not compatible with a port class B Master.

Maximum length of cables is 20 m, shielding is not required.

4.4 Communication features of SDCI

The generic Device model is shown in Figure 5 and explained in the following paragraphs.

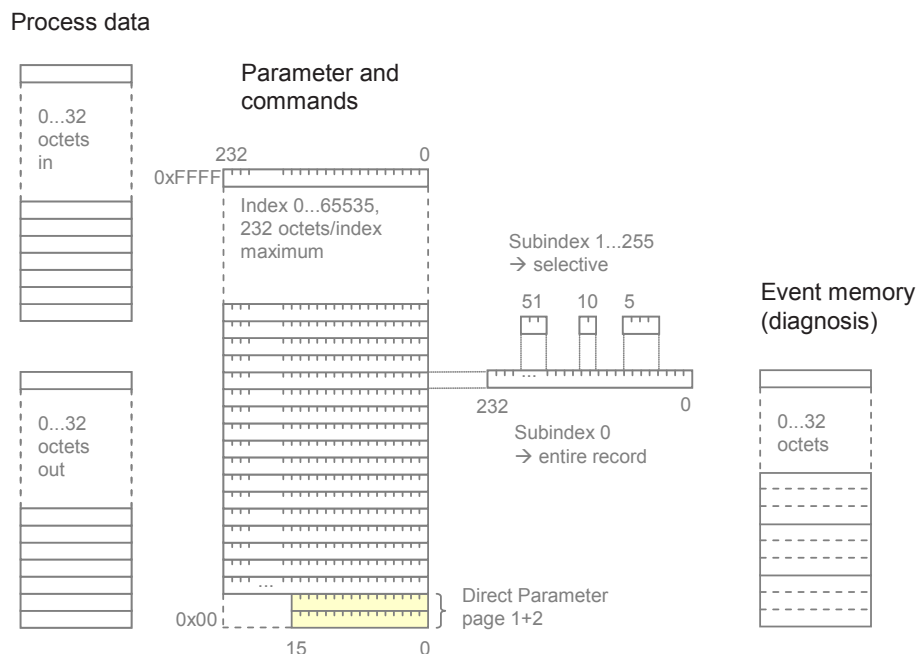


Figure 5 – Generic Device model for SDCI (Master's view)

A Device may receive Process Data (out) to control a discrete or continuous automation process or send Process Data (in) representing its current state or measurement values. The Device usually provides parameters enabling the user to configure its functions to satisfy particular needs. To support this case a large parameter space is defined with access via an Index (0 to 65 535; with a predefined organization) and a Subindex (0 to 255).

The first two index entries 0 and 1 are reserved for the Direct Parameter page 1 and 2 with a maximum of 16 octets each. Parameter page 1 is mainly dedicated to Master commands such as Device startup and fallback, retrieval of Device specific operational and identification information. Parameter page 2 allows for a maximum of 16 octets of Device specific parameters.

The other indices (2 to 65 535) each allow access to one record having a maximum size of 232 octets. Subindex 0 specifies transmission of the complete record addressed by the Index, other subindices specify transfer of selected data items within the record.

Within a record, individual data items may start on any bit offset, and their length may range from 1 bit to 232 octets, but the total number of data items in the record cannot exceed 255. The organization of data items within a record is specified in the IO Device Description (IODD).

All changes of Device condition that require reporting or intervention are stored within an Event memory before transmission. An Event flag is then set in the cyclic data exchange to indicate the existence of an Event.

Communication between a Master and a Device is point-to-point and is based on the principle of a Master first sending a request message and then a Device sending a response message (see Figure 36). Both messages together are called an M-sequence. Several M-sequence types are defined to support user requirements for data transmission (see Figure 37).

Data of various categories are transmitted through separate communication channels within the data link layer, as shown in Figure 6.

- Operational data such as Device inputs and outputs is transmitted through a process channel using cyclic transfer. Operational data may also be associated with qualifiers such as valid/invalid.
- Configuration and maintenance parameters are transmitted using acyclic transfers. A page channel is provided for direct access to parameter pages 1 and 2, and an ISDU channel is used for accessing additional parameters and commands.
- Device events are transmitted using acyclic transfers through a diagnostic channel. Device events are reported using 3 severity levels, error, warning, and notification.

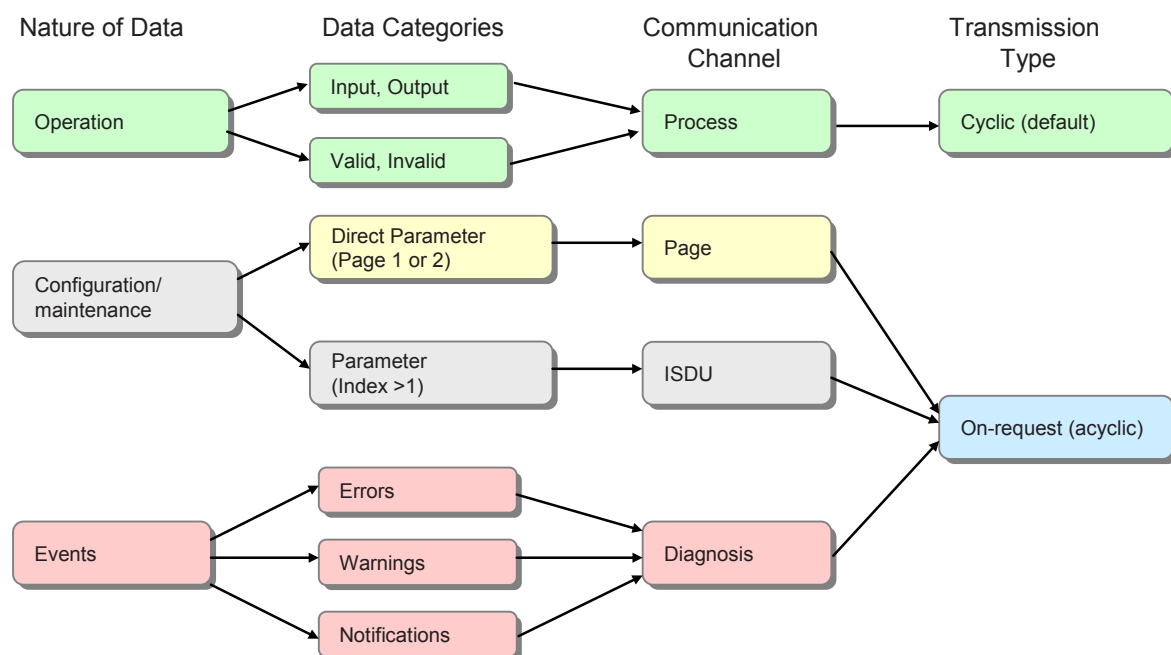


Figure 6 – Relationship between nature of data and transmission types

The first octet of a Master message controls the data transfer direction (read/write) and the type of communication channel.

Figure 7 shows each port of a Master has its own data link layer which interfaces to a common master application layer. Within the application layer, the services of the data link layer are translated into actions on Process Data objects (input/output), On-request Data objects (read/write), and events. Master applications include a Configuration Manager (CM),

Data Storage mechanism (DS), Diagnosis Unit (DU), On-request Data Exchange (ODE), and a Process Data Exchange (PDE).

System management checks identification of the connected Devices and adjusts ports and Devices to match the chosen configuration and the properties of the connected Devices. It controls the state machines in the application (AL) and data link layers (DL), for example at start-up.

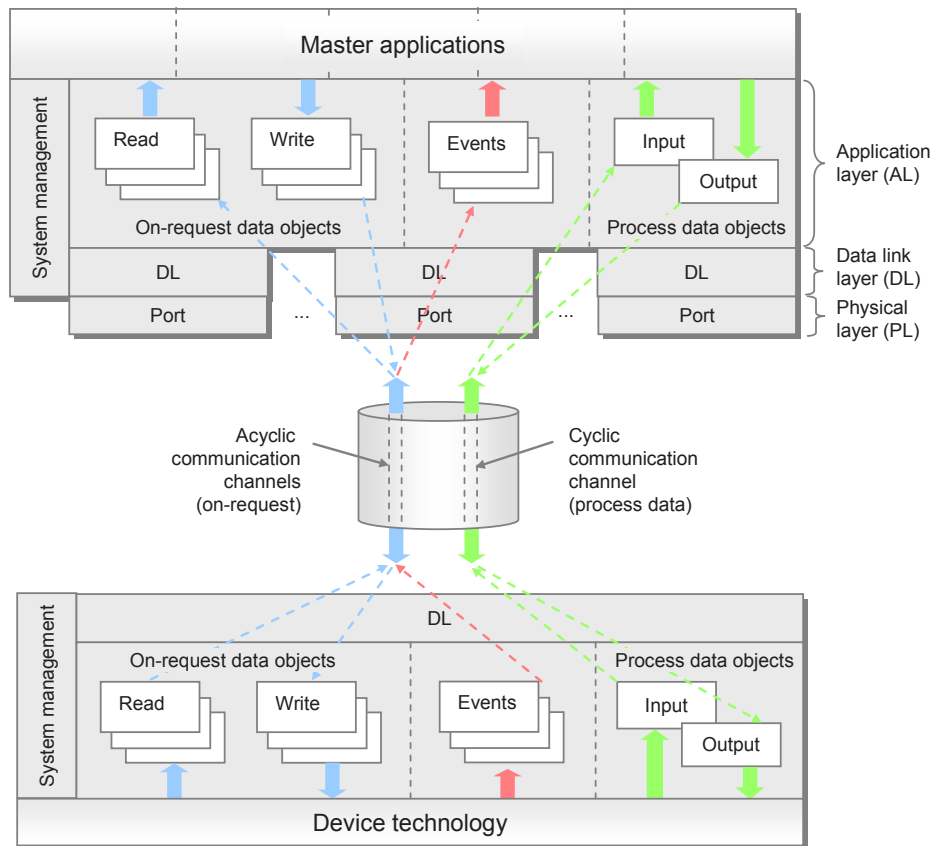


Figure 7 – Object transfer at the application layer level (AL)

4.5 Role of a Master

A Master accommodates 1 to n ports and their associated data link layers. During start-up it changes the ports to the user-selected port modes, which can be INACTIVE, DI, DO, FIXEDMODE, or SCANMODE. If communication is requested, the Master uses a special wake-up current pulse to initiate communication with the Device. The Master then auto-adjusts the transmission rate to COM1, COM2, or COM3 (see Table 8) and checks the "personality" of the connected Device, i.e. its VendorID, DeviceID, and communication properties.

If there is a mismatch between the Device parameters and the stored parameter set within the Master, the parameters in the Device are overwritten (see 11.3) or the stored parameters within the master are updated depending on configuration.

It is also possible to start a device in DI mode, switch to SDCI communication for configuration and parameterization and then use the fallback command (see 11.8.5) to switch back to DI mode for normal operation.

Coordination of the ports is also a task of the Master which the user can configure through the selection of port cycle modes. In "FreeRunning" mode, each port defines its own cycle based on the properties of the connected Device. In "MessageSync" mode, messages sent to the

connected ports start at the same time or in a defined staggered manner. In "FixedValue" mode, each port uses a user-defined fixed cycle time (see 11.2.2.2).

The Master is responsible for the assembling and disassembling of all data from or to the Devices (see Clause 11).

The Master provides a Data Storage area of at least 2 048 octets per Device for backup of Device data (see 11.3). The Master may combine this Device data together with all other relevant data for its own operation, and make this data available for higher level applications for Master backup purpose or recipe control (see 11.8.3).

4.6 SDCI configuration

Engineering support for a Master is usually provided by a Port and Device Configuration Tool (PDCT). The PDCT configures both port properties and Device properties (see parameters shown in Figure 5). It combines both an interpreter of the I/O Device Description (IODD) and a configurator (see 11.7). The IODD provides all the necessary properties to establish communication and the necessary parameters and their boundaries to establish the desired function of a sensor or actuator. The PDCT also supports the compilation of the Process Data for propagation on the fieldbus and vice versa.

4.7 Mapping to fieldbuses

Integration of a Master within a fieldbus system, i.e. the definition of gateway functions for exchanging data with higher level entities on a fieldbus, is out of the scope of this standard.

EXAMPLE These functions include mapping of the Process Data exchange, realization of program-controlled parameterization or a remote parameter server, or the propagation of diagnosis information.

The integration of a PDCT into engineering tools of a particular fieldbus is out of the scope of this standard.

4.8 Standard structure

Figure 8 shows the logical structure of the Master and Device. Clause 5 specifies the Physical Layer (PL) of SDCI, Clause 6 specifies details of the SIO mode. Clause 7 specifies Data Link Layer (DL) services, protocol, wake-up, M-sequences, and the DL layer handlers. Clause 8 specifies the services and the protocol of the Application Layer (AL) and Clause 9 the System Management responsibilities (SM).

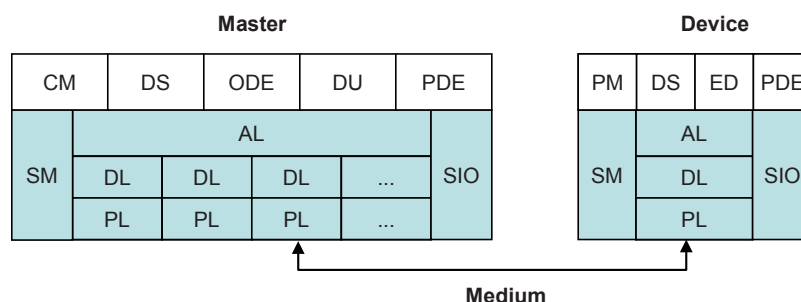


Figure 8 – Logical structure of Master and Device

Clause 10 specifies Device applications and features. These include Process Data Exchange (PDE), Parameter Management (PM), Data Storage (DS), and Event Dispatcher (ED). Technology specific applications are not part of this standard. They may be specified in profiles for particular Device families.

Clause 11 specifies Master applications and features. These include Process Data Exchange (PDE), On-request Data Exchange (ODE), Configuration Management (CM), Data Storage (DS) and Diagnosis Unit (DU).

Several normative and informative annexes are included. Annex A defines the available M-sequence types. Annex B describes the parameters of the Direct Parameter page and the fixed Device parameters. Annex C lists the error types in case of acyclic transmissions and Annex D the EventCodes (diagnosis information of Devices). Annex E specifies the available basic and composite data types. Annex F defines the structure of Data Storage objects. Annex G deals with conformity and electromagnetic compatibility test requirements and Annex H provides graphs of residual error probabilities, demonstrating the level of SDCI's data integrity. The informative Annex I provides an example of the sequence of acyclic data transmissions. The informative Annex J explains two recommended methods for detecting parameter changes in the context of Data Storage.

5 Physical Layer (PL)

5.1 General

5.1.1 Basics

The 3-wire connection system of SDCI is based on the specifications in IEC 60947-5-2. The three lines are used as follows: (L+) for the 24 V power supply, (L-) for the ground line, and (C/Q) for the switching signal (Q) or SDCI communication (C), as shown in Figure 9.

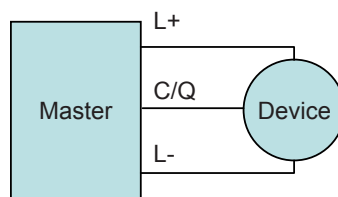


Figure 9 – Three wire connection system

NOTE 1 Binary sensors compliant with IEC 60947-5-2 are compatible with the SDCI 3-wire connection system (including from a power consumption point of view).

Support of the SDCI 3-wire connection system is mandatory for Master. Ports with this characteristic are called port class A.

Port class A uses a four pin connector. The fourth wire may be used as an additional signal line complying with IEC 61131-2. Its support is optional in both Masters and Devices.

Five wire connections (port class B) are specified for Devices requiring additional power from an independant 24 V power supply (see 5.5.1).

NOTE 2 A port class A Device using the fourth wire is not compatible with a port class B Master.

5.1.2 Topology

The SDCI system topology uses point-to-point links between a Master and its Devices as shown in Figure 10. The Master may have multiple ports for the connection of Devices. Only one Device shall be connected to each port.

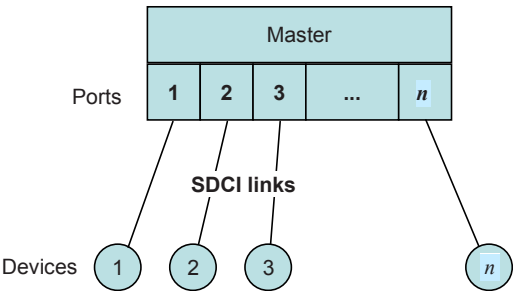


Figure 10 – Topology of SDCI

5.2 Physical layer services

5.2.1 Overview

Figure 11 shows an overview of the Master's physical layer and its service primitives.

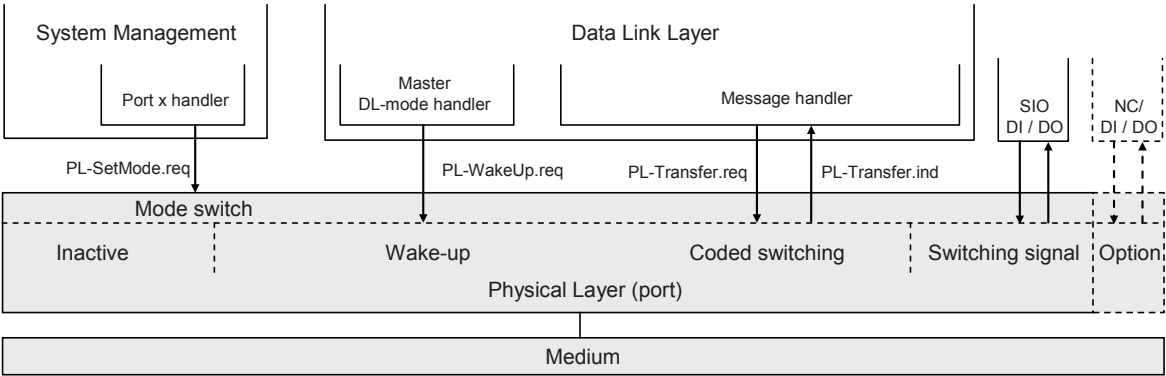


Figure 11 – Physical layer (Master)

The physical layer specifies the operation of the C/Q line in Figure 3 and the associated line driver (transmitter) and receiver of a particular port. The Master operates this line in three main modes (see Figure 11): inactive, "Switching signal" (DI/DO), or "Coded switching" (COMx). The service PL-SetMode.req is responsible for switching into one of these modes.

If the port is in inactive mode, the C/Q line shall be high impedance (floating). In SIO mode, the port can be used as a standard input or output interface according to the definitions of IEC 61131-2 or in Table 6 respectively. The communication layers of SDCI are bypassed as shown in Figure 11; the signals are directly processed within the Master application. In SDCI mode, the service PL_WakeUp.req creates a special signal pattern (current pulse) that can be detected by an SDCI enabled Device connected to this port (see 5.3.3.3).

Figure 12 shows an overview of the Device's physical layer and its service primitives.

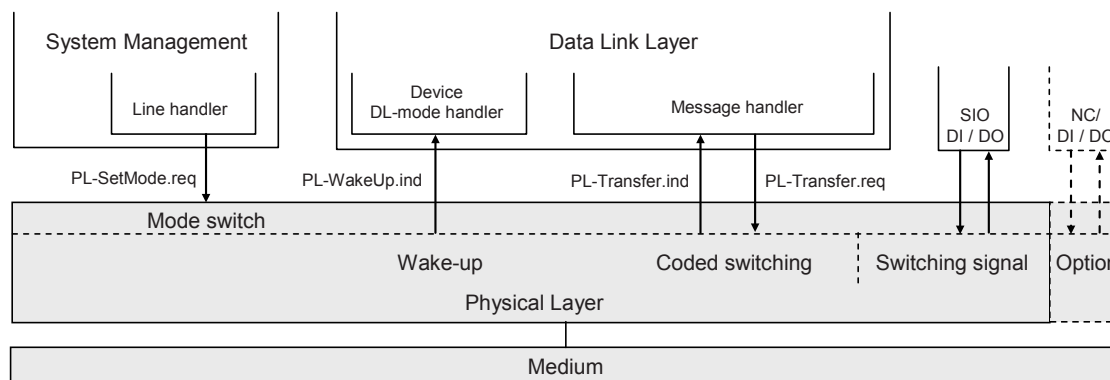


Figure 12 – Physical layer (Device)

The physical layer of a Device according to Figure 12 follows the same principle, except that there is no inactive state. By default at power on or cable reconnection, the Device shall operate in the SIO mode, as a digital input. The Device shall always be able to detect a wake-up current pulse (wake-up request). The service `PL_WakeUp.ind` reports successful detection of the wake-up request (usually a microcontroller interrupt), which is required for the Device to switch to the SDCI mode.

A special MasterCommand (fallback) sent via SDCI causes the Device to switch back to SIO mode.

Subsequently, the services are specified that are provided by the PL to System Management and to the Data Link Layer (see Figure 83 and Figure 94 for a complete overview of all the services). Table 1 lists the assignments of Master and Device to their roles as initiator or receiver for the individual PL services.

Table 1 – Service assignments of Master and Device

Service name	Master	Device
PL-SetMode	R	R
PL-WakeUp	R	I
PL-Transfer	I / R	R / I
Key (see 3.3.4) I Initiator of service R Receiver (Responder) of service		

5.2.2 PL services

5.2.2.1 PL_SetMode

The `PL-SetMode` service is used to setup the electrical characteristics and configurations of the Physical Layer. The parameters of the service primitives are listed in Table 2.

Table 2 – PL_SetMode

Parameter name	.req
Argument	M
TargetMode	M

Argument

The service-specific parameters of the service request are transmitted in the argument.

TargetMode

This parameter indicates the requested operation mode

Permitted values:

INACTIVE (C/Q line in high impedance),
 DI (C/Q line in digital input mode),
 DO (C/Q line in digital output mode),
 COM1 (C/Q line in COM1 mode),
 COM2 (C/Q line in COM2 mode),
 COM3 (C/Q line in COM3 mode)

5.2.2.2 PL_WakeUp

The PL-WakeUp service initiates or indicates a specific sequence which prepares the Physical Layer to send and receive communication requests (see 5.3.3.3). This unconfirmed service has no parameters. Its success can only be verified by a Master by attempting to communicate with the Device. The service primitives are listed in Table 3.

Table 3 – PL_WakeUp

Parameter name	.req	.ind
<none>		

5.2.2.3 PL_Transfer

The PL-Transfer service is used to exchange the SDCI data between Data Link Layer and Physical Layer. The parameters of the service primitives are listed in Table 4.

Table 4 – PL_Transfer

Parameter name	.req	ind.
Argument		
Data	M	M
Result (+)		S
Result (-)		S
Status		M

Argument

The service-specific parameters of the service request are transmitted in the argument.

Data

This parameter contains the data value which is transferred over the SDCI interface.

Permitted values: 0...255

Result (+):

This selection parameter indicates that the service request has been executed successfully.

Result (-):

This selection parameter indicates that the service request failed.

Status

This parameter contains supplementary information on the transfer status.

Permitted values:	
PARITY_ERROR	(UART detected a parity error),
FRAMING_ERROR	(invalid UART stop bit detected),
OVERRUN	(octet collision within the UART)

5.3 Transmitter/Receiver

5.3.1 Description method

The physical layer is specified by means of electrical and timing requirements. Electrical requirements specify signal levels and currents separately for Master and Device in the form of reference schematics. Timing requirements specify the signal transmission process (specifically the receiver) and a special signal detection function.

5.3.2 Electrical requirements

5.3.2.1 General

The line driver is specified by a reference schematic corresponding to Figure 13. On the Master side, a transmitter comprises a combination of two line drivers and one current sink. On the Device side, in its simplest form, the transmitter takes the form of a p-switching driver. As an option there can be an additional n-switching or non-switching driver (this also allows the option of push-pull output operation).

In operating status ON the descriptive variables are the residual voltage VRQ , the standard driver current IQ , and the peak current $IQPK$. The source is controlled by the On/Off signal. An overload current event is indicated at the "Overload" output (OVD). This feature can be used for the current pulse detection (wake-up).

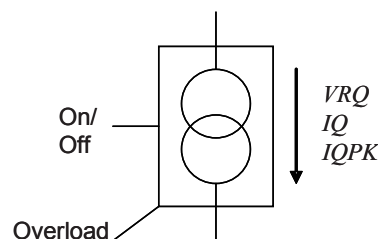


Figure 13 – Line driver reference schematics

The receiver is specified by a reference schematic according to Figure 14. It performs the function of a comparator and is specified by its switching thresholds VTH and a hysteresis $VHYS$ between the switching thresholds. The output indicates the logic level (High or Low) at the receiver input.

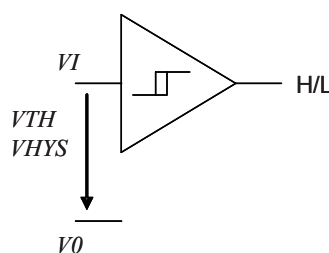
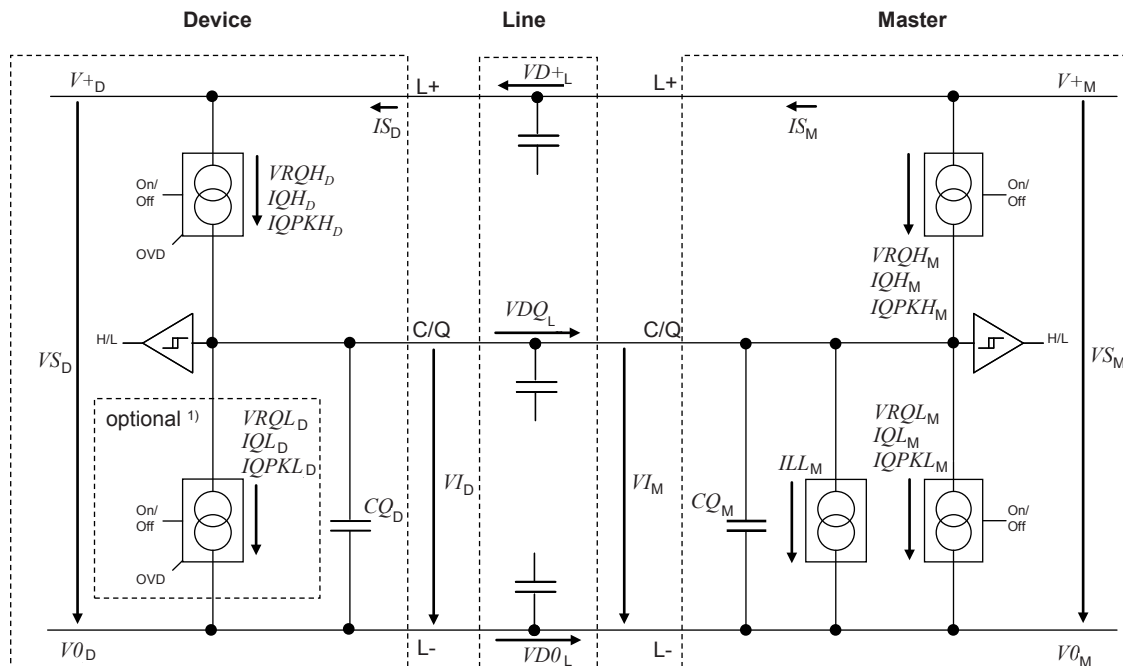


Figure 14 – Receiver reference schematics

Figure 15 shows the reference schematics for the interconnection of Master and Device for the SDCI 3-wire connection system.



1) Optional: low-side driver (push-pull only)

Figure 15 – Reference schematics for SDCI 3-wire connection system

The subsequent illustrations and parameter tables refer to the voltage level definitions in Figure 16. The parameter indices refer to the Master (M), Device (D) or line (L). The voltage drops on the line $VD+_{\text{L}}$, VDQ_{L} and $VD0_{\text{L}}$ are implicitly specified in 5.5 through cable parameters.

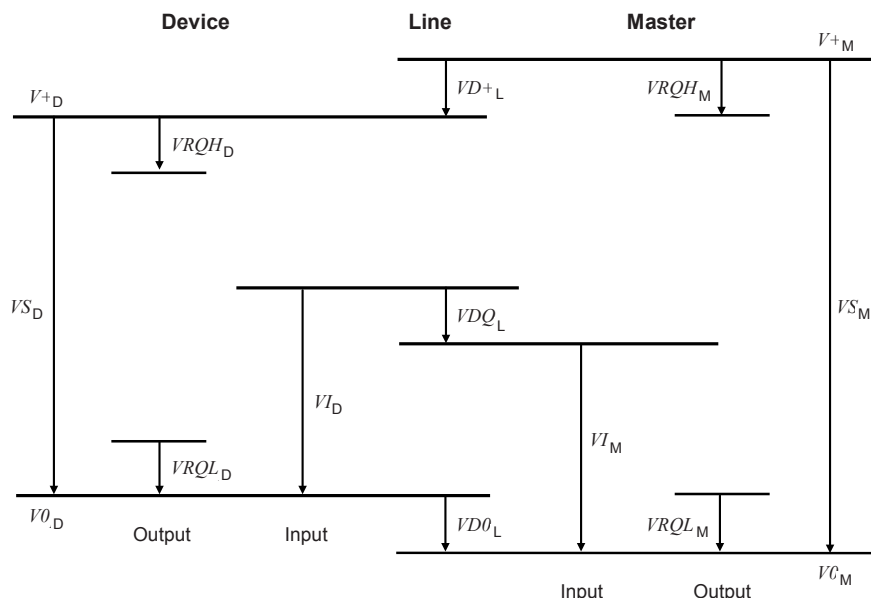


Figure 16 – Voltage level definitions

5.3.2.2 Receiver

The voltage range and switching threshold definitions are the same for Master and Device. The definitions in Table 5 apply.

Table 5 – Electric characteristics of a receiver

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
$V_{THH_{D,M}}$	Input threshold 'H'	10,5	n/a	13	V	See NOTE 1
$V_{THL_{D,M}}$	Input threshold 'L'	8	n/a	11,5	V	See NOTE 1
$V_{HYS_{D,M}}$	Hysteresis between input thresholds 'H' and 'L'	0	n/a	n/a	V	Shall not be negative See NOTE 2
$V_{IL_{D,M}}$	Permissible voltage range 'L'	$V_{0_{D,M}} - 1,0$	n/a	n/a	V	With reference to relevant negative supply voltage
$V_{IH_{D,M}}$	Permissible voltage range 'H'	n/a	n/a	$V^+_{D,M} + 1,0$	V	With reference to relevant positive supply voltage.

NOTE 1 Thresholds are compatible with the definitions of type 1 digital inputs in IEC 61131-2.
NOTE 2 Hysteresis voltage $V_{HYS} = V_{THH} - V_{THL}$.

Figure 17 demonstrates the switching thresholds for the detection of Low and High signals.

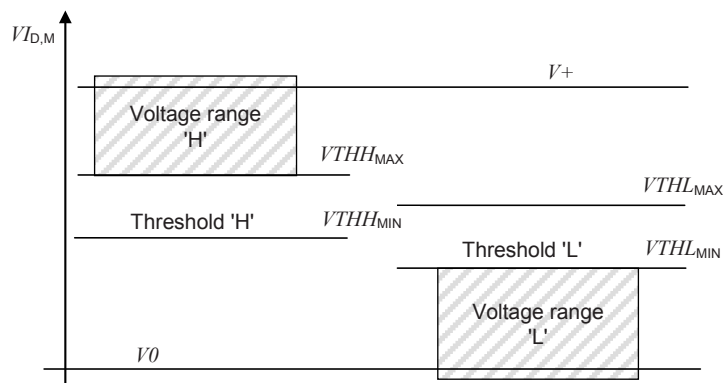


Figure 17 – Switching thresholds

5.3.2.3 Master port

The definitions in Table 6 are valid for the electric characteristics of a Master port.

Table 6 – Electric characteristics of a Master port

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
V_{S_M}	Supply voltage for Devices	20	24	30	V	See Figure 16
I_{S_M}	Supply current for Devices	200	n/a	n/a	mA	External supply required for > 200 mA
I_{SIR_M}	Current pulse capability for Devices	400	n/a	n/a	mA	Master supply current capability for a minimum of 50 ms at 18 V after power-on of the port supply

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
ILL_M	Load or discharge current for $0\text{ V} < V_{I_M} < 5\text{ V}$ $5\text{ V} < V_{I_M} < 15\text{ V}$ $15\text{ V} < V_{I_M} < 30\text{ V}$	0 5 5	n/a n/a n/a	15 15 15	mA mA mA	See NOTE 1
$VRQH_M$	Residual voltage 'H'	n/a	n/a	3	V	Voltage drop relating to V_{+M} at maximum driver current IQH_M
$VRQL_M$	Residual voltage 'L'	n/a	n/a	3	V	Voltage drop relating to V_{0M} at maximum driver current IQL_M
IQH_M	DC driver current 'H'	100	n/a	n/a	mA	
$IQPKH_M$	Output peak current 'H'	500	n/a	n/a	mA	Absolute value See NOTE 2
IQL_M	DC driver current 'L'	100	n/a	n/a	mA	
$IQPKL_M$	Output peak current 'L'	500	n/a	n/a	mA	Absolute value See NOTE 2
CQ_M	Input capacitance	n/a	n/a	1,0	nF	$f=0\text{ MHz to }4\text{ MHz}$
NOTE 1 Currents are compatible with the definition of type 1 digital inputs in IEC 61131-2. However, for the range $5\text{ V} < V_{I_M} < 15\text{ V}$, the minimum current is 5 mA instead of 2 mA in order to achieve short enough slew rates for pure p-switching Devices.						
NOTE 2 Wake-up request current (5.3.3.3).						

5.3.2.4 Device

The definitions in Table 7 are valid for the electric characteristics of a Device.

Table 7 – Electric characteristics of a Device

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
VS_D	Supply voltage	18	24	30	V	See Figure 16
ΔVS_D	Ripple	n/a	n/a	1,3	V _{pp}	Peak-to-peak absolute value limits shall not be exceeded. $f_{\text{ripple}} = \text{DC to } 100\text{ kHz}$
$VRQH_D$	Residual voltage 'H'	n/a	n/a	3	V	Voltage drop compared with V_{+D} (IEC 60947-5-2)
$VRQL_D$	Residual voltage 'L'	n/a	n/a	3	V	Voltage drop compared with V_{0D}
IQH_D	DC driver current P-switching output ("On" state)	50	n/a	minimum ($IQPKL_M$)	mA	Minimum value due to fallback to digital input in accordance with IEC 61131-2, type 2
IQL_D	DC driver current N-switching output ("On" state)	0	n/a	minimum ($IQPKH_M$)	mA	Only for push-pull output stages
IQQ_D	Quiescent current to V_{0D} ("Off" state)	0	n/a	15	mA	Pull-down or residual current with deactivated output driver stage

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
CQ_D	Input capacitance	0	n/a	1,0	nF	Effective capacitance between C/Q and L+ or L- of Device in receive state

The value of 1 nF is applicable for a transmission rate of 230,4 kbit/s. Input capacitance CQ_D may be relaxed to a maximum of 10 nF in the case of push-pull stage design when operating at lower transmission rates, provided that all dynamic parameter requirements in 5.3.3.2 are met.

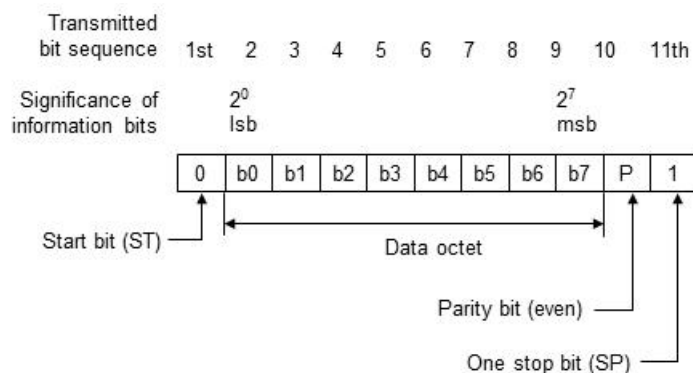
5.3.3 Timing requirements

5.3.3.1 Transmission method

The “Non Return to Zero” (NRZ) modulation is used for the bit-by-bit coding. A logic value “1” corresponds to a voltage difference of 0 V between the C/Q line and L- line. A logic value “0” corresponds to a voltage difference of +24 V between the C/Q line and L- line.

The open-circuit level on the C/Q line is 0 V with reference to L-. A start bit has logic value “0”, i.e. +24 V with reference to L-.

A UART frame is used for the "data octet"-by-"data octet" coding. The format of the SDCI UART frame is a bit string structured as shown in Figure 18.



Key:
lsb least significant bit
msb most significant bit

Figure 18 – Format of an SDCI UART frame

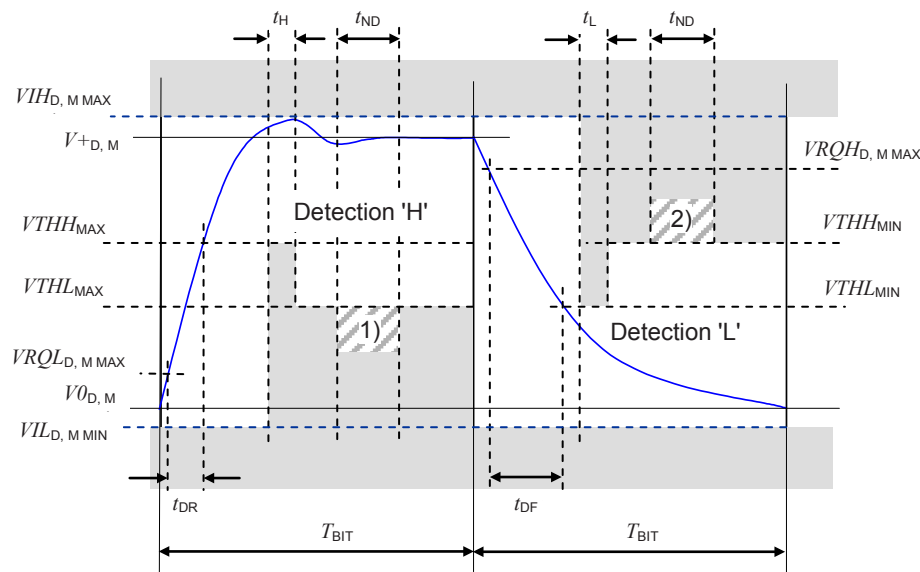
The definition of the UART frame format is based on ISO 1177 and ISO/IEC 2022.

5.3.3.2 Transmission characteristics

The timing characteristics of transmission are demonstrated in the form of an eye diagram with the permissible signal ranges (see Figure 19). These ranges are applicable for receiver in both the Master and the Device.

Regardless of boundary conditions, the transmitter shall generate a voltage characteristic on the receiver's C/Q connection that is within the permissible range of the eye diagram.

The receiver shall detect bits as a valid signal shape within the permissible range of the eye diagram on the C/Q connection. Signal shapes in the “no detection” areas (below V_{THL_MAX} or above V_{THH_MIN} and within t_{ND}) shall not lead to invalid bits.



NOTE In the figure, 1) = no detection "L"; and 2) = no detection "H"

Figure 19 – Eye diagram for the 'H' and 'L' detection

In order for a UART frame to be detected correctly, a signal characteristic as demonstrated in Figure 20 is required on the receiver side. The signal delay time between the C/Q signal and the UART input shall be taken into account. Time T_{BIT} always indicates the receiver's bit rate.

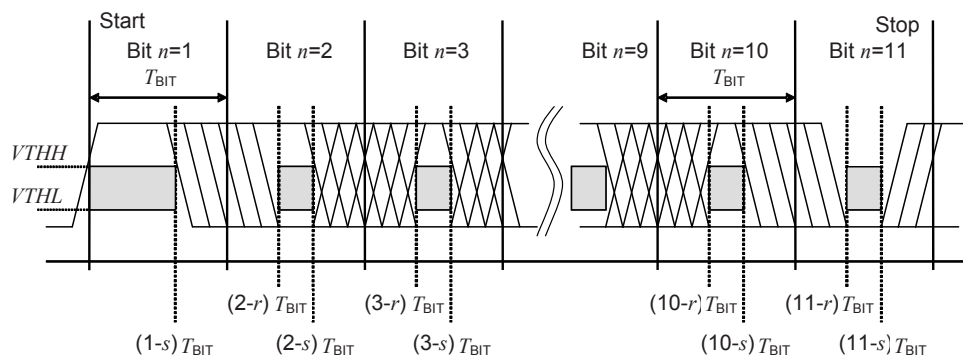


Figure 20 – Eye diagram for the correct detection of a UART frame

For every bit n in the bit sequence ($n = 1 \dots 11$) of a UART frame, the time $(n-r)T_{BIT}$ (see Table 8 for values of r) designates the time at the end of which a correct level shall be reached in the 'H' or 'L' ranges as demonstrated in the eye diagram in Figure 19. The time $(n-s)T_{BIT}$ (see Table 8 for values of s) describes the time, which shall elapse before the level changes. Reference shall always be made to the eye diagram in Figure 19, where signal characteristics within a bit time are concerned.

This representation permits a variable weighting of the influence parameters "transmission rate accuracy", "bit-width distortion", and "slew rate" of the receiver.

Table 8 specifies the dynamic characteristics of the transmission.

Table 8 – Dynamic characteristics of the transmission

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
f_{DTR}	transmission rate	n/a	4,8 38,4 230,4	n/a	kbit/s	COM1 COM2 COM3
T_{BIT}	Bit time at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s		208,33 26,04 4,34		μ s μ s μ s	
Δf_{DTRM}	Master transmission rate accuracy at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s	-0,1 -0,1 -0,1	n/a n/a n/a	+0,1 +0,1 +0,1	% % %	Tolerance of the transmission rate of the Master $\Delta T_{BIT}/T_{BIT}$
r	Start of detection time within a bit with reference to the raising edge of the start bit	0,65	n/a	n/a	-	Calculated in each case from the end of a bit at a UART sampling rate of 8
s	End of detection time within a bit with reference to the raising edge of the start bit	n/a	n/a	0,22	-	Calculated in each case from the end of a bit at a UART sampling rate of 8
T_{DR}	Rise time at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s	0 0 0 0	n/a n/a n/a n/a	0,20 41,7 5,2 869	T_{BIT} μ s μ s ns	With reference to the bit time unit
t_{DF}	Fall time at 4,8 kbit/s at 38,4 kbit/s at 230,4 kbit/s	0 0 0 0	n/a n/a n/a n/a	0,20 41,7 5,2 869	T_{BIT} μ s μ s ns	With reference to the bit time unit
t_{ND}	Noise suppression time	n/a	n/a	1/16	T_{BIT}	Permissible duration of a receive signal above/below the detection threshold without detection taking place
t_H	Detection time High	1/16	n/a	n/a	T_{BIT}	Duration of a receive signal above the detection threshold for 'H' level
t_L	Detection time Low	1/16	n/a	n/a	T_{BIT}	Duration of a receive signal below the detection threshold for 'H' level

The parameters 'r' and 's' apply to the respective Master or Device receiver side. This definition allows for a more flexible definition of oscillator accuracy, bit distortion and slewrate on the Device side. The over-all bit-width distortion on the last bit of the UART frame shall provide a correct level in the range of Figure 20.

5.3.3.3 Wake-up current pulse

The wake-up feature is used to request that a Device goes to the COMx mode.

A service call (PL_WakeUp.req) from the DL initiates the wake-up process (see 5.2.2.2).

The wake-up request (WURQ) starts with a current pulse induced by the Master (port) for a time T_{WU} . The wake-up request comprises the following phases (see Figure 21).

- a) Injection of a current $I_{Q_{WU}}$ by the Master depending on the level of the C/Q connection. For an input signal equivalent to logic “1” this is a current source; for an input signal equivalent to logic “0” this is a current sink.
- b) Delay time of the Device until it is ready to receive.

The wake-up request pulse can be detected by the Device through a voltage change on the C/Q line or evaluation of the current of the respective driver element within the time T_{WU} . Figure 21 shows examples for Devices with low output power.

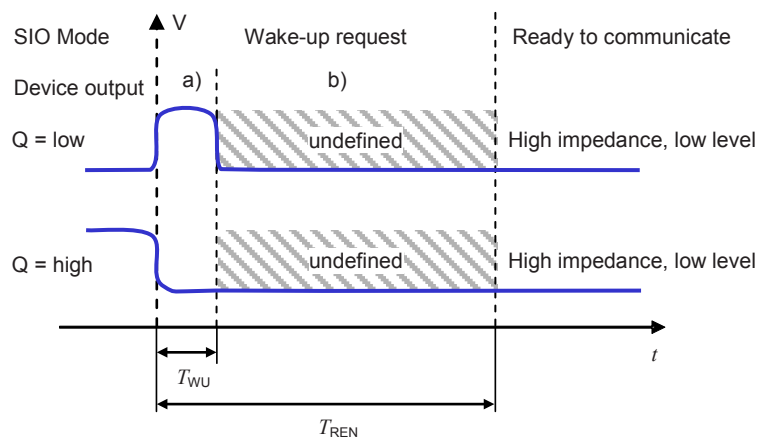


Figure 21 – Wake-up request

Table 9 specifies the current and timing properties associated with the wake-up request. See Table 6 for values of I_{QPKL_M} and I_{QPKH_M} .

Table 9 – Wake-up request characteristics

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
$I_{Q_{WU}}$	Amplitude of Master's wake-up current pulse	I_{QPKL_M} or I_{QPKH_M}	n/a	n/a	mA	Current pulse followed by switching status of Device
T_{WU}	Duration of Master's wake-up current pulse	75	n/a	85	μs	Master property
T_{REN}	Receive enable delay	n/a	n/a	500	μs	Device property

5.4 Power supply

5.4.1 Power supply options

The SDCI connection system provides dedicated power lines in addition to the signal line. The communication section of a Device shall always be powered by the Master using the power lines defined in the 3-wire connection system (Power1).

The maximum supply current available from a Master port is specified in Table 6.

The application part of the device may be powered in one of three ways:

- via the power lines of the SDCI 3-wire connection system (class A ports), using Power1;
- via the extra power lines of the SDCI 5-wire connection system (class B ports), using an extra power supply at the Master (Power2);

- via a local power supply at the Device (design specific).

Port class A allows power consumption of up to 200 mA, as specified in Table 6. Maximum power consumption on port class B depends on the selected connection method. M12 only allows up to an extra 3,5 A.

5.4.2 Power-on requirements

Figure 22 shows how the power-on behavior of a Device is defined by the ramp-up time of the Power1 supply and by the Device internal time to get ready for the wake-up operation.

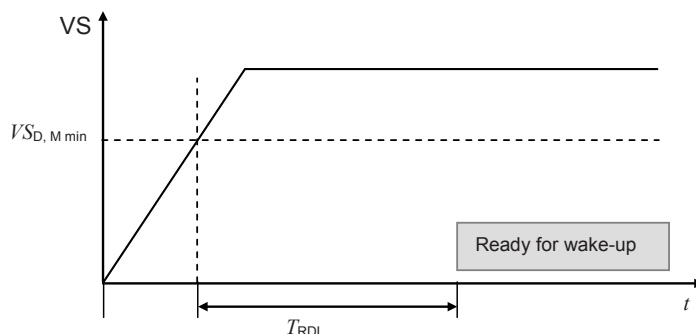


Figure 22 – Power-on timing for Power1

Upon power-on it is mandatory for a Device to reach the wake-up ready state within the time limits specified in Table 10.

Table 10 – Power-on timing

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
T_{RDL}	Wake-up readiness following power-on	n/a	n/a	300	ms	Device ramp-up time until it is ready for wake-up signal detection (See NOTE)
NOTE Equivalent to the time delay before availability in IEC 60947-5-2.						

5.5 Medium

5.5.1 Connectors

The Master and Device pin assignment is based on the specifications in IEC 60947-5-2, with extensions specified in the paragraphs below. Ports class A use M5, M8, and M12 connectors, with a maximum of four pins. Ports class B only use M12 connectors with 5 pins. M12 connectors are mechanically A-coded according to IEC 61076-2-101.

NOTE For legacy or compatibility reasons, direct wiring or different types of connectors can be used instead, provided that they do not violate the electrical characteristics and use signal naming specified in this standard.

Female connectors are assigned to the Master and male connectors to the Device. Table 11 lists the pin assignments and Figure 23 shows the layout and mechanical coding for M12, M8, and M5 connections.

Table 11 – Pin assignments

Pin	Signal	Designation	Remark
1	L+	Power supply (+)	See Table 7
2	I/Q P24	NC/DI/DO (port class A) P24 (port class B)	Option 1: NC (not connected) Option 2: DI Option 3: DI, then configured DO Option 4: Extra power supply for power Devices (port class B)
3	L-	Power supply (-)	See Table 7
4	C/Q	SIO/SDCI	Standard I/O mode (DI/DO) or SDCI (see Table 6 for electrical characteristics of DO).
5	NC N24	NC (port class A) N24 (port class B)	Option 1: Shall not be connected on the Master side (port class A). Option 2: Reference to the extra power supply (port class B)
NOTE M12 is always a 5 pin version on the Master side (female).			

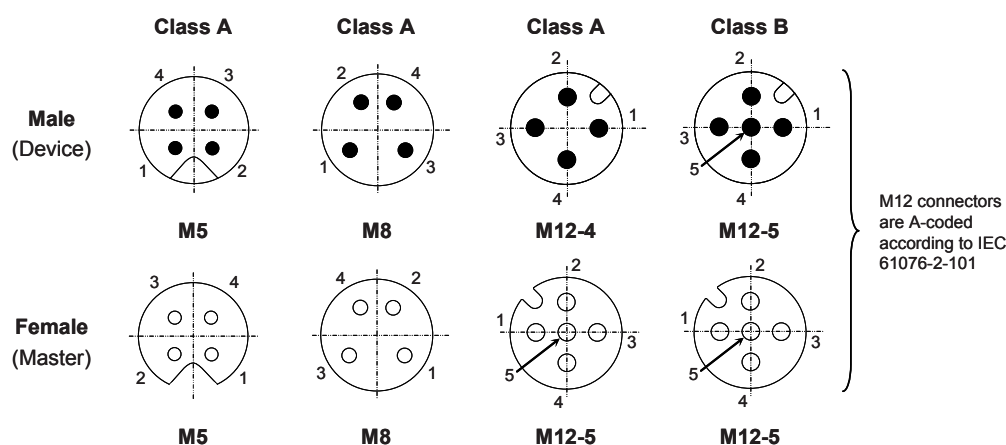


Figure 23 – Pin layout front view

Figure 24 shows the layout of the two port classes A and B. Class B ports shall be marked to distinguish them from Class A ports, because of risks deriving from incompatibilities.

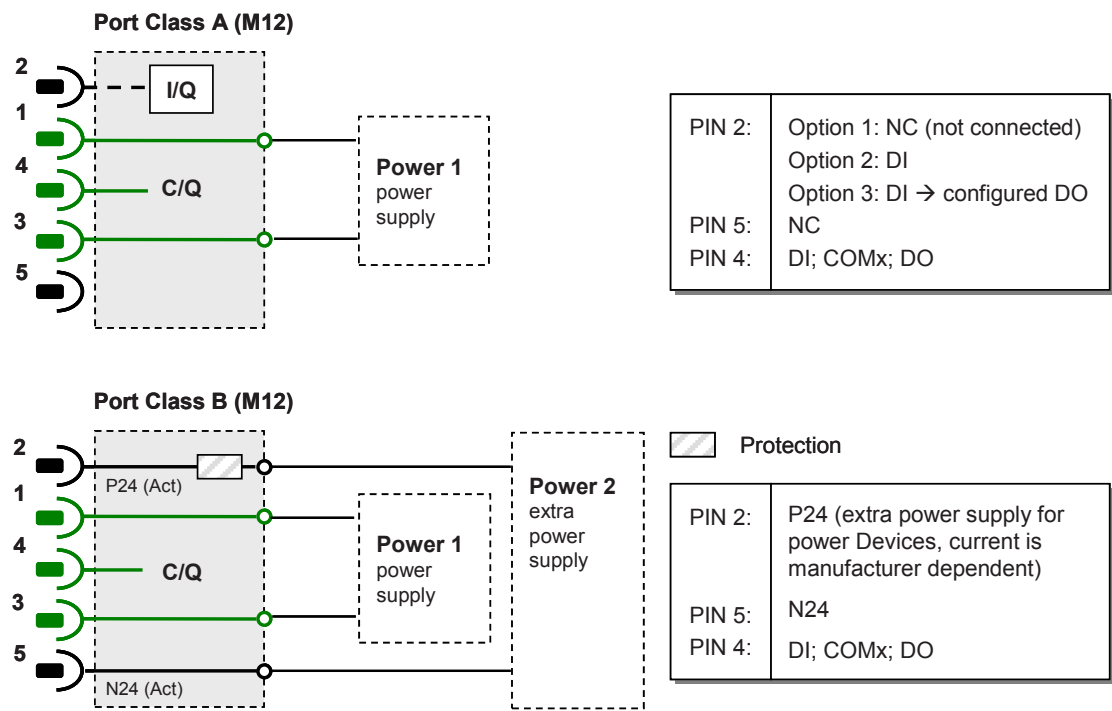


Figure 24 – Class A and B port definitions

5.5.2 Cable

The transmission medium for SDCI communication is a multi-wired cable with 3 or more wires. The definitions in the following paragraphs implicitly cover the static voltage definitions in Table 5 and Figure 16. To ensure functional reliability, the cable properties shall comply with Table 12.

Table 12 – Cable characteristics

Property	Minimum	Typical	Maximum	Unit
Length	0	n/a	20	m
Overall loop resistance RL_{eff}	n/a	n/a	6,0	Ω
Effective line capacitance CL_{eff}	n/a	n/a	3,0	nF (<1 MHz)

The loop resistance RL_{eff} and the effective line capacitance CL_{eff} may be measured as demonstrated in Figure 25.

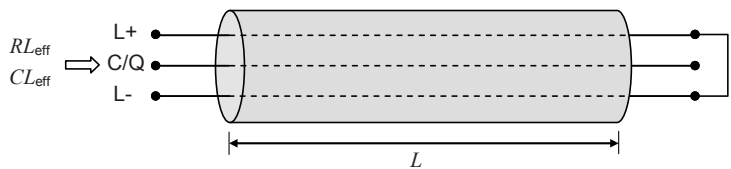


Figure 25 – Reference schematic for effective line capacitance and loop resistance

Table 13 shows the cable conductors and their assigned color codes.