

Printed boards and printed board assemblies — Design and use —

Part 1-2: Generic requirements — Controlled impedance

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National foreword

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Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, the EN title page, pages 2 to 33 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

Amendments issued since publication

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European Committee for Electrotechnical Standardization
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Foreword

The text of document 52/758/FDIS, future edition 1 of IEC 61188-1-2, prepared by IEC TC 52, Printed circuits, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61188-1-2 on 1998-08-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1999-05-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2001-05-01

Annexes designated “normative” are part of the body of the standard.

Annexes designated “informative” are given for information only.

In this standard, Annex ZA is normative and Annex A is informative.

Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61188-1-2:1998 was approved by CENELEC as a European Standard without any modification.

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Introduction

Packaging of electronic equipment has traditionally been an area for mechanical considerations. Packaging design is becoming more complex as today's electronics technologies are available in greater switching speed and higher density per chip. Individual chips have greater numbers of connections in smaller chip package sizes. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. Controlled impedance printed boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily have been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor and with interconnections specified in wire listing or net lists. Electrical conductors for signal transmission were routed with only a few concerns, that continuity was maintained between points, conductors had sufficient copper for the current and clearance was maintained to prevent voltage breakdown. Aside from providing a good electrical path, the electrical performance of the signal was not a major concern.

Advances in digital integrated circuits introduce new devices with extremely fast rise times which are housed in high density microelectronic packages. In order to optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance.

While many system problems are associated with high speed digital processing, none has received more attention than interconnection. It is evident that as system speeds increase, interconnection, packaging, and printed boards become the bottlenecks that slow system performance. Systems using 100 K ECL circuitry have almost 55 % of the system delay in the packaging and interconnect. CMOS is normally considered a "slow" technology, but is designed into system clock rates in excess of 100 MHz. In these cases, not only is system delay a problem but signal attenuation becomes an issue with the low powered, low voltage, lower noise margin BiCMOS devices.

1 Scope

This part of IEC 61188 is intended to be used by circuit designers, packaging engineers, printed board manufacturers and procurement personnel so that all may have a common understanding of each area. The aim in packaging is to transfer a signal from one device to one or more other devices through a conductor. High-speed designs are defined as designs in which the interconnecting properties affect circuit performance and require unique considerations.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 61188. At the time of publication, the editions indicated were valid. All normative documents are subject to revision, and parties to agreements based on this part of IEC 61188 are encouraged to investigate the possibility of applying the most recent editions of the normative documents listed below. Members of IEC and ISO maintain registers of currently valid international standards.

IEC 61182 (all parts), *Printed boards — Electronic data description and transfer*.

IEC 61182-1:1994, *Printed boards — Electronic data description and transfer — Part 1: Printed board description in digital form*.

IEC 61189-3:1997, *Test methods for electrical materials, interconnection structures and assemblies — Part 3: Test methods for interconnection structures (printed boards)*.

3 Engineering design overview

3.1 Device selection

Device technology options include TTL, Schottky TTL, CMOS, ECL and GaAs, each with its own set of power requirements, operating temperature range, density of chip, input impedance, output impedance, signal threshold levels, noise sensitivity, response time and output pulse rise/fall time. Many designs will have mixed technology where SMT and through hole packaging is intermixed with TTL, CMOS and ECL logic that may require multiple line widths (impedance values) on the same circuit layer or may compromise on a single conductor width that can provide enough margin for the different logic families.

Chips can be individually mounted on a large board or assembled into small boards or multichip modules mounted onto large boards. Large systems may require several large board assemblies with another level of interconnection. Noise, timing, and signal degradation will accompany transitions from one packaging level to the next.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert through plated holes in the board, as in dual in-line packages, to a series of lands for surface mount devices. Requirements for component packaging are dependent on many factors including space, economics, electrical performance and reliability, as well as the predominant packaging style of the assembly. The components shall be provided in a style that is compatible with the assembly processes used to manufacture the printed board assembly.

The component package shall be considered when designing for high speed. In passive components the predominant factor will be the lead length as leads provide additional inductance and capacitance that will affect propagation speed and switching transients. To minimize these effects the leads may be as short as possible or removed. Surface mount devices can provide leadless packages which can be directly mounted to the interconnecting substrate.

NOTE Component data sheets often do not provide parasitic values for high speed noise and propagation speed consideration.

Active devices, components such as integrated circuits, are often offered in several packages. In general, DIP packages, in either plastic or ceramic, have been the predominate package. These are typically the largest packages and provide the poorest high speed operating environment due to lead configuration. The next best package style is the surface mount package. These are offered in a variety of packages such as SOICs, PLCCs, PQFPs, TSOPs BGAs. These packages will typically reduce the lead capacitance and inductance.

To obtain the optimum performance from the device, the die can be directly mounted to the substrate using either the chip-on-board (COB), flip chip or tape automated bonding (TAB) approach. These offer an optimum approach since they minimize the lead capacitance/inductance.

3.2 Intraconnection

3.2.1 Connectors

Intraconnections are often troublesome in high speed application because a continuous signal environment is not provided. Most board to board connector systems are not designed for use in high performance applications and compromise the signal integrity of the system. Board to board connections often mismatch the characteristic impedance designed into the board themselves.

There are two primary approaches to reduce the signal discontinuity caused by interconnect systems:

- a) The first approach is to provide a connector style such that the pinouts can be arranged to provide a good signal path. Non-differential signals shall establish a relationship between the active signal line and the closest reference plane connection, either a voltage or ground plane. Non-differential signal conductors rely on controlled geometries and nearby reference plane for impedance control. Signal pin quality, reference pin quality and their location controls electrical performance. To optimise performance, reference pins shall be added to reduce the cross-talk problems. Generally a 3 : 1 ratio of signal to reference pins (i.e. 3 signal, 1 reference) is sufficient;
- b) The second approach is to modify the connector to minimize the discontinuity. By shortening the pin length, or adding a reference ground plane within the connector, smaller distances between boards can be used.

Board mounted coaxial connectors are frequently used when only a few signal lines are connecting to a circuit board or where either signal isolation or signal integrity is important.

3.2.2 Cables

Discrete coax connectors and cables are often used because they can couple high speed, high frequency signals to a printed board with little signal degradation. There are four areas that shall be considered:

- signal propagation speed;
- cross-talk;
- induced noise;
- impedance matching.

Discrete coaxial wires have been used with discrete wiring boards for unique, high-speed applications up to 18 GHz. An optical cable has also been used successfully with discrete wiring boards for high frequency signals.

3.3 Printed board and printed board assemblies

Component placement is a critical factor in the design of high-speed systems. The effects of unsuitable placement can be significant and include concerns in the following areas:

- cross-talk management;
- impedance control;
- power distribution.

3.3.1 Board design

The number of signal layers in multilayer boards will be influenced by the density of interconnections within the board as well as the effect of cross-talk or coupling between signal lines. Cross-talk allowance can make it necessary to add layers or can require increasing space between conductors decreasing the interconnect density.

Discrete wiring board density of interconnections within the board will influence the effect of cross-talk. The use of diagonal wire routing on the same wiring layers that route conductors vertically or horizontally (i.e. X and Y directions) may allow greater circuit density per layer and the placement geometries available can accommodate high density and low cross-talk.

A close relationship between design and performance exists in the case of interconnection lines involving high speed digital signals. This interdependence did not exist previously or could be ignored in low-speed signal applications, however, it now imposes new design rules, restrictions and process controls.

To meet the challenges of high-speed digital processing, today's multilayer printed board shall:

- reduce propagation delay;
- lower cross-talk and other line parasitics;
- reduce signal loss;
- allow for high density interconnections.

To achieve these desired goals the designer shall start by controlling the impedance of the transmission lines.

Controlled conductors on boards can be used for signal interconnect between devices. For a given construction, impedance can be controlled with a specific dielectric thickness, conductor thickness, conductor width and the relative permittivity (dielectric constant).

Board substrate selection, relative permittivity (dielectric constant) (ϵ_r) effects signal propagation and thickness for a given characteristic impedance as well as line width. Lower ϵ_r results in faster signal propagation, but increases conductor width for a given impedance value.

For discrete wired boards the conductor thickness and width is controlled by selection of the appropriate wire size. The insulation on the discrete wires can result in a lower effective relative permittivity (dielectric constant) for a given construction, resulting in higher signal propagation speeds in discrete wire boards. Designing to specific impedance values, controls (as transmission lines) the capacitance and the material between conductors. Signal paths should be kept short to minimize propagation delays. Even if it were possible to make a circuit capable of switching at infinite speed, the interconnection material would dictate the performance of the systems. Figure 1 illustrates the switching speed of a device versus propagation delay in a typical woven glass epoxide dielectric commonly used in the printed board industry.

Space constraints, number and complexity of interconnections, power distribution and cost of manufacture are some factors to be considered. When determining requirements of layer count the thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric composition, conductor width/thickness and the overall length. The width and thickness of the conductor will determine manufacturing costs.

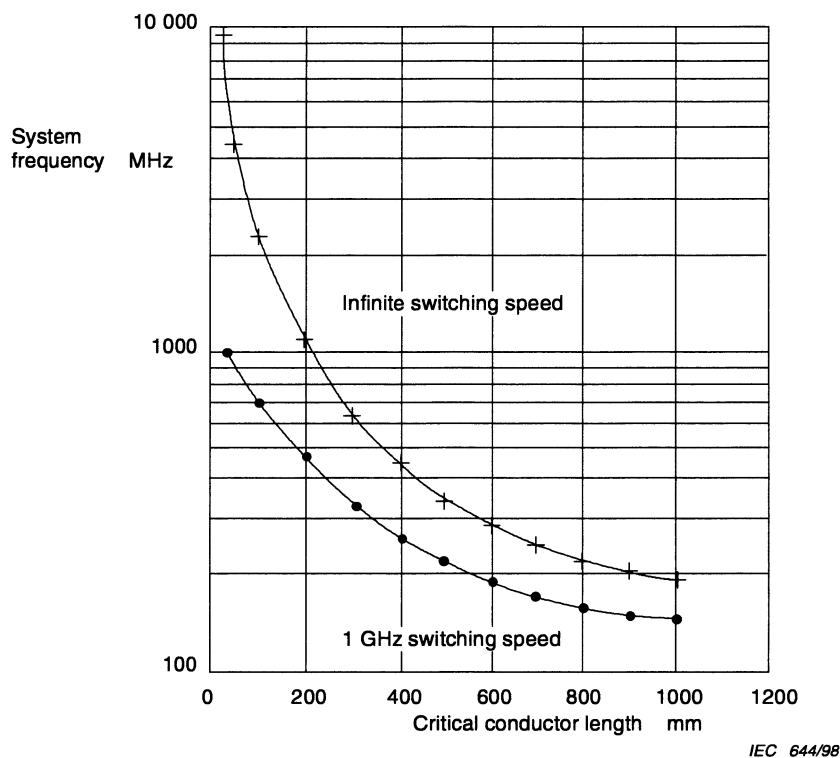


Figure 1 — Switching speed versus propagation delay

3.4 Performance requirements

Electromagnetic wave propagation theory shall be considered in evaluating the performance of the interconnection and their substrates. High-speed devices are characterized by the short rise time of the pulses whose wave form is similar to an a.c. sinusoidal signal. As the rise time of the pulse decreases, the frequency of the wave form increases and the printed board looks increasingly like a high-speed a.c. circuit.

3.4.1 Power distribution

For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in electrical current from the power supply. If several devices demand current at or near the same instant, the power distribution system is required to meet these demands while maintaining its voltage. This requirement demands low inductance connections to devices with high capacitance for the various voltages in the system.

3.4.2 Relative permittivity (dielectric constant)

The relative permittivity, ϵ_r , of a substance is defined as the ratio of the permittivity of the material to the permittivity of free space, which has a value of 1,00. Relative permittivity (dielectric constant) is the term in common use in industry even though dielectric constant varies with several parameters. Factors that influence the relative permittivity (dielectric constant) of a given material include the electrical frequency at which the measurement is performed, temperature, and extent of water absorption. In addition, if the material is a composite for example, a reinforced laminate, the value of ϵ_r may vary enormously as the relative amount of each component of the composite is changed.

The relative permittivity (dielectric constant), ϵ_r , of the dielectric of an interconnecting structure will affect electrical performance. The choice of ϵ_r is used in the design of the structure to meet the impedance, capacitance and propagation time requirements of the system. For a given conductor line geometry, propagation time will vary directly as the square root of ϵ_r , impedance inversely as the square root of ϵ_r , and capacitance directly as ϵ_r .

The effective relative permittivity (dielectric constant), ϵ_r' , is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. An experimental value of ϵ_r' may be obtained using a time domain reflectometry (TDR) technique.

3.4.3 Relative permittivity (dielectric constant) and frequency relationship

Values of both ϵ_r and ϵ_r' are dependent on the reinforcement to resin ratio, temperature, water uptake and the frequency at which the measurement is performed. Steps may be taken to ensure that electrical measurements are performed under conditions that are similar to the final application.

Some materials, such as an epoxide/glass laminate, exhibit a dependence of frequency component of dielectric properties, and it becomes important to choose carefully the frequency at which measurements are made. Select the frequency such that the dielectric parameters obtained may be used to provide a precise prediction of the electrical characteristics of the finished printed board.

Since most transmission characteristics for a printed board are determined by TDR measurements, it is appropriate to use the frequency corresponding to these TDR measurements as the frequency of choice for comparing dielectric properties.

The highest frequency of concern or bandwidth (BW) in gigahertz of a digital pulse may be obtained from the relationship:

$$BW = 0,35/t_r$$

where t_r in nanoseconds is the pulse rise time from 10 % to 90 % of its maximum value. Thus, a typical TDR pulse, with a rise time of 100 ps, has a bandwidth of 3,5 GHz. (Some degradation of this rise time, however, occurs in transmission through the test fixture, thus reducing the effective frequency somewhat.) This dictates that dielectric measurements made by methods other than TDR shall be conducted at higher frequency.

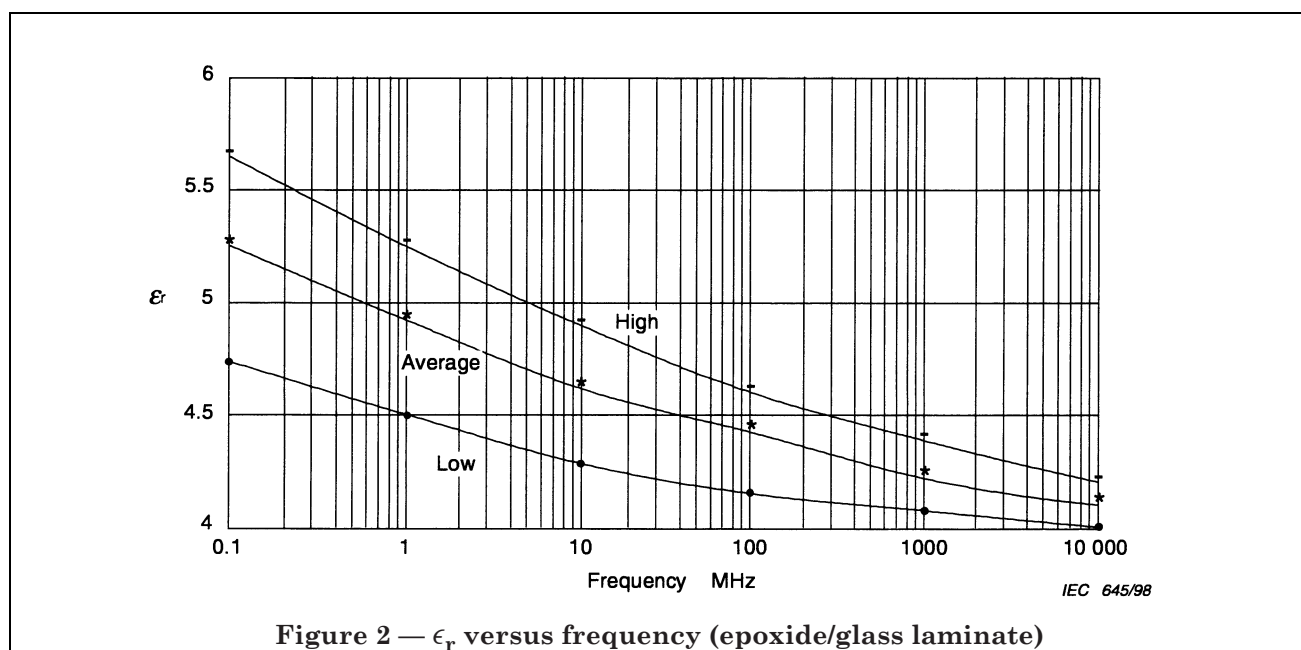


Figure 2 — ϵ_r versus frequency (epoxide/glass laminate)

The equation to predict worldwide average ϵ_r is:

$$\epsilon_r = 4,97 - 0,257 [\log f/10] \times 10^6$$

Three sigma variation was measured at $\pm 0,35$ (8 %).

Three sigma line to line ϵ_r variation on a printed board panel was measured at $\pm 0,26$ (6 %).

As previously stated, ϵ_r is related to the resin to glass ratio. Figure 2 represents an average which takes that into account.

Z_0 predictions will more closely agree with TDR measurements if a value of ϵ_r of 4,1 is used since TDR testing is done at very high frequencies.

Z_0 increases at frequencies below 1 MHz at a rate that is greater than expected. This is due to current spreading on the reference plane.

Figure 2 shows plots of the ϵ_r , measured over the frequency range 100 kHz to 10 GHz, for an epoxide/glass type laminate with a glass-to-resin ratio of approximately 40 : 60 by weight. The value of ϵ_r for this laminate varies from about 4,7 to 4,0 over this frequency range. This change in the magnitude of ϵ_r is principally due to the frequency response of the resin and thus is reduced if the proportion of glass in the composite is increased. In addition, the frequency response will also be changed if an alternative resin system is selected. Material suppliers typically quote values of dielectric properties determined at 1 MHz.

3.4.4 Critical signal speed

The general rule is that transmission line effects (wave effects) become an important design consideration when the length of the conductor approaches 1/7 of the wave length of the signal. If the system clock frequency is 300 MHz, the wavelength in air is about 1 m. Generally, the system clock is a repetition of a square wave pulse. Most systems will be digital, so data are carried in the leading edge of the pulse (the sharp rise). This edge shall be permitted to rise (or fall) as quickly as possible. Frequency and the rise time of the signal are related by the relation $t_r = 0.35/f$ where t_r is rise time in nanoseconds and f is the frequency in gigahertz.

Table 1 shows the rise times for some families of the ICs.

Table 1 — Device rise time

Device rise time	
Device family	Rise time ns
TTL	6–9
Schottky TTL	2–3
ECL	0,45–0,75
GaAs	0,05–0,20

For example, ECL has a rise of 0,45 ns time with a corresponding frequency of 0,35/0,45 GHz or 777 MHz. Using the formula $t_{pd} = \text{square root of } \epsilon_r/c$ (t_{pd} is the propagation delay, c is the speed of light), this translates to a wavelength in air of about 375 mm, 190 mm in epoxide/glass laminate or less than 100 mm in ceramic. This means that for printed boards fabricated from epoxide/glass laminate, if the interconnection path is more than 250 mm, the electromagnetic properties of the signal, and transmission line effects should be considered.

Therefore, the critical signal speed is the signal rise/fall time of the device instead of the clock frequency.

3.4.5 Capacitive line versus controlled impedance line environment

The conductor line can either be treated as a transmission line or a capacitive line. The design concept for transmission lines is to provide a known characteristic impedance with a matching impedance to minimize reflections resulting from fast rise time pulses. The concept for a capacitive line is that a line requires a certain amount of current flow to result in the changed voltage being detected at the destination. The critical design parameters and requirements will depend on which concept is appropriate.

3.4.5.1 Capacitive line

When the signal line is considered as a capacitive line, the propagation time is calculated assuming the line plus the loads connected to it are purely capacitive. Because the reflections on the short interconnecting line occur several times during the pulse's rise time, the net result is a degradation of the edge transition time, i.e. slowing down, as opposed to distinct steps that occur in transmission lines. Using the transmission line equations generally provides a much faster propagation time, creating an inaccurate result.