

Printed boards and printed board assemblies — Design and use —

Part 5-1: Attachment (land/joint) considerations — Generic requirements

The European Standard EN 61188-5-1:2002 has the status of a
British Standard

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National foreword

This British Standard is the official English language version of EN 61188-5-1:2002. It is identical with IEC 61188-5-1:2002.

The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic assembly technology, which has the responsibility to:

- aid enquirers to understand the text;
- present to the responsible international/European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
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**Printed boards and printed board assemblies -
Design and use
Part 5-1: Attachment (land/joint) considerations -
Generic requirements
(IEC 61188-5-1:2002)**

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Foreword

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Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annexes A and B are informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61188-5-1:2002 was approved by CENELEC as a European Standard without any modification.

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PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

Part 5-1: Attachment (land/joint) considerations – Generic requirements

1 Scope and object

This part of IEC 61188 provides information on land pattern geometries used for the surface attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface-mount land patterns to insure sufficient area for the appropriate solder fillet, and also to allow for inspection, testing, and rework of those solder joints.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60097, *Grid systems for printed circuits*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IEC 61188-1-1, *Printed boards and printed board assemblies – Design and use – Part 1-1: Generic requirements – Flatness considerations for electronic assemblies*

IEC 61191-1, *Printed board assemblies – Part 1: Generic specification – Requirements for soldered electrical and electronic assemblies using surface mount and related assembly technologies*

IEC 61191-2, *Printed board assemblies – Part 2: Sectional specification – Requirements for surface mount soldered assemblies*

IEC 61192-1, *Soldered electronic assemblies – Part 1: Workmanship requirements – General* ¹⁾

IEC 61192-2, *Soldered electronic assemblies – Part 2: Workmanship requirements – Surface mounted assemblies* ¹⁾

IEC 61760-1, *Surface mounting technology – Part 1: Standard method for the specification of surface mounting components (SMDs)*

IEC 62326 (all parts), *Printed boards*

¹⁾ To be published.

3 Terms and definitions

For the purposes of this part of IEC 61188, the terms and definitions given in English only in IEC 60194¹⁾ and the following apply.

3.1

assembly

number of parts, subassemblies or combinations thereof joined together

[IEC 60194]

3.2

assembly, double-sided

packaging and interconnecting structure with components mounted on both the primary and secondary sides

3.3

assembly, multilayer printed circuit (wiring)

multilayer printed circuit or printed wiring board on which separately manufactured components and parts have been added

3.4

assembly, packaging and interconnecting (P&IA)

generic term for an assembly that has electronic components mounted on either one or both sides of a packaging and interconnecting structure

3.5

assembly, printed board

assembly of several printed circuit assemblies or printed wiring assemblies, or both

3.6

assembly, printed circuit (wiring)

printed circuit or printed wiring board on which separately manufactured components and parts have been added

3.7

assembly, single-sided

packaging and interconnecting structure with components mounted only on the primary side

3.8

base material

insulating material upon which a conductive pattern may be formed (the base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet)

[IEC 60194]

3.9

basic dimension

numerical value used to describe the theoretical exact location of a feature or hole (it is the basis from which permissible variations are established by tolerance on other dimensions in notes or by feature-control symbols)

[IEC 60194]

¹⁾ Certain definitions of IEC 60194 have been translated into French.

3.10

blind via

via extending only to one surface of a printed board

[IEC 60194]

3.11

buried via

via that does not extend to the surface of a printed board

[IEC 60194]

3.12

castellation

recessed metallized feature on the edge of a leadless chip carrier that is used to interconnect conducting surfaces or planes within or on the chip carrier

[IEC 60194]

3.13

chip carrier

low-profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package (it may be leaded or leadless)

[IEC 60194]

3.14

chip-on-board (COB)

printed board assembly technology that places unpackaged semiconductor dice and interconnects them by wire bonding or similar attachment techniques. Silicon area density is usually less than of the printed board

[IEC 60194 modified]

3.15

coefficient of thermal expansion (CTE)

linear dimensional change of a material per unit change in temperature (see also "thermal expansion mismatch")

[IEC 60194]

3.16

component

individual part or combination of parts that, when together, perform a design function(s) (see also "discrete component" in IEC 60194)

[IEC 60194]

3.17

component mounting site

location on a P&I structure that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component

3.18

conductive pattern

configuration or design of the conductive material on a base material (this includes conductors, lands, vias, heatsinks and passive components when these are an integral part of the printed board manufacturing process)

[IEC 60194]

3.19**conductor**

single conductive path in a conductive pattern

[IEC 60194]

3.20**constraining core**

supporting plane that is internal to a packaging and interconnecting structure

[IEC 60194]

3.21**courtyard**

smallest rectangular area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundaries

3.22**courtyard excess**

area between the rectangle circumscribing the land pattern and the component, and the outer boundary of the courtyard. The courtyard excess may be different in the x and y direction

3.23**courtyard manufacturing zone**

courtyard area plus an allowance, as determined by manufacturing requirements, that will ensure

- a defect-free mounting of a surface-mounting device;
- a proper operation of the circuit, i.e. a function not impaired by too small distances of adjacent components;
- the inspection of the electrical function and of solder joints and, if required, rework and repair

3.24**dual in-line package (DIP)**

rectangular component package that has a row of leads extending from each of the longer sides of its body that are formed at right angles to a plane that is parallel to the base of its body

[IEC 60194]

3.25**fine-pitch technology (FPT)**

surface-mount assembly technology with component terminations on less than 0,625 mm (0,025 in) centres

[IEC 60194]

3.26**fiducial mark**

datum features of the PB used to provide common measurable points for assembly and inspection processes that require positional accuracy

3.27**flat pack**

rectangular component package that has a row of leads extending from each of the longer sides of its body that are parallel to the base of its body

[IEC 60194]

3.28

footprint

(see preferred term "land pattern")

[IEC 60194]

3.29

grid

orthogonal network of two sets of parallel equidistant lines that is used for locating points on a printed board

[IEC 60194]

3.30

integrated circuit (IC)

combination of inseparable associated circuit elements that are formed in place and interconnected on or within a single base material to perform a microcircuit function

[IEC 60194]

3.31

jumper wire

discrete electrical connection that is part of the original design and is used to bridge portions of the basic conductive pattern formed on a printed board (see also "haywire")

[IEC 60194]

3.32

land

portion of a conductive pattern usually, but not exclusively, used for the connection and/or attachment of components

[IEC 60194]

3.33

land pattern

combination of lands that is used for the mounting, interconnection and testing of a particular component

[IEC 60194]

3.34

leadless chip carrier

chip carrier whose external connections consist of metallized terminations that are an integral part of the component body (see also "leaded chip carrier")

[IEC 60194]

3.35

leaded chip carrier

chip carrier whose external connections consist of leads that are around and down the side of the package (see also "leadless chip carrier")

3.36

master drawing

document that shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated, including the arrangement of conductors and non-conductive patterns or elements; the size, type, and location of holes; and all other necessary information

[IEC 60194]

3.37

mixed mounting technology

component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure

3.38

module

separable unit in a packaging scheme

[IEC 60194]

3.39

nominal dimension

dimension that is between the maximum and minimum size of a feature (the tolerance on a nominal dimension gives the limits of variation of a feature size)

3.40

packaging and interconnection structure (P&IS)

general term for a completely processed combination of base materials, supporting planes or constraining cores, and interconnection wiring that are used for the purpose of mounting and interconnecting components

[IEC 60194]

3.41

plated-through hole (PTH)

hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layers, or both, of a printed board

[IEC 60194]

3.42

primary side

side of a packaging and interconnecting structure that is so defined on the master drawing (it is usually the side that contains the most complex or the highest number of components)

[IEC 60194]

3.43

printed board (PB)

general term for completely processed printed circuit and printed wiring configurations (this includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials)

[IEC 60194]

3.44

printed wiring

conductive pattern that provides point-to-point connections but not printed components in a predetermined arrangement on a common base (see also "printed circuit")

[IEC 60194]

3.45

registration

degree of conformity of the position of a pattern (or portion thereof), a hole, or other feature to its intended position on a product

[IEC 60194]

3.46

secondary side

side of a packaging and interconnecting structure that is opposite the primary side (it is the same as the "solder side" on through-hole mounting technology)
[IEC 60194]

3.47

single in-line package (SIP)

component package with one straight row of pins or wire leads
[IEC 60194]

3.48

static charge

electrical charge that has accumulated or built up on the surface of a material

3.49

static electricity control

technique where materials and systems are employed to eliminate/discharge static electricity build-up by providing continuous discharge paths

3.50

supported hole

hole in a printed board that has its inside surfaces plated or otherwise reinforced
[IEC 60194]

3.51

supporting plane

planar structure that is a part of a packaging and interconnecting structure in order to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics (it may be either internal or external to the packaging and interconnecting structure) (see also "constraining core")
[IEC 60194]

3.52

surface-mount technology (SMT)

technology where electrical connection of components is made to the surface of a conductive pattern of a printed board and does not utilize component lead holes

3.53

tented via

blind or through-hole via that has the exposed surface of the primary or secondary or both sides of a packaging and interconnecting structure fully covered by a masking material, such as a dry film polymer coating (solder mask), preimpregnated glass cloth (prepreg), etc., in order to prevent hole access by process solutions, solder, or contamination

3.54

thermal expansion mismatch

absolute difference between the thermal expansion of two components or materials (see also "coefficient of thermal expansion (CTE)")
[IEC 60194]

3.55

through connection

electrical connection between conductive patterns in different layers of a multilayer printed board, for example, a plated-through hole
[IEC 60194]

3.56**through-hole technology (THT)**

assembly process for mounting component packages where leads are passed through supported (plated-through) or unsupported (bare) holes in an interconnection substrate

3.57**tooling feature**

physical feature that is used exclusively to position a printed board or panel during a fabrication, assembly or testing process (see also "locating edge", "locating edge marker", "locating notch", "locating slot", and "tooling hole")

[IEC 60194]

3.58**via**

plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material (see also "blind via" and "buried via")

[IEC 60194]

4 Design requirements**4.1 General**

Although, in many instances, the land pattern geometries can be different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined in such a manner that they are transparent to the attachment process being used. Designers can use the information contained herein to establish standard configurations not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Although patterns are dimensionally defined and since they are a part of the printed board circuitry geometry, they are subject to the producibility levels and tolerances associated with plating, etching, assembly or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

NOTE 1 The dimensions used for component descriptions have been extracted from standards developed by industrial and/or standards bodies. Designers should refer to these standards for additional or specific component package dimensions.

NOTE 2 For a comprehensive description of the given printed board and for achieving the best possible solder joints to the devices assembled, the whole set of design elements includes, beside the land pattern definition:

- solder mask;
- solder paste stencil;
- clearance between adjacent components;
- clearance between bottom of component and PCB surface, if relevant;
- keep-out areas, if relevant;
- suitable rules for adhesive applications.

The whole of design elements is commonly defined as mounting conditions. This standard defines land patterns and includes recommendations for clearances between adjacent components and for other design elements.

NOTE 3 The land patterns and other elements of the mounting conditions, particularly the courtyard, given in this standard are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, have to be carried out by the user. This may also be relevant when solder alloys other than eutectic tin lead solders are used.

NOTE 4 This standard assumes that the land pattern follows the principle that even under worst-case conditions, the overlap of the component termination and the corresponding soldering land will be complete.

NOTE 5 Heat dissipation aspects have not been taken into account in this standard.

NOTE 6 Heavier components (greater mass per land) require larger lands. In some cases, the lands shown in the standard may not be large enough; in these cases, consideration of additional measures may be necessary.

NOTE 7 The land form may be rectangular with straight or rounded corners. In the latter case, the area of the smallest circumscribed rectangle shall be equal to that of one with straight corners.

NOTE 8 Land patterns for lead-free solder alloys may need modifications for optimizing the assembly processes and the reliability of the solder joint.

4.1.1 Classification

The IEC standard on soldering requirements (IEC 61191-1) recognizes that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product types have been established to reflect differences in producibility, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between types.

The user of the assemblies is responsible for determining the type family to which the product belongs. The contract shall specify the type required and indicate any exceptions or additional requirements to the parameters, where appropriate.

LEVEL A: General electronic products

Includes consumer products, some computer and computer peripherals, and hardware suitable for applications where the major requirement is function of the completed assembly.

LEVEL B: Dedicated service electronic products

Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required, and for which uninterrupted service is desired but not mandatory. Typically the end-use environment would not cause failures.

LEVEL C: High-performance electronic products

Includes all equipment where continued performance or performance-on-demand is mandatory. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment shall function when required, such as life support systems and other critical systems.

4.1.2 Land pattern determination

This standard discusses two methods of providing information on land patterns.

- 1) Exact details based on industry component specifications, board manufacturing and component placement accuracy capabilities. These land patterns are restricted to a specific component, and have an identifying land pattern number.
- 2) Equations can be used to alter the given information to achieve a more robust solder connection, when used in particular situations where the equipment for placement or attachment are more or less precise than the assumptions made when determining the land pattern details (see 4.1.2).

Three land pattern geometry variations are supplied for each of the device families: maximum land protrusion (Level 1), median land protrusion (Level 2) and minimum land protrusion (Level 3).

Before adopting the minimum land pattern variation the user should consider product qualification testing based on the conditions shown in table 14.

Level 1: Maximum – For low-density product applications, the maximum land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull-wing devices. The geometry furnished for these devices, as well as inward and J-formed lead contact device families, may provide a wider process window for reflow solder processes as well.

Level 2: Median – Products with a moderate level of component density may consider adapting the median land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded gull-wing type devices.

Level 3: Minimum – High component density typical of portable and hand-held product applications may consider the minimum land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories.

The use of levels of performance (A, B, and C) is combined with that of component density levels (1, 2, and 3) in explaining the condition of an electronic assembly. As an example, combining the description as levels A1 or B3 or C2, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

4.2 Dimensioning systems

This subclause describes a set of dimensional criteria for components, land patterns, positional accuracy of the component placement capability and the opportunity to create a certain size solder joint commensurate with reliability or product performance analysis.

Profile tolerances are used in the dimensioning system to define the size range between maximum and minimum component/lead dimensions without ambiguity. The profile tolerance is intended to control both size and position of the land. Figure 1 shows the profile tolerancing method.

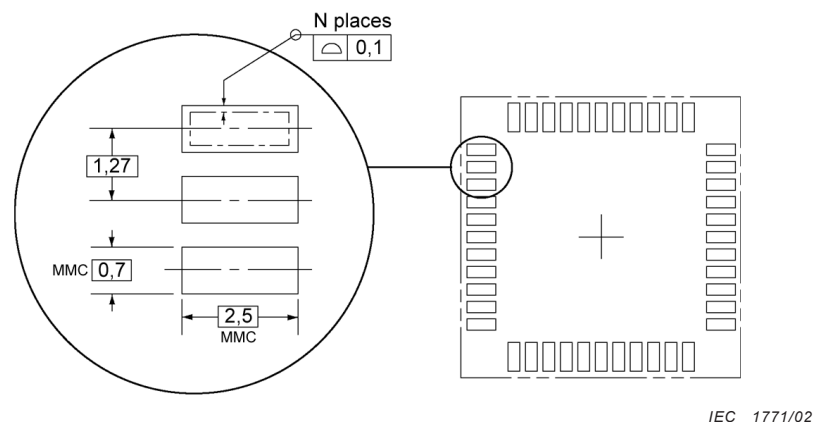


Figure 1 – Profile tolerancing method

The use of the profile dimensioning system requires an understanding of the concepts. The use of a set of requirements are adopted and invoke the following rules, unless otherwise modified.

- All dimensions are basic (nominal).
- Limits of size control form as well as size.
- Perfect form is required at maximum dimensions.

- d) Datum references and position tolerances apply at maximum dimensions, and are dependent on feature size.
- e) Position dimensions originate from maximum dimensions.
- f) Tolerances and their datum references other than size and position apply regardless of feature size (RFS).

The dimensioning concepts used for this system of analysis consider the assembly/attachment requirements as their major goal. Specification (data) sheets for components or dimensions for land patterns on boards may use different dimensioning concepts; however, the goal is to combine all concepts into a single system. Users are encouraged to establish the appropriate relationship between their dimensioning system(s) and the profile dimensioning system and analysis concepts described herein to allow for ease of tailoring these concepts for robust process performance. As an example, if the tolerance used for positioning is larger than the machine tolerance used in production, a single dimensional change could modify the land pattern.

4.2.1 Component tolerancing

The component manufacturers and the IEC technical committees are responsible for the dimensioning and tolerancing of electronic components. Their concepts have been converted to a functional equivalent using the profile tolerancing method with all components shown with their basic dimensions as limit dimensions (maximum or minimum size). Profile tolerances are unilateral and are described to reflect the best condition for solder joint formation.

The concept for component dimension evaluations is based on evaluating the surfaces of the component termination and component lead that are involved in the formation of the acceptable solder joint. Component manufacturers usually provide dimensions for their parts with a nominal size and then put a tolerance on that nominal dimension. In order to facilitate the dimensioning system, these dimensions and their associated tolerances are converted to minimum and maximum size.

As an example, capacitor C3216 has a manufactured nominal dimension for its length (L) of 3,2 mm. The tolerance described by the manufacturer is $\pm 0,2$ mm. Thus, the minimum dimension of L is 3,0 mm with a unilateral tolerance of 0,4 mm, resulting in its maximum dimension being 3,4 mm.

Figure 2 shows the characteristics for the 3216 capacitor. Figure 2a shows the component manufacturer's dimensions for the length of the capacitor. Figure 2b shows the component length at its minimum size in the converted dimensions of the new system using profile tolerancing. Figure 2c shows the land pattern at its maximum size. These conditions provide for an optimum toe fillet. For optimum heel fillet, the component basic dimensions are at the maximum and the land pattern is at its minimum.

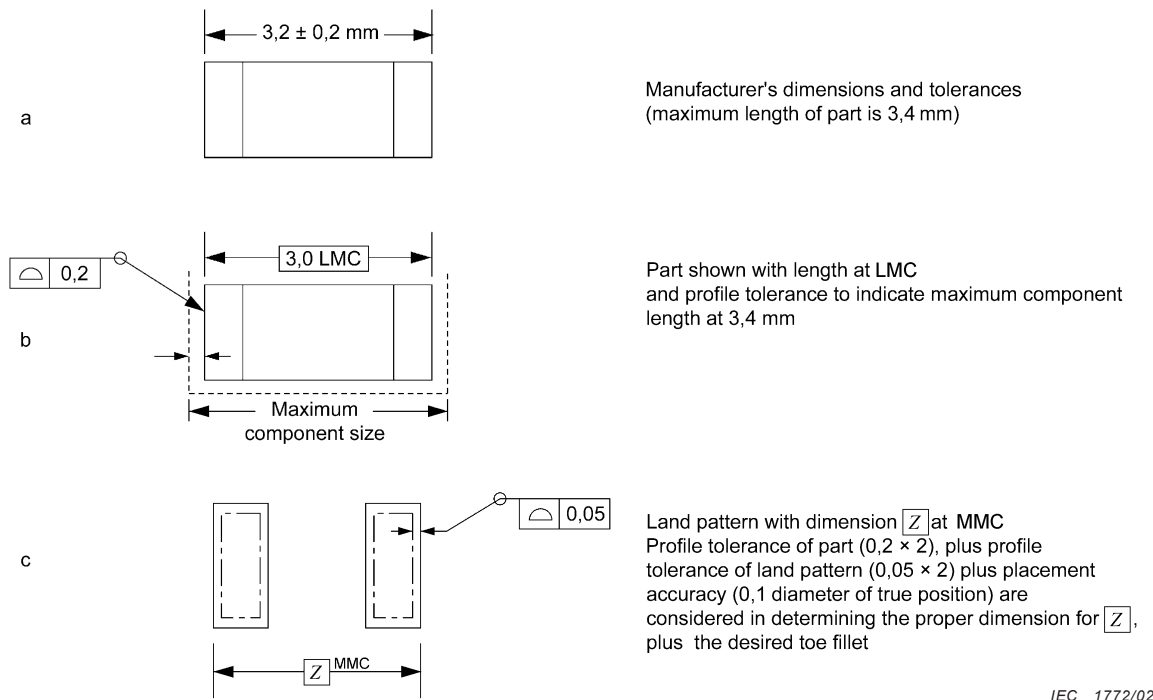


Figure 2 – Example of 3216 capacitor dimensioning for optimum solder fillet condition

Similar concepts are applied to leaded surface-mount parts. The critical dimensional characteristics identified are those that relate to the formation of the toe and heel solder fillet. For components with gull-wing leads, the basic dimensions apply across the outer extremities of the part for toe solder fillet formation; and within the inside of the formed radius of opposing leads for heel solder fillet formation.

The outer dimensions of leaded or even leadless chip carriers are usually easy to determine since these are readily available from the component manufacturer. The inner (heel-to-heel) dimensions are not provided in industry standards or manufacturers' specifications and are more difficult to determine, not only because of the form of the lead, termination, or castellation but also because the inner dimensions must be derived by subtracting the sum of the dimensions of the leads (with all their inherent tolerances) from the overall dimensions of the part.

Figure 3a shows the concept for the manufacturer's dimensions and tolerances for a gull-wing SOIC. Figure 3b shows the converted dimensions to be considered in the overall mounting system requirements. Figure 3c shows the land pattern dimensions. The basic dimensions define the minimum length as measured across the two outer extremities. Tolerances increase this dimension to the maximum width, reducing toe fillet opportunity.

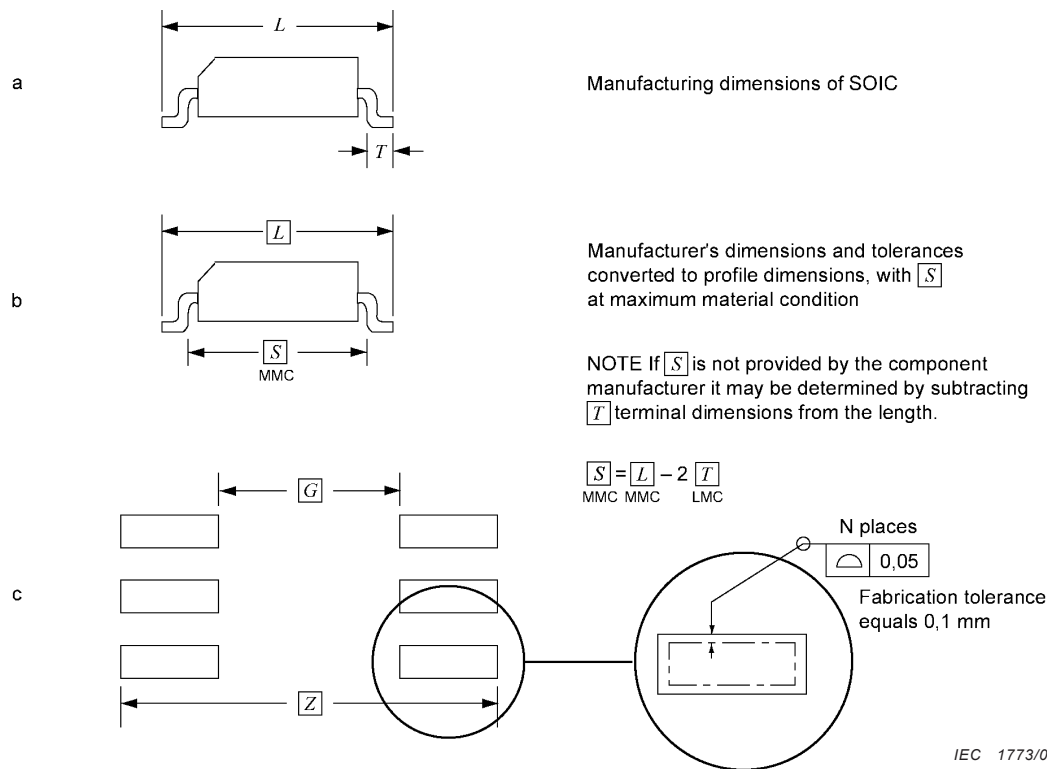


Figure 3 – Profile dimensioning of gull-wing leaded SOIC

The inner dimensions between heel fillets on opposing sides are the most important. Inner dimensions are derived by

- establishing the maximum width of the component as measured from lead termination to lead termination (this dimension is shown as L and is provided by the manufacturer);
- establishing the minimum amount of the lead length as measured across the footprint (from heel to toe for gull-wing leads) (this dimension is T and is provided by the manufacturer);
- subtracting twice the minimum lead length of (b) from the maximum overall component length of (a) to arrive at the maximum length inside the leads across the length of the component (the inner dimension between opposing heel fillets). Including the tolerances on dimensions (a) and (b) will yield the minimum dimension between opposing heels. This signifies worst-case tolerance analysis.
- Three sets of tolerances are involved in the analysis described in c): tolerances on the overall component, plus the tolerances for the lead on each end. Since not all three tolerances are considered at their worst case, a recommended method for determining the statistical impact is to summarize the squares of the tolerances and take the square-root of their sum as the r.m.s. (root-mean-square) tolerance difference.

For example,

$$\text{RMS tolerance accumulation} = \sqrt{(L_{\text{tol}})^2 + 2(T_{\text{tol}})^2}$$

where

$$L_{\text{tol}} = L_{\text{max}} - L_{\text{min}}$$

$$T_{\text{tol}} = T_{\text{max}} - T_{\text{min}}$$

As an example, the SOIC with 16 leads has the following limits for the L (component length) and T (terminal length) dimensions:

$$L_{\min} = 5,8 \text{ mm}, L_{\max} = 6,2 \text{ mm}$$

$$L_{\text{tol}} = L_{\max} - L_{\min} = 6,2 - 5,8 = 0,4 \text{ mm}$$

$$T_{\min} = 0,4 \text{ mm}, T_{\max} = 1,27 \text{ mm}$$

$$T_{\text{tol}} = T_{\max} - T_{\min} = 1,27 - 0,4 = 0,87 \text{ mm}$$

Therefore, the calculations for S minimum and maximum dimensions are as follows:

$$S_{\min} = L_{\min} - 2T_{\max} = 5,8 - 2(1,27) = 3,26 \text{ mm}$$

$$S_{\max} = L_{\max} - 2T_{\min} = 6,2 - 2(0,4) = 5,40 \text{ mm}$$

$$S_{\text{tol}} = S_{\max} - S_{\min} = 5,4 - 3,26 = 2,14 \text{ mm}$$

The difference between $S_{\min}$ and $S_{\max}$ is 2,14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-case scenario for the tolerance range for S can also be calculated by adding the tolerances for the component length and the two terminals:

$$S_{\text{tol}} = L_{\text{tol}} + 2 T_{\text{tol}} = 0,4 + 2(0,87) = 2,14 \text{ mm}$$

In order to arrive at a more realistic tolerance range, the r.m.s. value is calculated using the tolerances on the dimensions involved (L and T):

$$S_{\text{tol}} (\text{r.m.s.}) = \sqrt{(L_{\text{tol}})^2 + 2(T_{\text{tol}})^2} = \sqrt{0,4^2 + 2(0,87)^2} = 1,29 \text{ mm}$$

$S_{\text{tol}} (\text{r.m.s.})$ is added to $S_{\min}$ to arrive at a maximum S dimension. This technique is used so that a more realistic $S_{\max}$ dimension is used in the land pattern equations for calculating $G_{\min}$ (minimum land pattern gap between heel fillets). In this example, the following calculation is used for $S_{\max}$:

$$S_{\max} (\text{r.m.s.}) = S_{\min} + S_{\text{tol}} (\text{r.m.s.}) = 3,26 + 1,29 = 4,55 \text{ mm}$$

To determine the $G_{\min}$ dimension for the land pattern, $S_{\text{tol}} (\text{r.m.s.})$ is used for the component tolerance (i.e., $S_{\text{tol}} (\text{r.m.s.}) = C$). The calculations for $G_{\min}$ are as follows:

$$G_{\min} = S_{\max} - 2J - \sqrt{C^2 + F^2 + P^2}$$

NOTE See calculation in 4.2.4.

4.2.1.1 Solving for dimension Z

It should be noted that there are various options to determine the tolerances for the component (C), the fabrication allowance (F), and the placement tolerance (P). In determining the calculations for the example in figure 2 for the dimension Z , one would note that the component 3216 has an $L_{\max}$ equal to 3,4 mm, and an $L_{\min}$ equal to 3,0 mm. With the assumption that F is equal to 0,1 mm and P is equal to 0,2 mm, the following conditions would be used for determining the Z dimension:

$$Z_{\max} = L_{\min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$Z_{\max} = 3,0 + 2J_T + \sqrt{0,4^2 + 0,1^2 + 0,2^2}$$

In the above example, the two joints should be rounded to a realistic number. Normally, a total Z dimension of 4,6 would be acceptable for a level 2 land pattern providing a little larger than a 0,5 mm land protrusion at either end of the 3216 component.

4.2.2 Land tolerancing

Profile tolerancing is used for lands in a manner similar to that of the components. All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Unilateral tolerances are intended to reduce the land size and thus result in a lesser area for solder joint formation. In order to facilitate companion dimension systems, the land pattern is dimensioned across outer and inner extremities.

The dimensioning concept in this standard uses limiting dimensions and geometric tolerancing to describe the allowable maximum and minimum dimensions of the land pattern. When lands are at their maximum size, the result may be a minimum acceptable space between lands; conversely, when lands are at their minimum size, the result may be a minimum acceptable land pattern necessary to achieve the minimum required land protrusion. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this standard is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions, etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis (see table 14).

4.2.3 Fabrication allowances

Figure 3 shows the land pattern for an SOIC with gull-wing leads intended to be a companion to the chip component dimensioning concepts shown previously in figure 2. The basic L dimension is across the outer extremities of the component.

For the land pattern, dimension Z is at maximum size, while the inner extremities (dimension G) are dimensioned at minimum size. Unilateral tolerances decreased the basic dimension for Z while increasing the basic G dimension. This action results in a reduced land pattern at least material condition (LMC). Thus, processing target values shall be as close as possible to the basic Z and G dimensions at maximum material condition (MMC). This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

The variation between the dimensions Z , G , and X are indicated as a fabrication allowance (F). This fabrication allowance (see table 14) represents the maximum variation between the largest land pattern size (MMC) and the least land pattern size (LMC). This does not include material movement as described in table 15, which is included in the assembly tolerancing since machine vision capability re-evaluates the true position of the land pattern.

4.2.4 Assembly tolerancing

Another part of the equation is the assembly variation defined by the letter P . This variation represents the location of the component in relation to its true position as defined by the design. The term diameter of true position (DTP) is used to describe this variation and is a single number that can be used in the dimensional tolerance analysis.

As an example, for establishing the target heel protrusion dimensions of the example shown in figure 3, the following conditions would be true: