

Printed boards and printed board assemblies — Design and use —

Part 5-2: Attachment (land/joint) considerations — Discrete components

The European Standard EN 61188-5-2:2003 has the status of a
British Standard

ICS 31.180; 31.190

National foreword

This British Standard is the official English language version of EN 61188-5-2:2003. It is identical with IEC 61188-5-2:2003.

The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic assembly technology, which has the responsibility to:

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- monitor related international and European developments and promulgate them in the UK.

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**Printed boards and printed board assemblies -
Design and use
Part 5-2: Attachment (land/joint) considerations -
Discrete components
(IEC 61188-5-2:2003)**

Cartes imprimées et cartes imprimées
équipées -
Conception et utilisation
Partie 5-2: Considérations sur les liaisons
pistes-soudures -
Composants discrets
(CEI 61188-5-2:2003)

Leiterplatten und Flachbaugruppen -
Konstruktion und Anwendung
Teil 5-2: Betrachtungen zur Montage
(Anschlussfläche/Verbindung) -
Einzelbauelemente
(IEC 61188-5-2:2003)

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 91/382/FDIS, future edition 1 of IEC 61188-5-2, prepared by IEC TC 91, Electronics assembly technology, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61188-5-2 on 2003-09-01.

This European Standard is to be read in conjunction with EN 61188-5-1:2002.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2004-06-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2006-09-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61188-5-2:2003 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standards indicated:

IEC 60051	NOTE	Harmonized as EN 60051 series (not modified).
IEC 61191-1	NOTE	Harmonized as EN 61191-1:1998 (not modified).
IEC 61191-2	NOTE	Harmonized as EN 61191-2:1998 (not modified).

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INTRODUCTION

This part of IEC 61188 covers land patterns for discrete components such as chip resistors, chip capacitors, and various diode and transistor types.

The proposed land pattern dimensions are based upon the fundamental tolerance calculation combined with the given land protrusions and courtyard excesses (see IEC 61188-5-1, Generic requirements). The courtyard includes all issues relating to normal manufacturing requirements.

The land pattern dimensions given in this standard are generally applicable for reflowed solder paste processes. For immersion soldering processes (e.g. wave, jet, drag soldering), lands may have to be modified to prevent shadowing and shorting (e.g. by extending land length parallel to the direction of motion of the board and/or provision of solder thieves).

This standard offers a threefold land pattern dimensioning (levels 1, 2 and 3) on the basis of a threefold set of land protrusions and courtyard excesses: maximum (max.), median (mdn) and minimum (min.). Each land pattern has been assigned an identification number to indicate the characteristics of the specific robustness of the land patterns. Users also have the opportunity to organize the information so that it is most useful for their particular design.

This standard assumes that land dimensions are always larger than component termination or lead outlines. If a user has good reason to use solder resist to limit wetting on a land, or to use lands smaller than component terminations, or to apply a concept different from that of IEC 61188-5-1, then this standard may not apply.

It is the responsibility of the user to verify the SMD land patterns used for achieving an undisturbed mounting process, including testing, and an ensured reliability for the product stress conditions in use.

Dimensions of the components listed in this standard are those available on the market and are for reference only.

PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

Part 5-2: Attachment (land/joint) considerations – Discrete components

1 Scope

This part of IEC 61188 provides information on land pattern geometries used for the surface attachment of discrete electronic components.

The purpose of this standard is to provide the appropriate size, shape and tolerances of surface mount land patterns to ensure sufficient area for the appropriate solder fillet, and also allow for inspection, testing and rework of resulting solder joints.

Each clause contains a specific set of clearly presented criteria providing information on the component, the component dimensions, the solder joint design and the land pattern dimensions.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60115-1, *Fixed resistors for use in electronic equipment – Part 1: General specification*

IEC 60286-3, *Packaging of components for automatic handling – Part 3: Packaging of leadless components on continuous tapes*

IEC 60286-4, *Packaging of components for automatic handling – Part 4: Stick magazines for electric components encapsulated in packages of form E and G*

IEC 60286-5, *Packaging of components for automatic handling – Part 5: Matrix trays*

IEC 60286-6, *Packaging of components for automatic handling – Part 6: Bulk case packaging for surface mounting compounds*

IEC 60384-3, *Fixed capacitors for use in electronic equipment – Part 3: Sectional specification: Fixed Tantalum chip capacitors*

IEC 60384-18, *Fixed capacitors for use in electronic equipment – Part 18: Sectional specification – Fixed aluminium electrolytic chip capacitors with solid and non-solid electrolyte*

IEC 60384-20, *Fixed capacitors for use in electronic equipment – Part 20: Sectional specification – Fixed metallized polyphenylene sulfide film dielectric chip d.c. capacitors*

IEC 61188-5-1, *Printed boards and printed board assemblies – Design and use – Part 5-1: Attachment (land/joint) considerations – Generic requirements*

IEC 61605, *Fixed inductors for use in electronic and telecommunication equipment – Marking codes*

3 Packaging

The following IEC standards shall be referred to:

- IEC 60286-3 (see figure 1);
- IEC 60286-4;
- IEC 60286-5;
- IEC 60286-6.

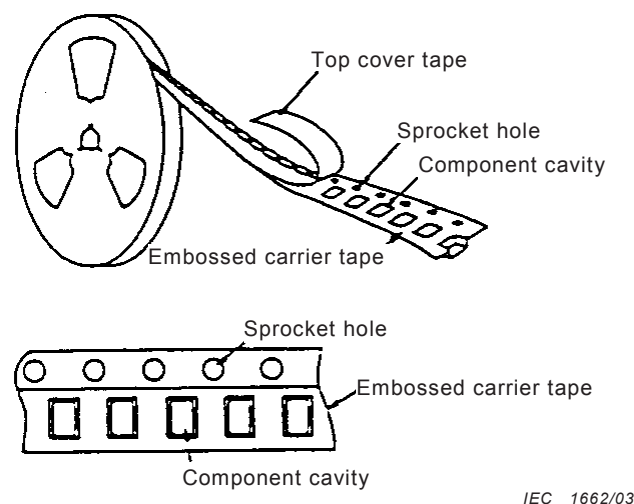


Figure 1 – Packaging

4 Fixed rectangular chip resistors

4.1 Introductory remark

This clause specifies the dimensions of components and land patterns for fixed rectangular chip resistors, together with an analysis of tolerance and solder joint assumptions for the land pattern dimensions.

4.2 Component description

A variety of values exist for the dimensions of resistors. The following subclauses describe the most common types.

4.2.1 Basic construction

Figure 2 shows a typical construction example. The resistive material is coated to a ceramic substrate and terminated symmetrically at both ends with a "wrap around" metal U-shaped band. The resistive material is face-up. Since most equipment uses a vacuum-type pick-up head, it is important that the surface of the resistor is made flat, otherwise vacuum pick-up might be difficult.

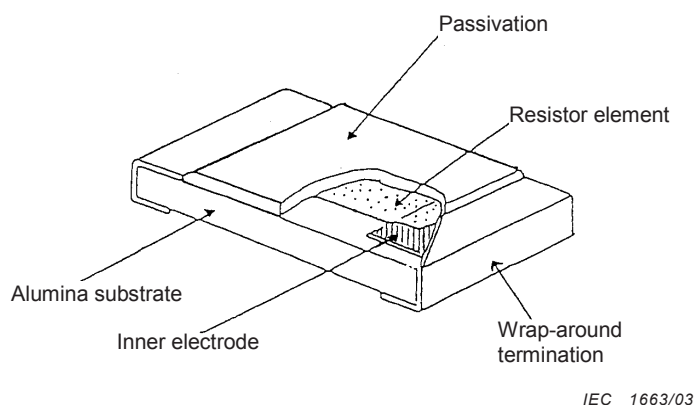


Figure 2 – Fixed rectangular chip resistor construction

4.2.2 Termination materials

Electrodes should be coated with a material suited to the solder and method of soldering to be used.

The terminations shall be symmetrical, and shall not have nodules, lumps, protrusions, etc., that degrade the symmetry or dimensional tolerances of the part. The end termination shall cover the end of a component, and shall extend out to the top and bottom of the component. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer material should be nickel or a similar metal effective as a diffusion barrier.

4.2.3 Marking

Chip resistors are generally not marked on the body. If some marking can be applied, the chip resistor shall be clearly marked with the rated resistance, and as many of the remaining items as possible from 2.4 of IEC 60115-1.

4.2.4 Carrier package format

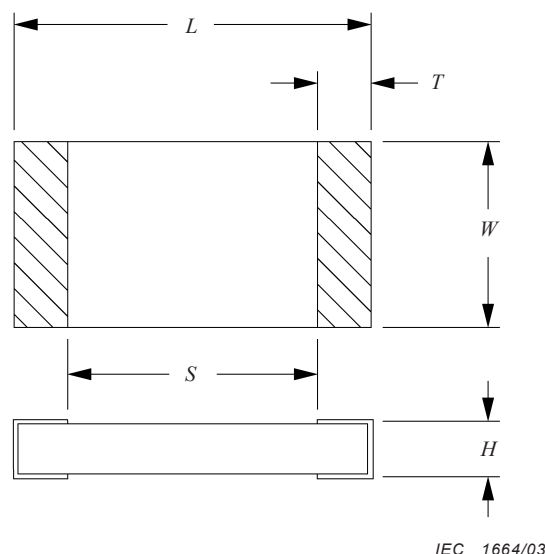
Refer to IEC 60286-3.

4.2.5 Solderability and resistance to dissolution of metallization and to soldering heat

Refer to IEC 60068-2-58.

4.3 Component dimensions

Figure 3 shows the component dimensions for fixed rectangular chip resistors.



Dimensions in millimetres

Component identifier	L		S		W		T		H	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1005	0,95	1,05	0,35	0,75	0,45	0,55	0,15	0,30	0,30	0,40
1608	1,50	1,70	0,50	1,50	0,70	0,90	0,10	0,50	0,35	0,55
2012	1,90	2,10	0,70	1,70	1,15	1,35	0,20	0,60	0,45	0,65
3216	3,00	3,40	1,50	2,90	1,45	1,75	0,25	0,75	0,45	0,65
3225	3,00	3,40	1,50	2,90	2,30	2,70	0,25	0,75	0,45	0,65
5025	4,80	5,20	3,10	4,50	2,30	2,70	0,35	0,85	0,35	0,75
6332	6,10	6,50	4,40	5,80	3,00	3,40	0,35	0,85	0,35	0,75

Figure 3 – Fixed rectangular chip resistor dimensions

4.4 Solder joint fillet design

Figure 4 shows the shape and dimensions of the solder fillet after the soldering process. The minimum, median and maximum dimensions of each of toe, heel, and side fillet are determined by taking into consideration solder joint reliability and also quality and productivity in the parts mount process. Designing land patterns needs consideration of three factors in accuracy: parts dimensions accuracy (C), parts mount accuracy on PWBs (P) and land shape accuracy on PWBs (F), in addition to fillet dimensions. The formulae to obtain the tolerance resulting from these factors are as follows:

a. Design consideration when soldered without self-alignment effect (level 1)

In flow soldering process, there is no self-alignment effect. Thus, the formulae cannot be simplified but remain the same as follows:

$$\begin{aligned}
 Z_{\max} &= L_{\min} + 2J_{T \max} + T_T & T_T &= \sqrt{F_{L1}^2 + P_{L1}^2 + C_L^2} \\
 G_{\min} &= S_{\max} - 2J_{H \max} - T_H & T_H &= \sqrt{F_{L1}^2 + P_{L1}^2 + C_S^2} \\
 X_{\max} &= W_{\min} + 2J_{S \max} + T_S & T_S &= \sqrt{F_{L1}^2 + P_{L1}^2 + C_W^2}
 \end{aligned}$$

b. Design consideration when soldered without self-alignment effect (level 2)

$$\begin{aligned} Z_{\max} &= L_{\min} + 2J_{T \text{ mdn}} + T_T & T_T &= \sqrt{F_{L2}^2 + P_{L2}^2 + C_L^2} \\ G_{\min} &= S_{\max} - 2J_{H \text{ mdn}} - T_H & T_H &= \sqrt{F_{L2}^2 + P_{L2}^2 + C_S^2} \\ X_{\max} &= W_{\min} + 2J_{S \text{ mdn}} + T_S & T_S &= \sqrt{F_{L2}^2 + P_{L2}^2 + C_W^2} \end{aligned}$$

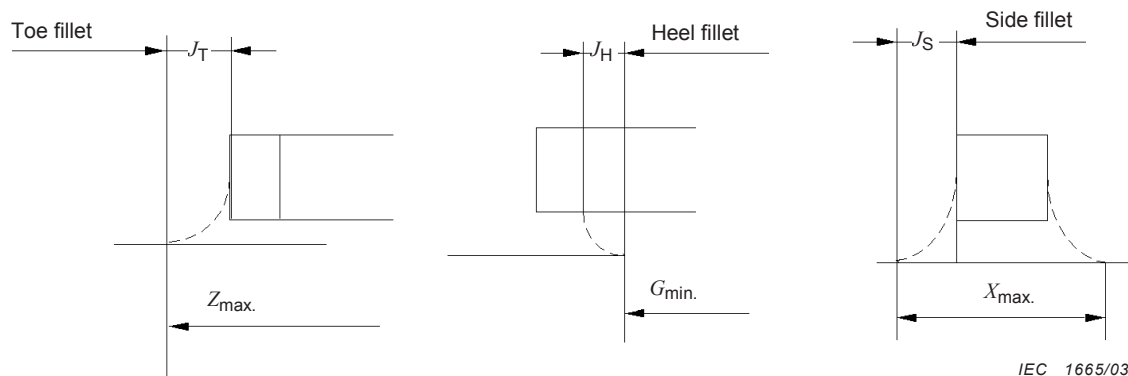
c. Design consideration when soldered with self-alignment effect (level 3)

$$\begin{aligned} Z_{\max} &= L_{\min} + 2J_{T \text{ min}} + T_T & T_T &= \sqrt{F_{L3}^2 + P_{L3}^2 + C_L^2} \\ G_{\min} &= S_{\max} - 2J_{H \text{ min}} - T_H & T_H &= \sqrt{F_{L3}^2 + P_{L3}^2 + C_S^2} \\ X_{\max} &= W_{\min} + 2J_{S \text{ min}} + T_S & T_S &= \sqrt{F_{L3}^2 + P_{L3}^2 + C_W^2} \end{aligned}$$

In a reflow soldering process, there is a self-alignment effect because adhesives are not used to hold components. In the surface mount process of reflow soldering, parts mount displacement and the land shape accuracy on PWBs, when soldered, can be corrected by self-alignment effect (therefore factor P and F can be regarded as 0). Thus, the formulae can be simplified as follows:

$$\begin{aligned} T_T &= C_L, & Z_{\max} &= L_{\min} + 2J_{T \text{ min}} + C_L = L_{\max} + 2J_{T \text{ min}} \\ T_H &= C_S, & G_{\min} &= S_{\max} - 2J_{H \text{ min}} - C_S = S_{\min} - 2J_{H \text{ min}} \\ T_S &= C_W, & X_{\max} &= W_{\min} + 2J_{S \text{ min}} + C_W = W_{\max} + J_{S \text{ min}} \end{aligned}$$

Any tolerance other than the above may be used depending on the soldering strength required, the capability of the production process used, etc.



NOTE Where resistors have no side termination material, the 'side fillet' or J_S dimension refers to the tapered portion of the end fillet.

Dimensions in millimetres

Component identifier	Tolerance assumptions						Solder joint											
							Toe				Heel				Side			
	F			P			J_T				J_H				J_S			
	$L-1$	$L-2$	$L-3$	$L-1$	$L-2$	$L-3$	C_L	Max.	Mdn	Min.	C_S	Max.	Mdn	Min.	C_W	Max.	Mdn	Min.
1005	0,3	0,2	0,1	0,2	0,15	0,1	0,1	0,6	0,4	0,2	0,4	0	0	0	0,1	0	0	0
1608	0,3	0,2	0,1	0,4	0,2	0,1	0,2	0,6	0,4	0,2	1	0	0	0	0,2	0	0	0
2012	0,3	0,2	0,1	0,4	0,2	0,1	0,2	0,6	0,4	0,2	1	0	0	0	0,2	0	0	0
3216	0,3	0,2	0,1	0,4	0,2	0,1	0,4	0,6	0,4	0,2	1,4	0	0	0	0,3	0	0	0
3225	0,3	0,2	0,1	0,4	0,2	0,1	0,4	0,6	0,4	0,2	1,4	0	0	0	0,4	0	0	0
5025	0,3	0,2	0,1	0,4	0,2	0,1	0,4	0,6	0,4	0,2	1,4	0	0	0	0,4	0	0	0
6332	0,3	0,2	0,1	0,4	0,2	0,1	0,4	0,6	0,4	0,2	1,4	0	0	0	0,4	0	0	0

Figure 4 – Solder joint protrusion

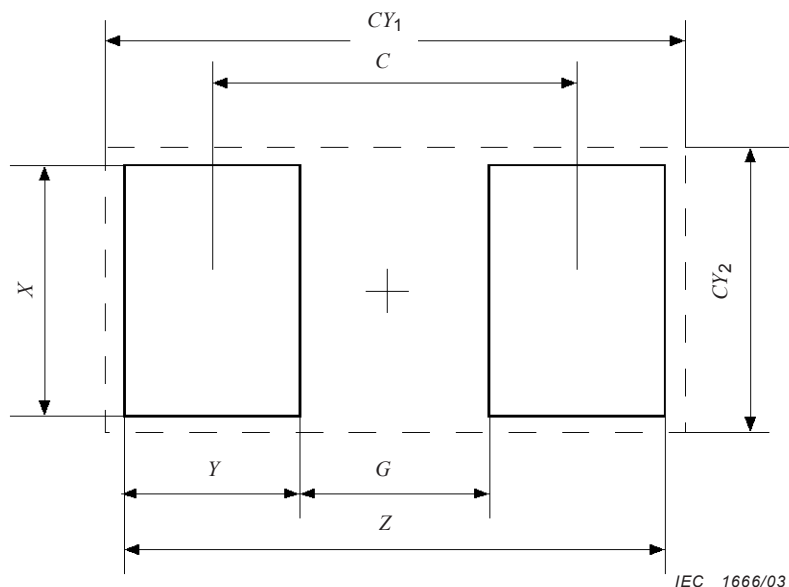
4.5 Land pattern dimensions

Figure 5 shows the land pattern dimensions for fixed rectangular chip resistors for reflow and flow soldering. These values are calculated based on the formulae for the solder joint fillet design given in 4.4. G_{min} values for chip resistor of 1005 are larger than the calculated values to prevent the solder from forming a bridge between neighbouring lands.

The courtyard is calculated using the following formulae and rounded up (round-up factor is nearest 0,05 for min. and 0,5 for max).

$$CY_1 = \{ \text{whichever is larger } [L_{min} + \sqrt{F^2 + P^2 + C_L^2}] \text{ or } [Z] \} \\ + (\text{courtyard excess} \times 2)$$

$$CY_2 = \{ \text{whichever is larger } [W_{min} + \sqrt{F^2 + P^2 + C_W^2}] \text{ or } [X] \} \\ + (\text{courtyard excess} \times 2)$$



Level 1

Dimensions in millimetres

Pattern identifier	Component identifier	Z	G	X	Y	C	CY ₁	CY ₂
2010M	1005	2,55	0,5	0,85	1,05	1,55	4	2
2011M	1608	3,25	0,5	1,25	1,4	1,9	5	3
2012M	2012	3,65	0,55	1,7	1,55	2,1	5	3
2013M	3216	4,85	1,6	2,05	1,65	3,25	6	4
2014M	3225	4,85	1,6	2,95	1,65	3,25	6	4
2015M	5025	6,65	3,2	2,95	1,75	4,95	8	4
2016M	6332	7,95	4,5	3,65	1,75	6,25	9	5

Level 2

Pattern identifier	Component identifier	Z	G	X	Y	C	CY ₁	CY ₂
2010N	1005	2,05	0,5	0,75	0,8	1,3	2,6	1,3
2011N	1608	2,65	0,5	1,05	1,1	1,6	3,2	1,6
2012N	2012	3,05	0,65	1,5	1,2	1,85	3,6	2
2013N	3216	4,3	1,65	1,9	1,35	3	4,8	2,4
2014N	3225	4,3	1,65	2,8	1,35	3	4,8	3,3
2015N	5025	6,1	3,25	2,8	1,45	4,7	6,6	3,3
2016N	6332	7,4	4,55	3,5	1,45	6	7,9	4

Level 3

Pattern identifier	Component identifier	Z	G	X	Y	C	CY ₁	CY ₂
2010L	1005	1,45	0,5	0,55	0,5	1,0	1,6	0,8
2011L	1608	2,1	0,5	0,9	0,8	1,3	2,2	1,1
2012L	2012	2,5	0,7	1,35	0,9	1,6	2,6	1,5
2013L	3216	3,8	1,5	1,75	1,15	2,65	3,9	1,9
2014L	3225	3,8	1,5	2,7	1,15	2,65	3,9	2,9
2015L	5025	5,6	3,1	2,7	1,25	4,35	5,7	2,9
2016L	6332	6,9	4,4	3,4	1,25	5,65	7,0	3,6

Figure 5 – Fixed rectangular chip resistor land pattern dimensions

5 Fixed cylindrical chip resistors

5.1 Introductory remark

This clause specifies the dimensions of components and land patterns for fixed cylindrical chip resistors, together with an analysis of tolerance and solder joint assumptions for the land pattern dimensions.

5.2 Component description

A variety of values exist for the dimensions of resistors. The following subclauses describe the most common types.

5.2.1 Basic construction

Figure 6 shows a typical construction example.

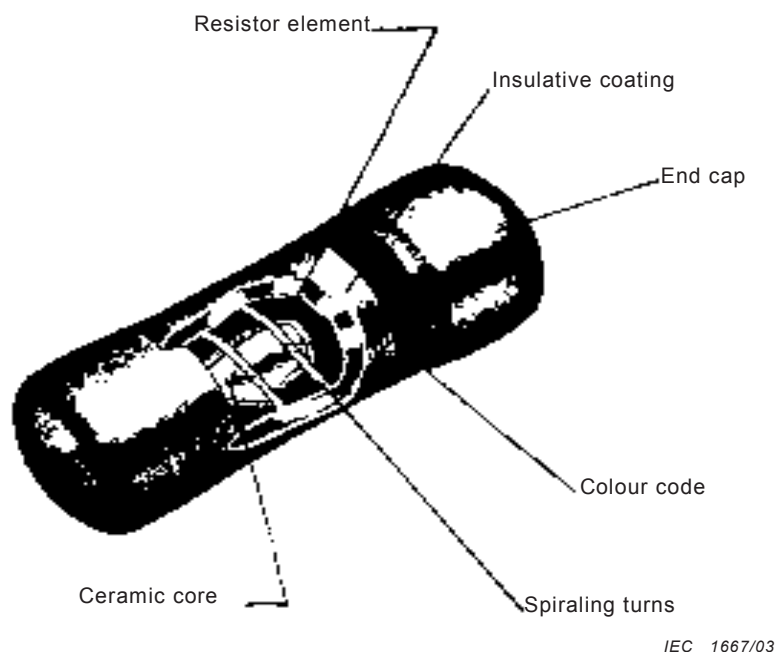


Figure 6 – Fixed cylindrical chip resistor construction

5.2.2 Termination materials

Electrodes should be coated with a material suited to the solder and method of soldering to be used.

The terminations shall be symmetrical and shall not have nodules, lumps, protrusions, etc. that degrade the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components and shall extend around the entire periphery.

5.2.3 Marking

Chip resistors are generally not marked on the body. If some marking can be applied, the chip resistor shall be clearly marked with the rated resistance, and as many of the remaining items as possible from 2.4 of IEC 60115-1.

5.2.4 Carrier package format

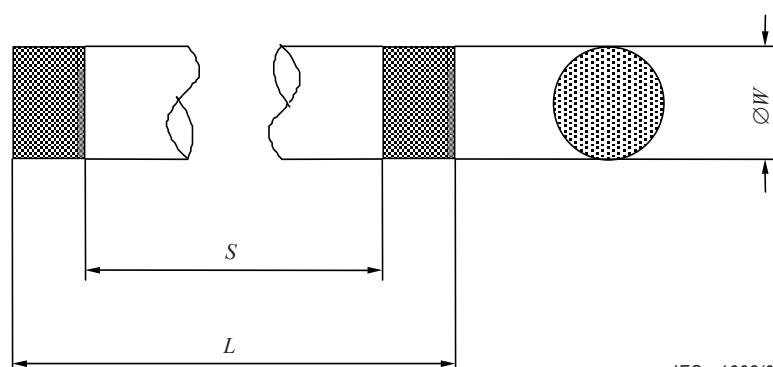
Refer to IEC 60286-3 or IEC 60286-6.

5.2.5 Solderability and resistance to dissolution of metallization and to soldering heat

Refer to IEC 60068-2-58.

5.3 Component dimensions

Figure 7 shows the component dimensions for fixed cylindrical chip resistors.



IEC 1668/03

Dimensions in millimetres

Component identifier	L		S		W		T	
	Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.
1610	1,50	1,65	0,50	1,35	0,95	1,15	0,15	0,50
2012	1,90	2,10	0,60	1,50	1,15	1,35	0,30	0,65
3514	3,30	3,70	1,10	3,10	1,30	1,50	0,30	1,10
5922	5,70	6,10	2,70	5,10	2,10	2,30	0,50	1,50

Figure 7 – Fixed cylindrical chip resistor dimensions

5.4 Solder joint fillet design

Figure 8 shows the shape and dimensions of the solder fillet after soldering process. The minimum, median and maximum dimensions of each of toe, heel, and side fillet are determined by taking into consideration solder joint reliability, and also quality and productivity in parts mount process. Designing land patterns needs consideration of three factors in accuracy: parts dimensions accuracy (C), parts mount accuracy on PWBs (P) and land shape accuracy on PWBs (F), in addition to fillet dimensions. The formulae to obtain the tolerance resulted from these factors are as follows:

a. Design consideration when soldered without self-alignment effect (level 1)

In flow soldering process, there is no self-alignment effect. Thus, the formulae cannot be simplified but remain the same as follows:

$$\begin{aligned}
 Z_{\max} &= L_{\min} + 2J_{T \max} + T_T & T_T &= \sqrt{F_{L1}^2 + P_{L1}^2 + C_L^2} \\
 G_{\min} &= S_{\max} - 2J_{H \max} - T_H & T_H &= \sqrt{F_{L1}^2 + P_{L1}^2 + C_S^2} \\
 X_{\max} &= W_{\min} + 2J_{S \max} + T_S & T_S &= \sqrt{F_{L1}^2 + P_{L1}^2 + C_W^2}
 \end{aligned}$$