

Printed boards and printed board assemblies — Design and use —

Part 5-6: Attachment (land/joint) considerations — Chip carriers with J-leads on four sides

The European Standard EN 61188-5-6:2003 has the status of a
British Standard

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National foreword

This British Standard is the official English language version of EN 61188-5-6:2003. It is identical with IEC 61188-5-6:2003.

The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic assembly technology, which has the responsibility to:

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- present to the responsible international/European committee any enquiries on the interpretation, or proposals for change, and keep the UK interests informed;
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Cross-references

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**Printed boards and printed board assemblies –
Design and use
Part 5-6: Attachment (land/joint) considerations –
Chip carriers with J-leads on four sides
(IEC 61188-5-6:2003)**

Cartes imprimées et cartes imprimées
équipées –
Conception et utilisation
Partie 5-6: Considérations sur les liaisons
pistes-soudures –
Composants à sorties en J sur quatre
côtés
(CEI 61188-5-6:2003)

Leiterplatten und Flachbaugruppen -
Konstruktion und Anwendung
Teil 5-6: Betrachtungen zur Montage
(Anschlussfläche/Verbindung) -
Bauelemente mit J-förmigen Anschlüssen
auf vier Seiten
(IEC 61188-5-6:2003)

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

The text of document 91/338/FDIS, future edition 1 of IEC 61188-5-6, prepared by IEC TC 91, Electronics assembly technology, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61188-5-6 on 2003-03-01.

This European Standard should be read in conjunction with EN 61188-5-1:2002.

The following dates were fixed:

- latest date by which the EN has to be implemented
at national level by publication of an identical
national standard or by endorsement (dop) 2003-12-01
- latest date by which the national standards conflicting
with the EN have to be withdrawn (dow) 2006-03-01

Annexes designated "normative" are part of the body of the standard.
In this standard, annex ZA is normative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 61188-5-6:2003 was approved by CENELEC as a European Standard without any modification.

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INTRODUCTION

This part of IEC 61188 covers land patterns for components with J leads on four sides. Each clause contains information in accordance with the following format:

The proposed land pattern dimensions in this standard are based upon the fundamental tolerance calculation combined with the given land protrusions and courtyard excesses (see IEC 61188-5-1). The courtyard covers all issues pertaining to normal manufacturing needs.

The land pattern dimensions covered in this standard are generally applicable for reflowed solder paste processes. For immersion soldering processes (e.g. wave, jet, drag soldering), lands may have to be modified to prevent shadowing and shorting (e.g. by extending land length parallel to the direction of motion of the board and/or provision of solder thieves).

This specification offers a threefold land pattern dimensioning (levels 1, 2, and 3) on the basis of a threefold set of land protrusions and courtyard excesses maximum (max.), median (mdn.), and minimum (min.). Each land pattern has been assigned an identification number to indicate the characteristics of the specific robustness of the land patterns. Users also have the opportunity to organize the information to suit their particular design.

This standard assumes that land dimensions are always larger than component termination or lead outlines. If a user has good reason to use solder resist to limit wetting on a land, or to use lands smaller than component terminations, or to apply a concept different from that of IEC 61188-5-1, this standard may not apply.

It is the responsibility of the user to verify the surface mounting devices (SMD) land patterns used for achieving an undisturbed mounting process, including testing, and an ensured reliability for the product stress conditions when in use.

Dimensions of the components listed in this standard are those available on the market, and are for reference purposes only.

PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

Part 5-6: Attachment (land/joint) considerations – Chip carriers with J-leads on four sides

1 Scope and object

This part of IEC 61188 provides information on land pattern geometries used for the surface attachment of electronic components with J leads on four sides.

The object of this standard is to provide the appropriate size, shape and tolerances of surface mount land patterns so as to ensure sufficient area for the appropriate solder fillet, and also allow for inspection, testing and reworking of resulting solder joints.

Each clause contains a specific set of criteria, setting out details on the component, the component dimensions, the solder joint design and the land pattern dimensions.

NOTE The acronym QFJ is the naming convention used by Japan; the acronym PLCC is the naming convention used by the USA for these components.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and soldering heat of surface mounting devices (SMD)*

IEC 60191-2, *Mechanical standardisation of semiconductor devices – Part 2: Dimensions*

IEC 61188-5-1, *Printed boards and printed board assemblies – Design and use – Part 5-1: Attachment (land/joint) considerations – Generic requirements*

IEC 61760-1, *Surface mounting technology – Part 1: Standard method for the specification of surface mounting components (SMDs)*